Stacked Multi-Level Long Pulse Modulator Topology for ESS

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Abstract— **The European Spallation Source (Lund, Sweden) is an under construction multi-disciplinary research facility to be based around a Linear Particle Accelerator which is to provide 2.86 ms long proton pulses at 2 GeV at a pulse repetition rate of 14 Hz, representing an average beam power of 5 MW. To accommodate the requirements of the proton linac, a large number of klystrons driven by power electronic modulators will be needed. Conventional long pulse modulators are pulse transformer based and commonly exhibit poor efficiency, low power density, large footprint and cost. In addition, these topologies due to their nature in combination with the above cited high peak power requirement for short periods of time commonly produce prohibitive levels of flicker and harmonic content while operating at suboptimal power factor, problems usually corrected by both costly and spacious external grid compensators. This paper presents the stacked multi-level (SML) klystron modulator topology, a novel, modular concept based on high-frequency transformers and rectifier bridges stacked in series, believed to better suit the application and better satisfy ESS requirements, directly addressing the mentioned shortcomings of conventional topologies. The development of this new klystron modulator topology has included the design and construction of a reduced scale prototype with the potential of delivering long (3.5 ms) high quality dc pulses (0-99% rise time of less than 100 µs and flat top ripple less than that of 0.15%) of high voltage (115 kV) and high power (peak power > 2 MW) while on its own maintaining excellent AC grid power quality (low flicker operation < 0.2%, sinusoidal current absorption with total harmonic distortion < 3%, and unitary power factor). The paper in detail describes the essential features of the topology and outlines the working principle, presenting results from both simulation and experimental work.**

Keywords— Klystron modulator; Active Front End; High Voltage High Frequency transformers; Flicker free operation; Pulse power quality

I. INTRODUCTION

Traditionally, solid state long pulse klystron modulators are based on topologies requiring pulse transformers [1], the size and weight of which are highly impacted by pulse length, pulse power, and required rise time. In the case of the ESS Linac, these parameters have to be combined in an unprecedented and extremely demanding way. Indeed, the pulse length is defined by accelerator beam length (2.86 ms) derived from requirements imposed by the neutron physics users. Simultaneously, pulse rise time should be as short as possible in order to improve system efficiency while the pulse power should be maximized so as to allow connection of several klystrons in parallel to the same modulator, decreasing the total modulator quantity and hence total cost and footprint in the accelerator gallery. Furthermore, practical pulse transformer based topologies require the following additional autonomous systems. First, flat top droop needs to be compensated for. This system may be passive, in which case it will be spacious, or active, in which case it will affect system efficiency and further complicate regulation. Second, a pulse transformer demagnetization circuit, difficult to implement given the tradeoff between demagnetization time (linked to pulse repetition rate) and maximum allowed reverse voltage defined by the klystron, is necessary. Finally, a dc flux bias power supply is required, which if implemented passively will be spacious, requiring additional oil tank space. The complex synchronization of these systems over the entire power operating range is an additional drawback. For these reasons, such topologies are typically non-modular, i.e. they are formed by one capacitor charger, one capacitor bank, one high voltage switch, one pulse transformer, and, additionally, one set of the auxiliary systems outlined above. Hence, no redundancy is possible, and mean time to repair might be considerably higher for certain subsystems [2].

Below, the novel SML (Stacked Multi-Level) topology is described and analyzed as an alternative klystron modulator well suited particularly for long pulse and high power applications, e.g. the ESS Linac.

II. THE SML MODULATOR TOPOLOGY

A. SML Modulator Concept

Fig. 1 shows a simplified conceptual block diagram of one SML modulator module. It is formed by an AC/DC Active Front-End [3] working as an active rectifier followed by a DC/DC buck converter charging a capacitor bank (main energy storage) at low voltage (~1 kV). After the main capacitor bank is a pulse forming stage comprised by a high frequency DC/AC inverter feeding the primary winding of a High Voltage High Frequency (HVHF) transformer, amplifying the voltage waveform. It is followed by a high voltage full diode bridge rectifier and low pass filter,

producing a smooth flat top pulse without degrading the rise time [4]. Each conversion stage is discussed in detail in the following sections.

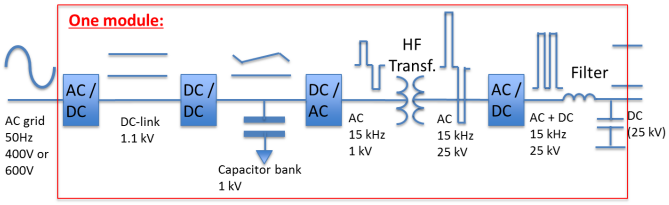

Fig. 1. Conceptual diagram of a SML modulator complete module

a) Active Front-End: The first conversion stage is an active rectifier implemented by a three-phase voltage source converter as shown in Fig. 2. This converter connects the modulator to the grid via a three-phase inductor, indicating that measurement of the grid voltage along with resulting grid current allows for active control of grid current shape, magnitude and phase through proper selection of converter output voltage. In this case, knowledge of average output power and desired dc-link voltage provides reference grid current in a straightforward fashion. Grid voltage and resulting line current and dc-link voltage are shown in the below figure.

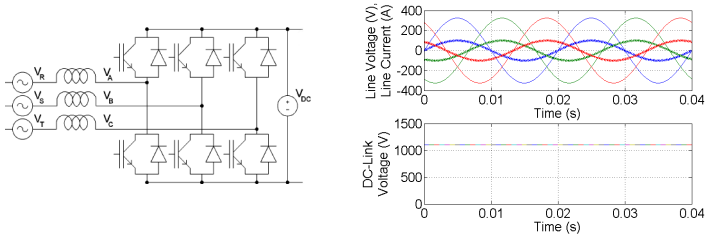

Fig. 2. Schematics of AC/DC Active Front End and typical waveforms

b) DC/DC Capacitor Bank Charger: Following the active rectifier is a step down converter connecting the dc-link capacitor to the main capacitor bank storing the energy needed in pulsing through an inductor, Fig. 3, again allowing inductor current control.

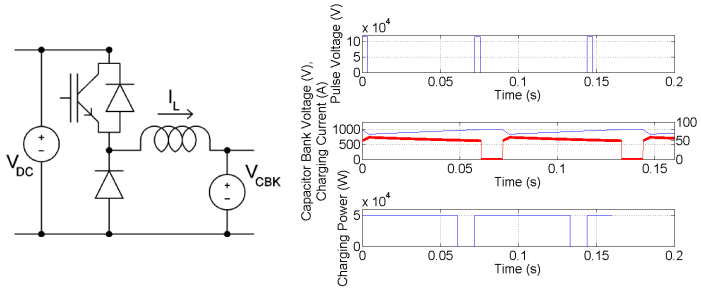

Fig. 3. Schematics of DC/DC Converter and typical waveforms

In pulsing, energy is taken from the capacitor bank and fed to the output load, reducing the capacitor bank voltage. This energy needs to be replenished before the next pulse, and ideally this is done at constant rate, i.e. the current should exhibit inverse behavior with respect to the capacitor bank voltage, allowing constant power charging, such that the energy is replenished just in time for the next pulse. If this is accomplished, flicker-free operation is attained despite sourcing high power pulsing loads, Fig. 3. In summary, the two first power electronic conversion stages allow for constant power (i.e. flicker-free) capacitor bank charging while effectively shaping grid current so as to be sinusoidal and in phase with the grid voltage, reducing both generated grid current harmonics and reactive power to a minimum.

c) DC/AC H-Bridge Inverter: Having attained the required capacitor bank voltage, the following stages step up and shape this voltage to exhibit desired pulse characteristics, such as those outlined in Table I. The first step in this chain is an H-bridge inverter seen in Fig. 4, synthesizing an AC square wave fed to a high voltage module explained in sub-section 4.

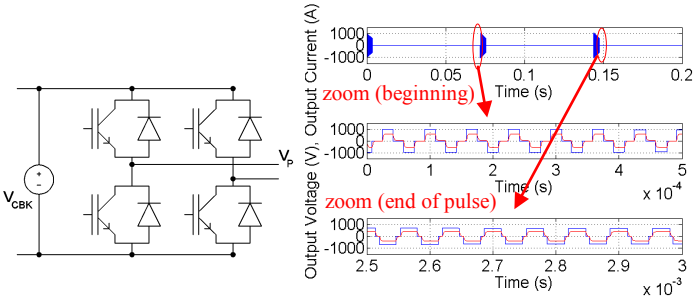

Fig. 4. Schematics of DC/AC H-bridge inverter and typical waveforms in pulsed mode

As is clearly seen in Fig. 4 and as was explained in sub-section 2, the capacitor bank voltage decreases throughout the pulse. This decrease, of course, directly affects the average output voltage and is ultimately seen as output pulse flat-top droop, something that must be avoided. As is seen in Fig. 4, this issue is in the SML topology counteracted by increasing converter duty cycle.

d) High Voltage Module: Following the H-bridge inverter is a high voltage module comprised of a HVHF transformer, a high voltage rectifier, and a high voltage output filter, Fig. 5, effectively amplifying, rectifying, and filtering the generated pulse waveform.

B. SML Modulator Configuration for the ESS Linac

The main requirements for the ESS Linac klystron modulators, allowing to power up to 4 x 704MHz 1.6MWpk klystrons in parallel, are shown in Table I.

The modularity of the SML topology, along the different power conversion stages, facilitates compliancy with these requirements particularly when it comes to conjugate parameters difficult to conciliate together like high pulse power, high average power, high pulse length, fast rise/fall times, high flat-top accuracy.

The configuration adopted for the ESS klystron modulators is shown in Fig. 6. In order to reduce the number of components, increasing reliability and reducing cost, the number of power conversion modules was adjusted on each stage:- 3 modules for capacitor charging (#1A,#1B,#1C); 3

modules for the inverters with double DC/AC's per module (#2A,#2B,#2C); 6 modules for the HV stage (#3A1/A2, #3B1/B2, #3C1/C2). This arrangement also allows splitting the total energy storage amongst three independent capacitor banks therefore reducing the amount of released arc energy in case of short circuits or insulation breakdown.

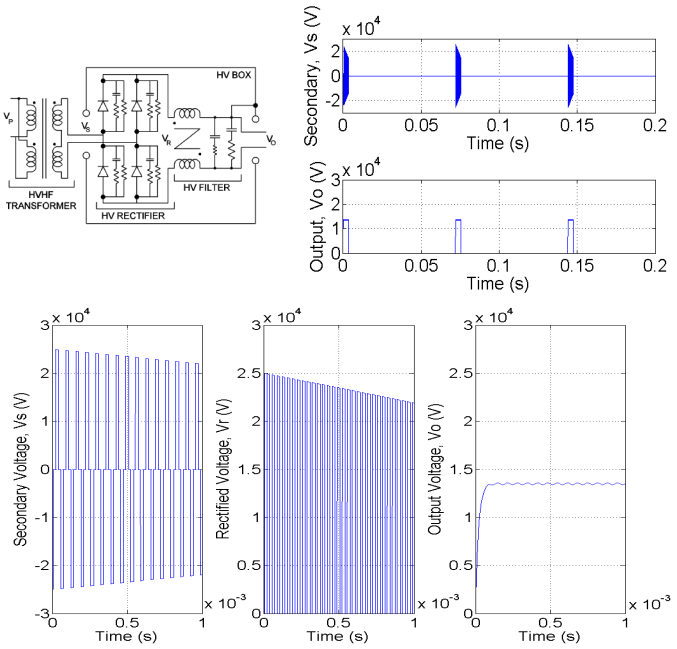

Fig. 5. Schematics of HV module and typical waveforms in pulsed mode

All six HV modules on the output stage are connected in series in the oil tank; each module delivering 20 kV during the pulse. On the AC grid side, the 3 capacitor chargers are connected in parallel in their input side and each one charges a separated capacitor bank. In order to allow for this arrangement, the HVHF transformers provide galvanic isolation, primary to secondary, on the order of 160kV$_{DC}$/1min.

III. Implementation of SML Modulator Topology for the ESS Linac

A. Reduced Scale Prototype

In order to validate this new topology, ESS launched a R&D project in collaboration with Lund Technical University in June 2013. This project included construction and validation of a reduced scale technology demonstrator rated for all requirements mentioned in Table I, except for the pulse current amplitude which was set to 20A (rated power 20% of the full scale units). This approach of prototype validation at full voltage but reduced current allows for a cheaper and faster validation of the entire concept in view of a future straightforward and low risk scaling up process. Indeed, in HV systems the most difficult design aspect is to withstand the voltage (insulation, parasitic capacitances) rather than the current which stays always low therefore constituting mainly a normal thermal problem.

Fig. 7 shows the detailed electrical schematic of the modulator prototype derived from the configuration depicted in Fig. 6. It comprises the following main components:- 1x EMC filter (1), 1x Main Circuit Breaker (2), 3x AC contactors to isolate each sub-system (3), 3x AC line inductors (4), 3x AC/DC+DC/DC power stacks (5), 3x DC inductors (6), 3x DC common mode filters (7), 3x double DC/AC power stacks (8), 1x HV oil tank assembly (9) with 6 HV modules connected in series at the output side. All of these components and sub-assemblies, except (9), are standard off-the-shelf.

TABLE I. Main Requirements for the ESS Linac Modulators

Pulse voltage amplitude, U_N	-115kV
Pulse current amplitude (total for 4 klystrons in //)	100A
Pulse length (50% amplitude)	3.5ms
Pulse repetition rate:	14Hz
Max. pulse rise time (0..99%) / fall time (100..10%)	120µs / 150 µs
Max. pulse overshoot	2% of U_N
Max. pulse reverse (backswing) voltage	10% of U_N
Max. voltage droop on pulse flat-top	1% of U_N
Max. voltage ripple on pulse flat-top	0.15% of U_N
AC grid line voltage	600V
Max. flicker on AC grid	0.3% of U_N
Max. current THD on AC grid	3%
Min. efficiency, AC grid to HV output	90%

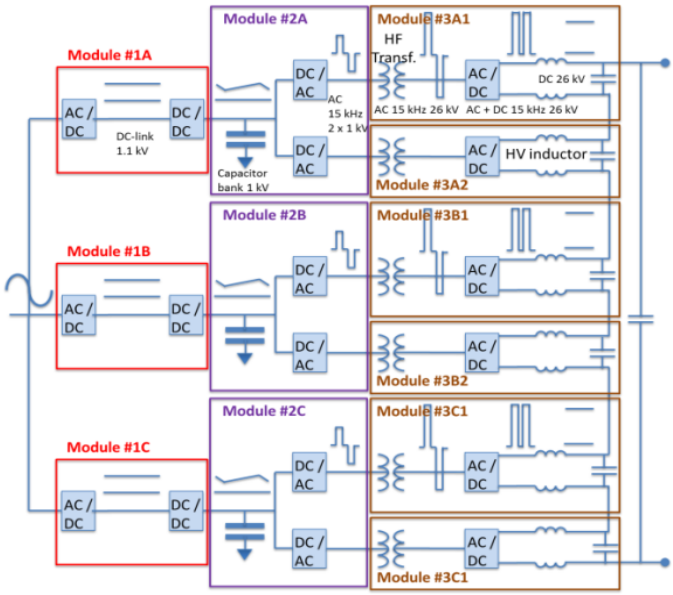

Fig. 6. SML modulator configuration diagram for ESS Linac

In the capacitor chargers, the AC/DC and the DC/DC converters operate at switching frequencies of 5kHz and 7.5kHz, respectively. The inverters (DC/AC's) and HV modules operate at a switching frequency of 15kHz. These values seem a good compromise between efficiency and lifetime of power semiconductors in one hand and low ripple/fast transient response of the HV pulse in the other hand. The DC-link bus operating voltages of the AC/DC+DC/DC capacitor chargers and DC/AC inverters was chosen to be 1.1kV and 1kV respectively, therefore compatible with usage of common 1.7kV IGBT technology.

Fig. 8 shows the corresponding mechanical layout. The LV power conversion stage was accommodated into two cabinets (#1 and #2). Cabinet #2 is placed on the top of the oil tank in order to allow straight and short connections between the

DC/AC inverters and the HVHF transformers which is crucial to reduce stray inductances and voltage drops in the connections.

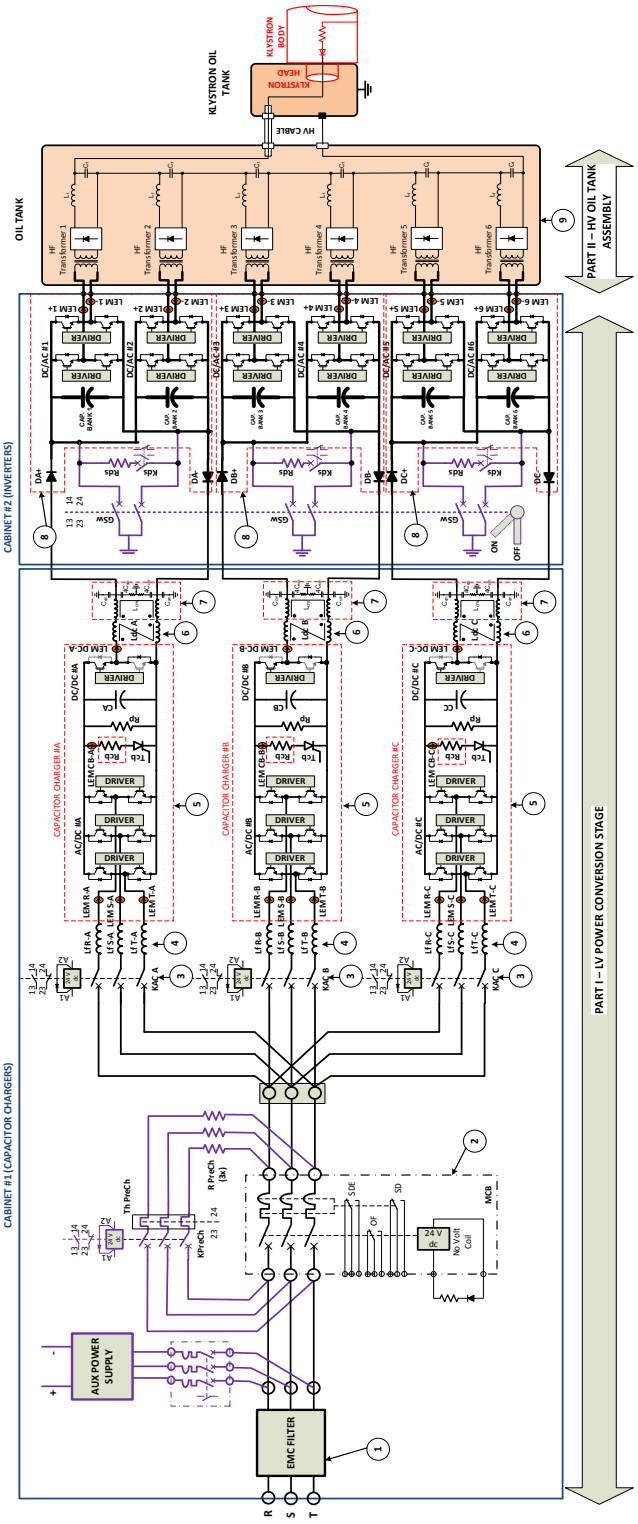

Fig. 7. SML Modulator detailed electrical schematics

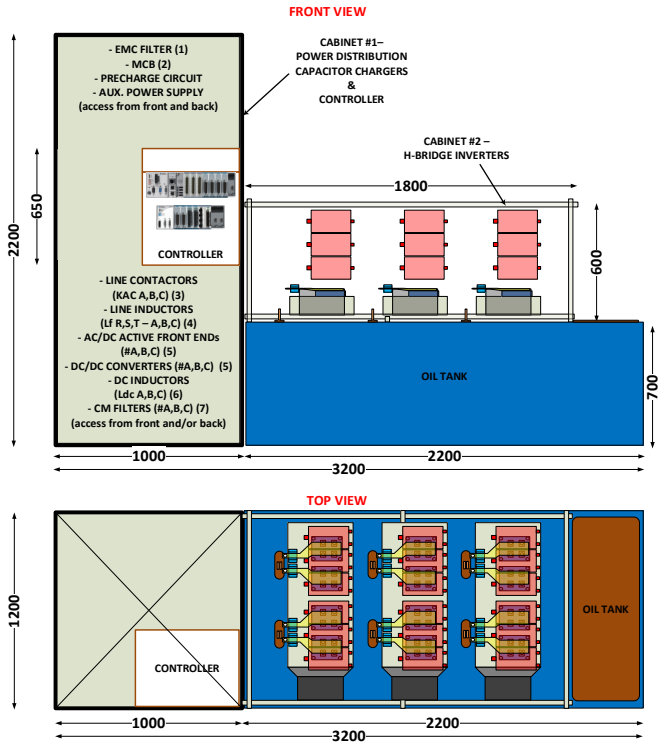

Fig. 8. SML Modulator mechanical layout for reduced scale prototype rated 115kV/20A ; 3.5ms/14Hz (dimmensions are in mm)

Fig. 9 shows the SML modulator reduced scale prototype installed in the test stand. The HV oil tank was moved out from its final location, underneath cabinet #2, in order to facilitate inspection and accessibility during the testing phase.

a) The HV Oil tank assembly: For voltage insulation in the order of 100kV and above, oil is believed to be the most suitable insulation medium in particle accelerator systems. The HV oil tank assembly for the SML modulators at ESS (Fig. 10) hosts mainly the 6 HV modules, an output filter and a HV divider. For environmental reasons, a synthetic ester is preferred, although their insulation strength might be lower in the long term with respect to conventional mineral oil.

b) HV modules: A HV module is shown in Fig. 11. It comprises one HVHF transformer rated 1kV/500A_{pk} in primary and 25kV/20A_{pk} in secondary and a switching frequency of 15kHz. The transformer core is made with two nanocrystalline rings for lower losses. The primary windings are made with insulated copper foils rolled around each limb. The two secondary windings are made with standard enamelled wire and supported by two fiberglass frames. The anti-corona cage "hides" the sharp edges of the primary busbars and of the core from a field control perspective. The HV rectifier and HV filter are located in an aluminium HV rectifier box.

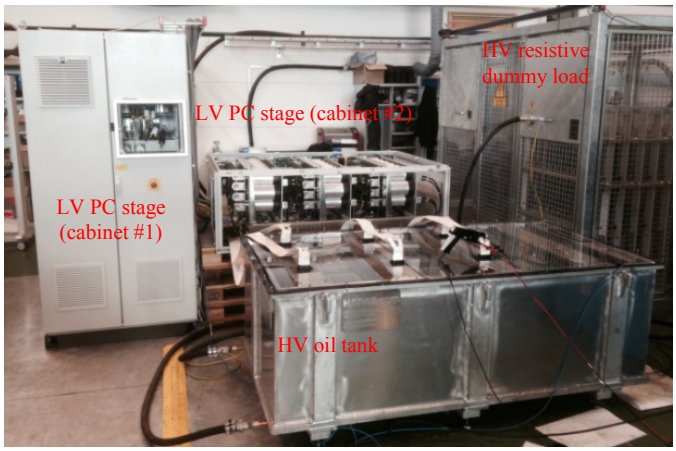

Fig. 9. SML modulator reduced scale prototype in the test stand at LTH

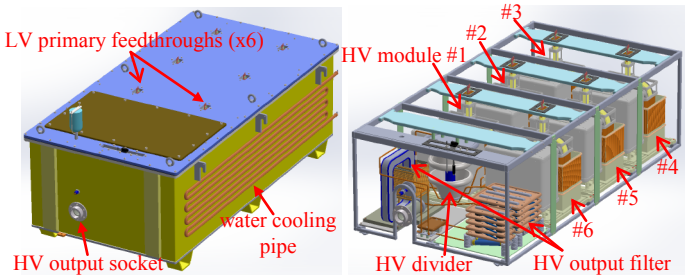

Fig. 10. Complete HV oil tank assembly: Left – external view; Right – Internal view

This box is floating with respect to the tank wall (ground) with an insulation withstanding of $160kV_{dc}$/1min. The circuit inside the box operates at $25kV_{pk}$ with respect to the box walls and is insulated at a 50kVdc/1min level. By this way, the HV rectifier box works as a shield or floating ground with regards to field control, "hiding" all sharp edges of the components and circuit inside with respect to the tank wall.

The HV rectifier bridge is built with 21 PCB's per leg (2 legs needed to form a full bridge) stacked and mounted together around a central insulation rod. Each PCB comprises 4 1.2kV/50A diodes connected in series. In parallel with each diode a RC snubber is connected in order to dump the oscillations created by the resonance between the HVHF transformer and the parasitic capacitances of the system. Furthermore, a static voltage balancing resistor is also connected in parallel with each diode. A 4mm diameter copper anti-corona ring is welded on the external edges of each PCB for field control purposes.

The HV filter inductor is made with a conventional 0.25mm thick laminated silicon steel core. The core is formed by two U shape sections mounted together on a fiberglass supporting frame. Two windings are wound on each limb over fiberglass plates also secured by the same frame allowing for a 10mm clearance between the windings and the core which is connected to the floating ground (aluminium box). This technique is important to allow the oil to fill this gap and ensure a liquid insulation layer, judged to be the most reliable one in those applications where high voltage and high frequency is simultaneously required.

All solid insulators for mechanical supporting on the HV modules are of fiberglass G11.

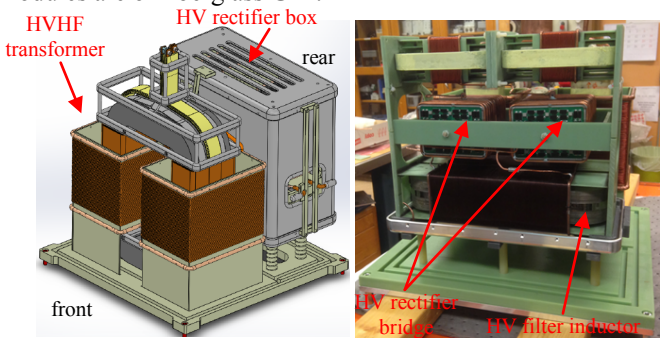

Fig. 11. One HV module; Left: 3D CAD model; Right: Picture from rear side without box enclosure

B. *Full Scale Modulators*

The strategy for the development of the full scale modulators is based on the same topology and schematics shown in Fig. 7. The voltage levels and switching frequencies at the different stages will remain the same as in the reduced scale prototype, except for the AC line voltage which will be 600V. Each component will be scaled up in current by a factor of 5. The mechanical layout will also be similar to the one of the reduced scale prototype (Fig. 8) although the space above cabinet #2 will be filled with the required extra capacitors. The design of the HV oil tank assembly (Part II) is complete. The design of the LV power converter stage (Part I) will be finalized by August 2016. The procurement of the series units (3 units for the RFQ/DTL + 9 units for the Medium Beta Linac) is foreseen to start by August/September 2016.

IV. Validation

A. *Simulation Results*

Below, simulation results are shown for the AC grid input side in Fig. 12, and for the output side in Fig. 13. Note the attainment of sinusoidal grid current in phase with the grid voltage, representing minimal reactive power and low flicker (0.06%) during high power pulsing operation.

On the output side, a pulse rise time (0-99%) of approximately 120 µs is achieved. Flat top ripple less than 0.15% and flat top droop below 1% is seen.

B. *Experimental Results*

In the below figures, experimental results at reduced scale prototype rating are shown. Fig. 14 and Fig. 15 correspond to Fig. 12 and Fig. 13, respectively. Again, the grid current is seen to be sinusoidal and in phase with the line voltage (i.e. unitary power factor) and of constant amplitude (i.e. flicker free operation). This may also be inferred from the capacitor bank voltage and charging current waveforms – the current is seen to exhibit inverse behavior to the voltage, keeping instantaneous charging power constant over time.

The output side waveforms are also seen to agree with simulation results shown in Fig. 13, validating the derived simulation model. It should be noted that all experimental

results demonstrated in this section were obtained after a successful 12 hour continuous heat run test at nominal operating point.

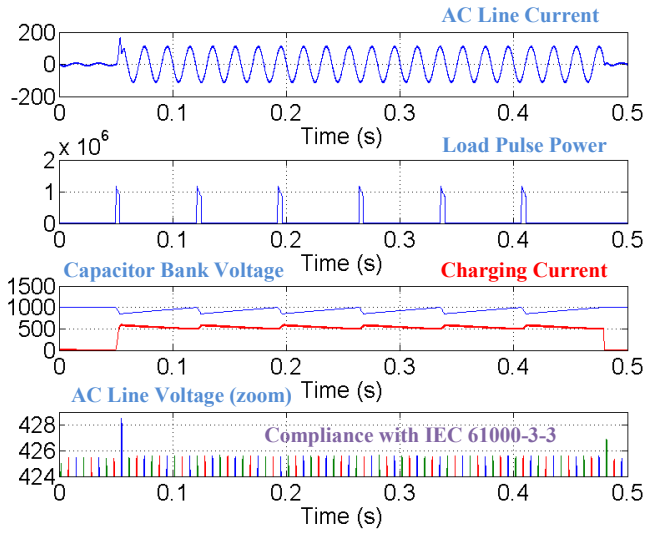

Fig. 12. Capacitor charger waveforms and AC grid power quality (simulation)

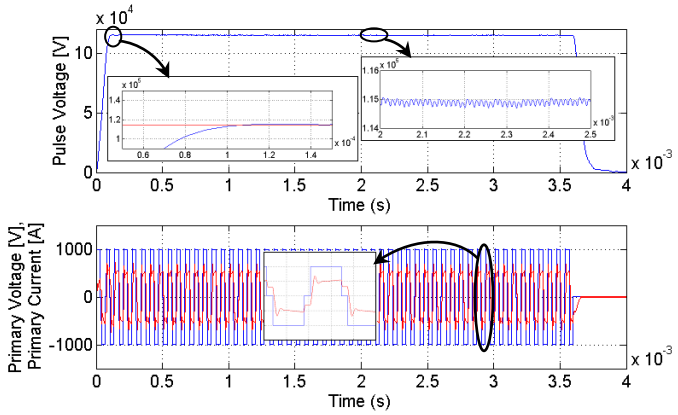

Fig. 13. Output pulse waveforms (simulation)

V. Conclusions

In this paper, the SML topology has been presented as an alternative to conventional pulse transformer based topologies for long pulse high power applications.

The topology is modular, i.e. redundancy may be exploited, increasing system power density as well as facilitating maintenance. Utilization of a HF transformer also means avoidance of auxiliary systems such as dc flux bias and transformer demagnetization, requirements for pulse transformer based topologies. Flat top droop compensation is intrinsic to the pulse generation circuit stage allowing for closed loop feedback regulation.

With a reduced scale prototype, a pulse rise time of 120 µs as well as a flat top droop less than 1% has been achieved experimentally. Simultaneously, a flicker below 0.3% with grid current THD better than 3% and unitary power factor were demonstrated.

The footprint of the reduced scale prototype modulator is relatively compact (1m x 3m). The circuit uses standard off the shelf components to maximum extent (including entire LV power conversion stage) and is straightforward to scale by at least a factor 5 through increase of rated power/current, keeping the same electrical and mechanical arrangement, but scaling up each component individually in current.

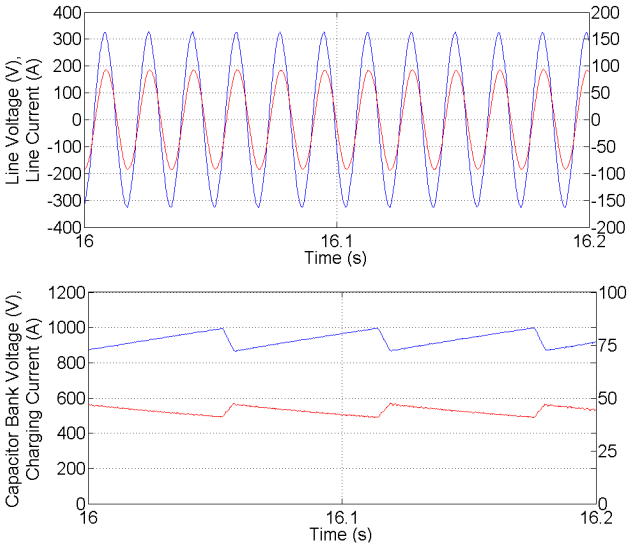

Fig. 14. Input side waveforms (experimental)

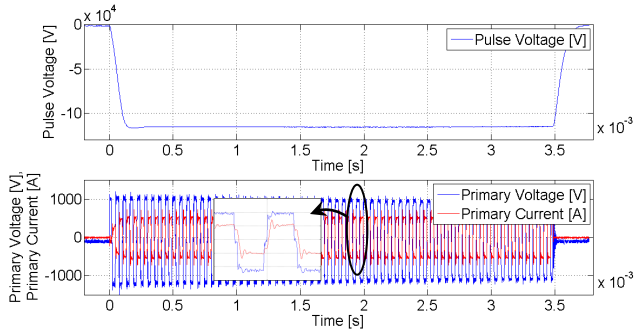

Fig. 15. Output pulse waveforms (experimental)

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