Tokamak Vertical Stability Coil Power Supply based on Modular Multilevel Converter

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Abstract— **Tokamak is a nuclear fusion reactor that involves high-current power supply systems. Vertical stabilization is required to achieve desired plasma current and elongation in the tokamak. Due to the high current and fast current dynamic response requirements, circuit topology of power supply for vertical stabilization coil is important. In this paper, a full-bridge single-phase modular multilevel converter (MMC) is proposed. Circuit design, voltage balancing strategy and circulating current suppression control method are presented. The proposed topology and strategies are verified in simulations with MATLAB/Simulink.**

Keywords—Nuclear fusion reactor; Tokamak; Power supply; Modular Multilevel Converter (MMC); Voltage balancing; Circulating current suppression

I. INTRODUCTION

Tokamak is a nuclear fusion reactor based on magnetic confinement. During the operation of Tokamak, a large plasma current, in the scale of mega-ampere (MA), is induced around the tokamak's vessel. Multiple sets of coils are deployed in order to keep the plasma current away from the vessel. One of them is the vertical stabilization coil. The current going through the coil will produce a magnetic field, which can control the position of plasma. In order to achieve the desired driving current, the power supply for coil is required to meet the high current and fast current dynamic response requirements, which present significant challenges to the circuit and associated controller design.

Various repetitive pulse power generators have been proposed. References [1]-[3] reported the use of switching devices for repetitive pulse generators for various load conditions. Hardware experiment in [3] suggests that the output pulse rising time can be as short as 70ns when the pulse is 3 times the source voltage. Reference [4] proposed a circuit topology with modular solid-state switching. Based on the desired voltage levels, different numbers of capacitors from one arm can be put in series creating the pulse while the capacitors from the other arm are connected in parallel to charge. However, these types of pulse generators are only capable of generating single pulses whereas the required output current consists more than simply a pulse: there are also small pulses of 6 Hz and 10 Hz in between them. Such an output requires the pulse generator to also have control flexibility and good dynamic performance.

In recent years, vertical stabilization power supply systems with different circuit structures have been studied. Thyristor AC/DC converters are commonly used for such power supply design owing to the high current rating [5] [6]. Multilevel inverters with carrier phase shift half bridge were proposed to achieve high voltage and large current requirements [5]. Thyristor-based converters are connected in series with switching network unit, but fast response is still one of main challenges [6].

MMC is an attractive topology as power sources because of its ease of assembly, dynamic response and high reliability. Each arm of an MMC is formed by multiple sub-modules, each sub-module is composed by a pair of switches and a capacitor. By controlling the switch pair, a sub-module could output two voltage levels: zero or capacitor voltage V_C. MMC was first introduced in 2003 and had quickly gained popularity for medium and high voltage applications such as high voltage DC transmission and motor drives [7]. MMC high-voltage direct current (HVDC) application was first proposed in [8] and Siemens uses MMC to achieve sinusoidal AC output voltage for HVDC transmission system [9].

A power supply for voltage stabilization coils based on MMC was proposed in [10] where an individual DC voltage source was used for each capacitor. Although the converter fulfills the output requirement with fast dynamic response, the individual DC power sources could be both expensive and bulky. Therefore, in this paper, a full-bridge single-phase MMC solution with a single centralized DC power source is proposed. Without the individual power supply, two issues would arise: 1) unbalanced capacitor voltage among sub-modules, 2) high circulating current through each leg, which would significantly increase the electrical stress on the circuit components. Although the same type problems would occur for HVDC and motor drive applications, the controller reference is relatively straightforward with sinusoidal waveforms. However, for pulse power applications such as the vertical stabilization coil in Tokamak, the reference current is comprised of a very high initial current peak with fast ramp, and the frequency component of the reference is more complicated.

In the rest of this paper, MMC topology and its control strategies for voltage balancing and circulating current control

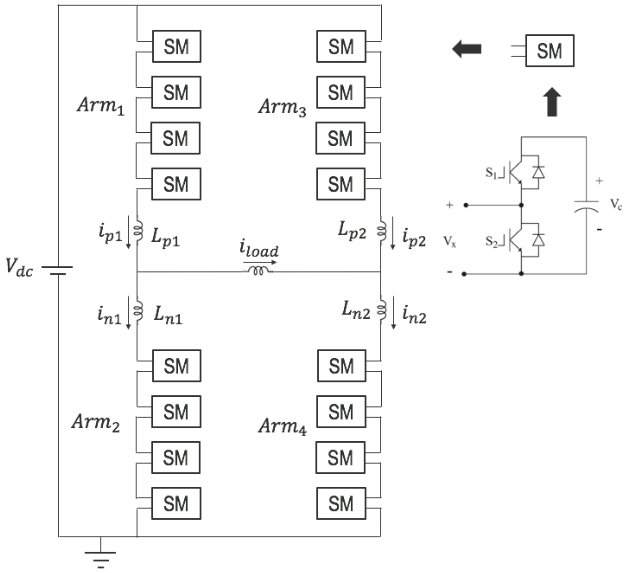


Fig. 1 A full-bridge single phase modular multilevel (MMC) power supply for vertical stabilization (VS) coils.

for vertical stabilization coil power supply are proposed in Section II and simulation results and discussions are presented in Section III. In Section IV, conclusion and future works are summarized.

II. MMC TOPOLOGY AND CONTROL STRATEGY FOR VERTICAL STABILIZATION COILS POWER SUPPLY

A. *MMC Citcuit Toplogy*

A full-bridge single-phase MMC with 16 sub-modules (SMs) and a centralized power source is proposed in Fig. 1. The system parameters are given in Table 1 and its reference output current is shown in Fig. 2. Because of the centralized power supply, capacitor voltage unbalance and circulating current issues become challenging.

TABLE I. SYSTEM PARAMETERS

Items	***Values***
V_{dc}	4000 V
N	4
r_{load}	0.01 Ω
l_{load}	140 μH
C_{SM}	2 F
$R_{p(n)}$	0 Ω
$L_{p(n)}$	1 mH
f_c	2000 Hz

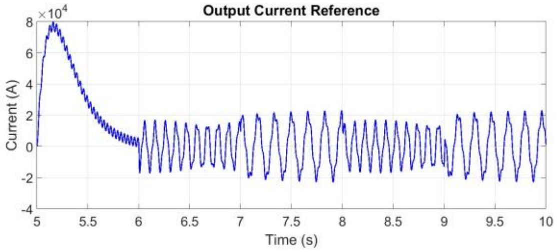


Fig. 2 The waveform of the output current reference.

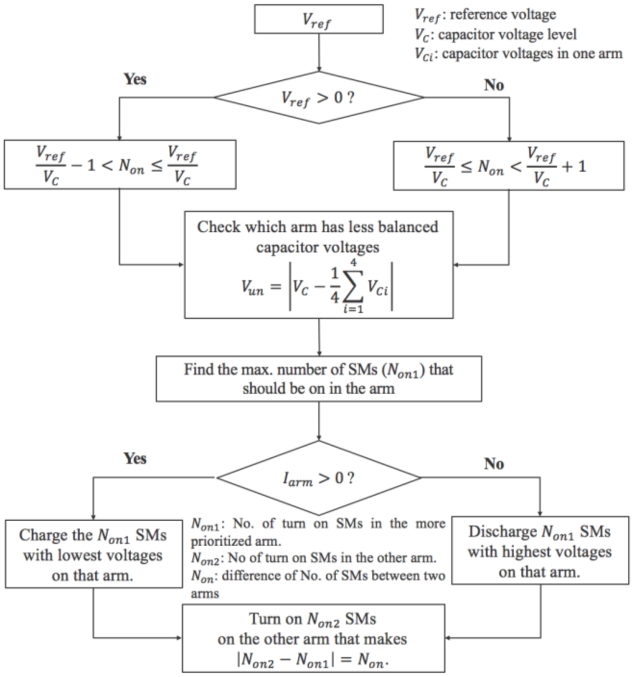


Fig. 3 Flowchart of the proposed voltage balancing control

B. *Voltage Balancing Control*

In the MMC, capacitors have different on-off times, which cause capacitor voltage unbalance. To balance the capacitor voltages, different voltage balancing strategies have been developed for multilevel converters. Conventional voltage balancing control (VBC) was proposed in [11] and [12], in which capacitor voltages are monitored and sorted. The algorithm selects sub-modules with the lowest or highest capacitor voltages to turn on based on the directions of arm currents. In [13], reduced switching-frequency (RSF) voltage balancing was proposed. The principle of this control algorithm is based on the conventional method. But the state of sub-modules is also monitored every cycle in RSF algorithm so that unnecessary switching could be avoided. A modified control algorithm is presented in this paper which is also based on the conventional voltage balancing algorithm. But the proposed MMC topology is single-phase. So, the algorithm will first determine which arms have less balanced capacitor voltages. Then, these arms are prioritized when determining the number of on-state sub-modules. The proposed algorithm prevents extremely over or under charged capacitors. Fig. 3 presents the flowchart of the proposed algorithm.

C. *Circulating Current Suppression Controller (CCSC)*

Another major challenge is the circulating current which occurs due to the difference between leg voltage and DC source voltage. Circulating current increases the stress on circuit component and should be suppressed through appropriate controller design. References [14] – [16] have presented comprehensive studies of circulating currents in HVDC applications. A circulating current controller for three-phase MMC based on Proportional Integral Resonant (PIR) controller is proposed in [15]. However, for the majority of MMCs used in HVDC, suppressing circulating current involves dq transformation. And due to the nature that HVDC supplies the demanded power for industrial, commercial or residential loads, the controller must use real and reactive power to calculate the voltage or current reference, creating an extra control loop.

To model the circulating current in this full-bridge single-phase MMC, one way is to focus on one leg at a time. There are two legs in the proposed MMC, Arm1-Arm2 and Arm3-Arm4. And the circuit diagram for the Arm1-Arm2 leg is given in Fig. 4.

As shown in Fig. 4, to supply the load, Arm1 and Arm2 will both contribute. And since both arms have the same impedance, they provide half of the load current each. However, there will be a difference between the two arm currents, i_{diff}, as expressed by (1) and (2) because of the existence of circulating current,

$$i_p = i_{diff} + \frac{1}{2} I_{load} \tag{1}$$

$$i_n = i_{diff} - \frac{1}{2} I_{load} \tag{2}$$

After eliminating the common half load currents from (1) and (2), one can then write the expression for the difference current:

$$i_{diff} = \frac{1}{2}\left(i_p + i_n\right) \tag{3}$$

One way to counter-balance the effects that the circulating current imposes to the circuit is to regulate the voltages that i_{diff} induces on the two arm inductors. By Kirchhoff's Voltage Law, the voltage relations of a phase leg can be expressed with (4) and (5).

$$V_{dc} - V_p - \frac{L_p}{2}\frac{dI_{load}}{dt} - V_{diff} - e = 0 \tag{4}$$

$$-V_n + \frac{L_n}{2}\frac{dI_{load}}{dt} - V_{diff} + e = 0 \tag{5}$$

Where V_{diff} is the voltage induced by i_{diff} on the arm inductance and e is the output of the phase leg.

$$e = \frac{V_n + V_{dc} - V_p}{2} \tag{6}$$

From (4) and (5), one can have the following equation:

$$\frac{1}{2}\left[V_{dc} - \left(V_p + V_n\right)\right] = V_{diff} \tag{7}$$

With (6) and (7), it is possible to get the equations to determine the reference voltage for Arm1 and Arm2.

$$V_{pref} = V_{dc} - V_{diff} - e \tag{8}$$

$$V_{nref} = e - V_{diff} \tag{9}$$

Equations (8) and (9) provide the theoretical basis for the circulating current suppression controller design. By subtracting V_{diff} from the original reference, one is able to modify the arm currents to negate the effects of i_{diff} without changing the phase output e and therefore the load voltage and current will not be affected.

References [17] and [18] have shown that the circulating current in a MMC contains mostly 2nd order harmonics when it is used for HVDC with a sinusoidal output. However, in the proposed MMC, the output of each phase also contains a noise. So the expression of the voltage e has the following form:

$$e(t) = E_0 \sin(\omega_0 t) + E_n \sin(\omega_n t + \varphi_n) \tag{10}$$

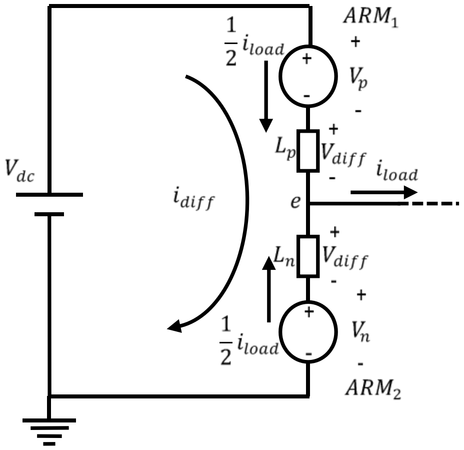


Fig. 4 The cause of circulating current and its path.

Where ω_0 is the fundamental frequency of the output while ω_n is the frequency of the noise. And the load current can be expressed as the following:

$$i_{load}(t) = I_0 \sin(\omega_0 t + \varphi_i) + I_n \sin(\omega_n t + \varphi_{in}) \tag{11}$$

Since the difference current is the one that actually provides power to the load from the DC power source, the following equation can be written:

$$V_{dc} i_{diff}(t) = e(t) i_{load}(t) \tag{12}$$

The mathematical expression of instantaneous i_{diff} can be then derived by substituting (10) and (11) into (12) as following:

$$i_{diff} = I_{dc} + i_1(2f_0) + i_2(2f_n) + i_3(f_0 - f_n) + i_4(f_0 + f_n)$$

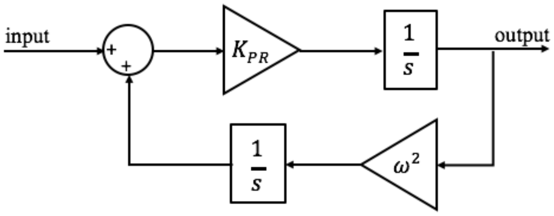


Fig. 5 The block diagram of a PR controller.

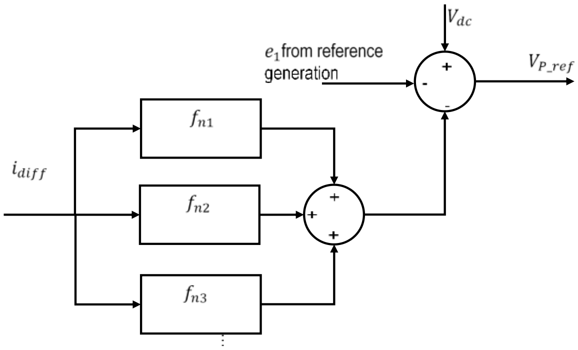


Fig. 6 The block diagram of the proposed CCSC.

When the fundamental frequency is 10 Hz and the noise frequency is 30 Hz, i_{diff} will have significant 20 Hz and 40 Hz harmonic components as well as the already existing 30 Hz noise.

To compensate the more complicated noises compared to regular HVDC, Proportional Resonant (PR) Controllers are chosen as they have an infinite gain at a certain frequency. The transfer function is given below:

$$G(s) = \frac{k_{pr}s}{s^2 + \omega^2}$$

The block diagrams of a PR controller and the circulating current suppression controller for upper arms (V_{p1}or V_{p2}) are shown in Fig 5 and 6, respectively. The PR controllers are tuned to extract the most significant components from the harmonics of the circulating current. Then the selected signals are added to create the compensation signal. The compensation signal is used to create the new reference with circulating current suppression based on (8). For the effectiveness of the proposed controller, see Fig. 14.

III. SIMULATION VERIFICATIONS

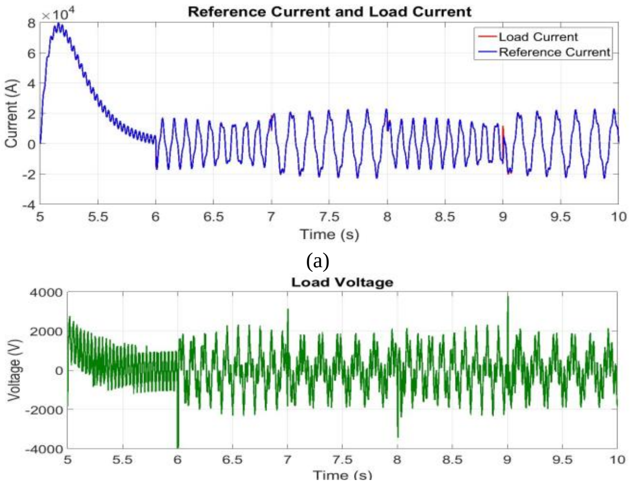
To test the performance of the full-bridge single-phase MMC with the proposed voltage balancing control and circulating current suppression control, various simulations have been conducted. System parameters during simulation are shown in Table 1. The simulations were carried out using Matlab/Simulink.

A. *Verification of the Full-bridge Single-phase MMC*

Fig. 7 shows the waveforms of the current reference, the load current and the load voltage. Detailed waveforms of the load voltage and current are plotted in Fig. 8. The proposed MMC adopts the 2N+1 Phase Shifted PWM (PSPWM), where N is the number of sub-modules in each arm. Therefore, to provide a full scale output, there will be 9 voltage levels with around 500 V per level. As mentioned previously, the load current follows a reference with a pulse that appears every 5 seconds and lasts for 1 second. During the pulse, the current ramp rate can be as high as 400 kA/s. From the figures, it is clear that the proposed MMC's output current is able to follow the reference well and that the output voltage is very well leveled at 500 V.

B. *Verification of the Voltage Balancing Control*

The challenge of voltage balancing control (VBC) with pulse power is that during the pulse, a high, long-lasting, single-direction current flows through the arms and the load. Therefore, in a phase leg, the arm that generates the pulse current is going to be undercharged while the other arm is overcharged. With conventional voltage balancing algorithm, which only turns on set numbers of sub-modules in each arm based on the reference signal but does not compare the overall capacitor voltage conditions of each arm, as shown in Fig. 9, this unbalance becomes rather severe. It can be seen that one arm reaches 2500 V while the other one at only 500 V for a long time, about the entire pulse duration. What's more, the voltage unbalance is unable to recover even long after the initial pulse period has ended. With the proposed balancing control, however, the capacitor voltages are kept at a much more balanced condition as shown in Fig. 10. Even at the peak of the pulse, the



(a)

(b)

Fig. 7 The waveforms of (a) reference vs load current and (6) the load voltage.

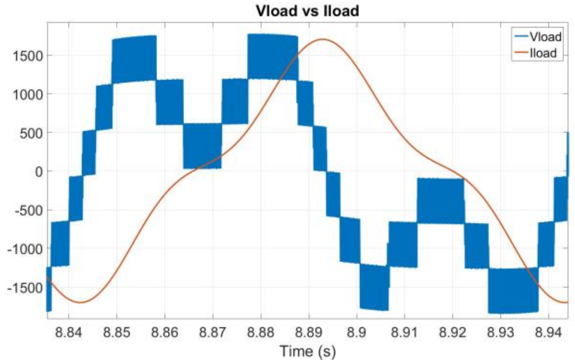


Fig. 8 Detailed load voltage and current waveforms.

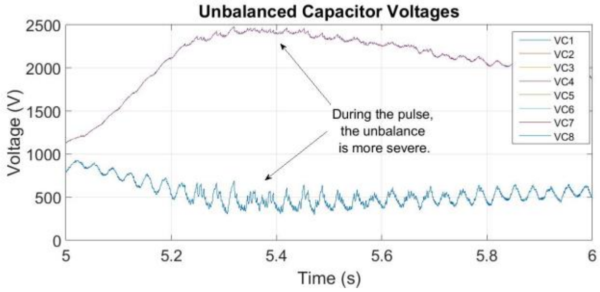


Fig. 9 Capacitor voltages during the pulse with conventional voltage balancing algorithm.

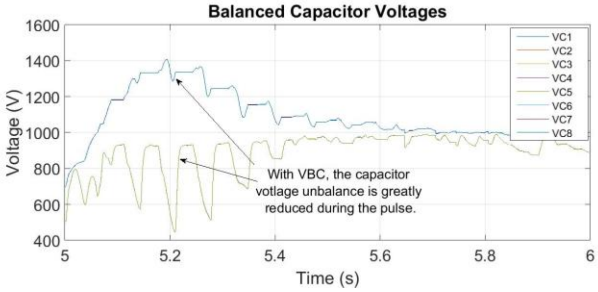


Fig. 10 Capacitor voltages during the pulse with proposed VBC.

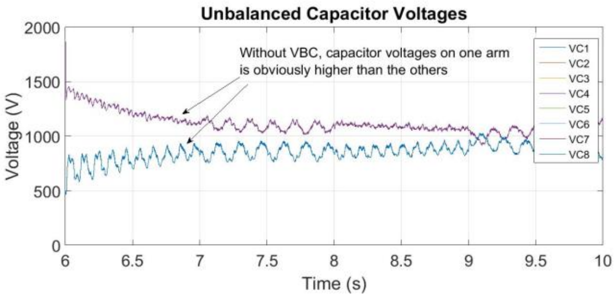


Fig. 11 Capacitor voltages during small pulses with conventional voltage balancing algorithm.

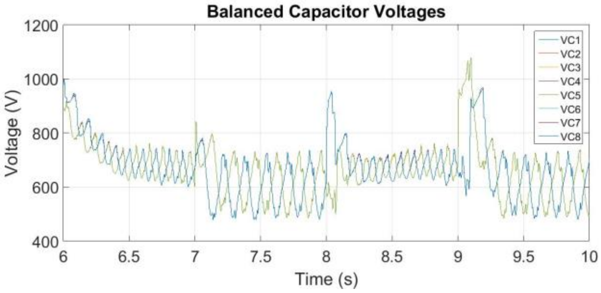
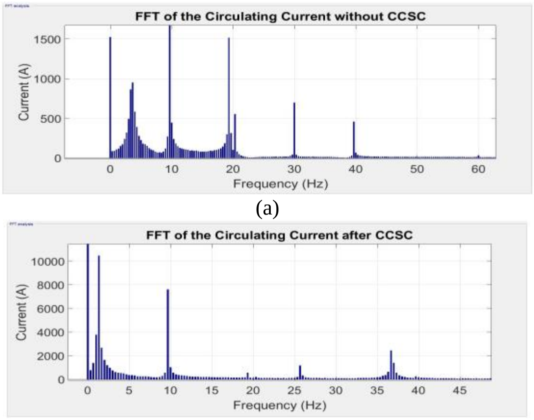


Fig. 12 Capacitor voltages during small pulses with proposed VBC.



(a)

(b)

Fig. 13 FFT of the circulating current without CCSC (a) and with CCSC (b)

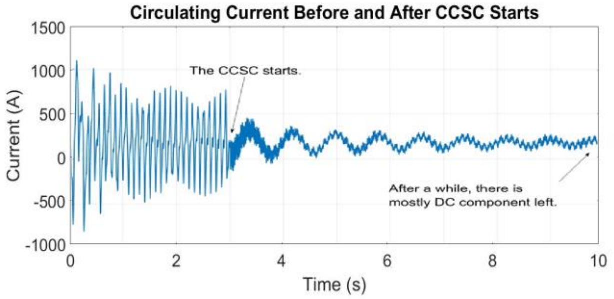


Fig. 14 Waveform of the circulating current before and after CCSC activates.

overcharged group manages to stay below 1400 V while the undercharged group is above 800 V most of the time. During the other 4 seconds of small pulses, the proposed algorithm is able to keep all the capacitor voltages at the same level while the capacitors with conventional voltage balancing control are still trying to recover from the unbalance caused during the pulse period as can be seen in Fig. 11 and 12.

C. *Verification of the Circulating Current Controller*

As discussed previously, the main goal of the circulating current suppression controller (CCSC) is to eliminate certain frequency components from the circulating current. For example, for every cycle of 5 seconds, there are 2 seconds where the fundamental frequency is 10 Hz and the noise is 30 Hz. Therefore, the controller should be able to eliminate the circulating current components of 20 Hz, 30 Hz and 40 Hz. Fig. 13 shows the comparison between the frequency spectrums with and without CCSC. The target frequencies are eliminated. Fig. 14 shows the change of the time domain waveform with CCSC. At 3 second, the most significant components in the circulating current are eliminated leaving only low frequency and high frequency ones.

IV. CONCLUSION AND FUTURE WORK

This paper investigated the potential of utilizing MMC with centralized DC power source to replace traditional thyristor based pulse power supply design. The proposed full-bridge single-phase H-bridge MMC is able to provide required pulse power to Tokamak vertical stabilization coil. With proposed voltage balancing control and circulating current control, it can operate with considerable enhancements. The voltage balancing control enables its capacitor voltages to maintain balanced with non-sinusoidal pulse output. The circulating current suppression controller is able to eliminate most of the 2nd and 4th order harmonics as well as the 30 Hz noise from the circulating current.

Future work to this project includes validation of the Simulink model with real-time simulation or control in the loop verification.

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