Charge Transfer-based Sensorless Voltage Feedback in HV Capacitor Chargers

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***Abstract*— Rapid capacitor chargers are typically used to charge a bank of capacitors with the purpose of discharging it into a pulsed power load [1,3]. Previous research shows that the charging voltage of the load can be accurately calculated in real-time using microcontroller software algorithms [1,5]. The objective of this paper is to report a hardware based approach to measure the charge transfer into the load capacitor and implicitly the capacitor charging voltage. The proposed circuit uses operational amplifiers in order to integrate the input charge. A microcontroller receives the integrated signal to compute the output voltage and stop the charging process when the target voltage has been reached. Failure to accurately detect the end of charge time could lead to an excessively large capacitor bank voltage. For this reason, the proposed method can be utilized as a primary means of end-of-charge detection in conjunction with a traditional voltage sensing scheme.**

Keywords—rapid capacitor charger; RCC; pulsed power; end of charge; charge detection

I. INTRODUCTION

Rapid capacitor chargers (RCC) are a fundamental component of many pulsed power systems like vircators, Marx generators, radar systems, pulse forming networks (PFNs), and semiconductor device testbeds. For most of these applications the required capacitor voltage can be as high as 50 kV [4]. The use of RCCs is preferred over standard high-voltage power supplies when high repetition rates are required. This is due to the inherent inefficiencies associated with charging capacitors using a voltage source [1]. Rapid capacitor chargers behave as current sources in order to charge large capacitor banks to high voltages very quickly and efficiently.

A grid-tied RCC takes power from the grid which is rectified and filtered. This DC voltage is converted to high frequency (10's of kHz) AC by high-speed switching semiconductors such as metal-oxide-semiconductor field effect transistors (MOSFET) or insulated gate bipolar transistors (IGBT). The AC voltage is fed into a high frequency step-up transformer and its output is rectified once again to charge the capacitor bank.

Multiple methods to detect the output capacitor bank voltage have been developed and discussed, however each have disadvantages that make them unsuitable in certain applications. This paper will discuss some of the existing approaches and a new method to detect the output capacitor bank voltage will be proposed.

II. END OF CHARGE VOLTAGE DETECTION METHODS

The end-of-charge detection methods can be software-based and hardware-based. A common hardware-based method used to stop the charging process is by using a high ratio voltage probe [3]. This approach works very well when the probe is designed to take full advantage of the analog to digital converter (ADC) resolution. The disadvantage of this approach is that if a lower charge voltage is needed, the accuracy of this method is significantly decreased as a result of the lower signal-to-noise ratio. Accurate output voltage monitoring is very important depending on the application. When the RCC is used in a power semiconductor device testbed, the capacitor bank voltage needs to be very accurate for consistent test results.

A very reliable software-based end of charge detection method is discussed in [1, 5]. This method uses a hardware comparator internal to a digital signal controller (DSC) to detect a predetermined current peak in order to calculate the rising and falling slope of the input current waveform. With both slopes and the known current peak, the amount of charge transferred can be calculated by the control software. Assuming that the capacitance of the bank is known, this method can be used to indirectly calculate the capacitor bank voltage and terminate the charging process as needed. This approach is very accurate regardless of the output voltage target. Even though this method works very accurately, it has a disadvantage. If the inverter current fails to reach the current limit at the end of the charging cycle, the algorithm will underestimate the voltage and may not be capable of ending the charge event accurately. This would force the RCC to stop the charging process based on backup sensors.

The proposed method is similar to the previously discussed software-based approach but instead it uses discrete hardware operational amplifier circuits and integrators. The input current is measured using a current transformer which outputs a voltage proportional to the measured current with the addition of a load resistor. This sensor is already included for the peak current

mode control. As it is discussed in [2], the current signal is used for slope compensation to preserve converter stability at high duty cycles. This current measurement is the foundation for the proposed method.

III. Proposed Method Circuit Simulation

A SPICE simulation of the hardware portion of the proposed method was performed in order to validate the idea. The schematic diagram used in the simulation is shown in Fig. 1. The current source labeled CT simulates the current transformer output. This output current flows through the load resistor R_L which generates a proportional voltage as a function of the input current (I_{IN}). The operational amplifier U1 converts the voltage to a proportional current which is scaled by the resistor R_1. At the same time, the current pulses that flow through R_1 charge the capacitor labeled C_1. The voltage across this capacitor is proportional to the voltage present at the output capacitor bank.

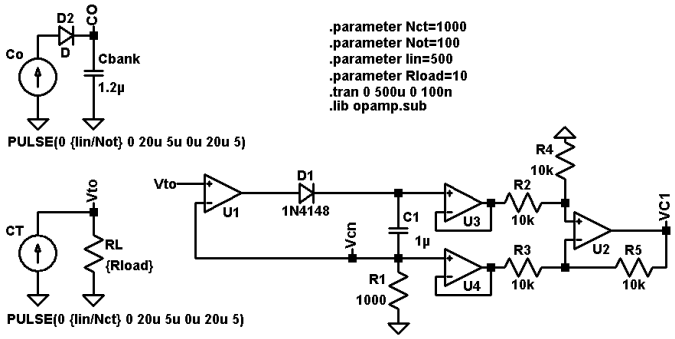

Fig. 1. End of charge detection circuit schematic diagram.

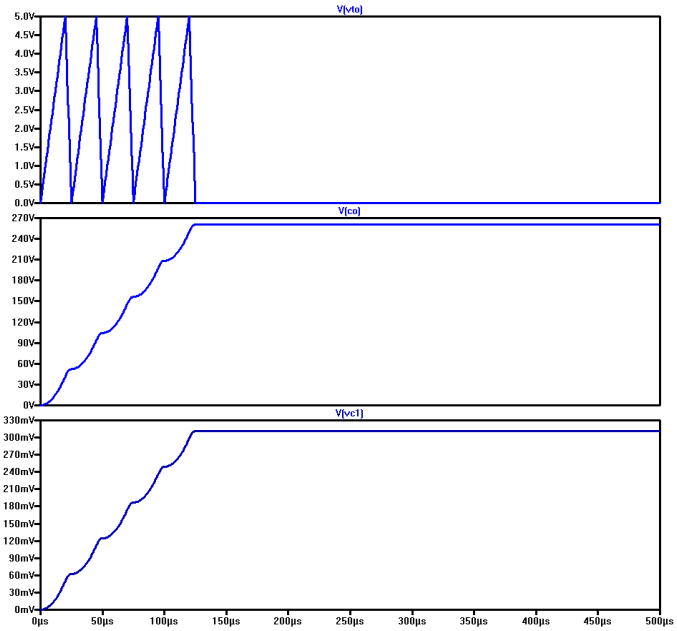

Fig. 2. Comparison between the initial breakdown IV curve and the breakdown IV curve after performing the resistive and insductive switching tests.

Ideally, the DSC would use an ADC channel to read the voltage across C_1 to determine when to stop the charging process. Reading differential voltages is not a feature that many microcontrollers and digital signal controllers have. For this reason, the voltage across the capacitor was buffered by U3 and U4 to prevent loading and a differential amplifier formed by U2, R_2, R_3, R_4, and R_5 was used to convert the differential voltage to a single ended voltage. If needed, a voltage gain can be obtained from this amplifier by selecting the appropriate resistor values. The expression that relates the voltage across C_1 and the output capacitor bank voltage is given by (1). A derivation of this equation is shown in the next section.

$$V_{CO} = k \cdot V_{C1} \tag{1}$$

Where,

V_{CO} is the output capacitor bank voltage,
V_{C1} is the voltage across C_1,
and

$$k = \frac{N \cdot R_1 \cdot C_1}{C_O \cdot R_L \cdot N_{OT}} \tag{2}$$

The derivation of (2) is shown in section IV. Utilizing the values given in the circuit schematic diagram shown in Fig. 1, the constant k is calculated to be 833.34. By taking the voltage across the capacitor C_1 (312 mV) and multiplying it by this constant, the capacitor bank voltage is calculated to be 260 V. This voltage corresponds to the output capacitor bank voltage calculated by the simulation software.

IV. Mathematical Derivation

With the use of basic equations derived from the circuit's known behavior the value of the constant k can be derived. A series of equations derived by performing simple circuit analysis are shown in (3)-(6). V_{OT} is the output voltage generated by the current transformer with a turns ratio N through a load resistor RL with and an input current $I_{IN}(t)$. N_{OT} is the turns ratio of the output power transformer, I_O is the output current, and I_{C1} is the current flowing through the capacitor C_1.

$$V_{OT}(t) = \frac{I_{IN}(t) \cdot R_L}{N} \tag{3}$$

$$I_{C_1}(t) = \frac{V_{OT}(t)}{R_1} \tag{4}$$

$$I_{IN}(t) = N_{OT} \cdot I_O(t) \tag{5}$$

$$I_{C_1}(t) = \frac{I_{IN}(t) \cdot R_L}{N \cdot R_1} \tag{6}$$

Using (1) and the relationship between the voltage and current in a capacitor, (7) is formed. By substituting $I_{C1}(t)$ in (7) with (6) yields (8).

$$\frac{1}{C_O} \cdot \int I_O(t)dt = k \cdot \frac{1}{C_1} \cdot \int I_{C_1}(t)dt \tag{7}$$

$$\frac{1}{C_O}\cdot\int I_O(t)dt = k\cdot\frac{1}{C_1}\cdot\int\frac{I_{IN}(t)\cdot R_L}{N\cdot R_1}dt \quad (8)$$

$$\frac{1}{C_O}\cdot\int I_O(t)dt = \frac{k\cdot R_L}{N\cdot R_1\cdot C_1}\cdot\int I_{IN}(t)dt \quad (9)$$

$$\frac{1}{C_O}\cdot\int I_O(t)dt = \frac{k\cdot R_L\cdot N_{OT}}{N\cdot R_1\cdot C_1}\cdot\int I_O(t)dt \quad (10)$$

$$\frac{1}{C_O} = \frac{k\cdot R_L\cdot N_{OT}}{N\cdot R_1\cdot C_1} \quad (11)$$

After (8) is derived, further work can be performed to obtain a simpler solution. All the terms that are not a function of t can be pulled out of the integral leaving only $I_{IN}(t)$ inside. $I_{IN}(t)$ is replaced by (5) and N_{OT} is pulled out of the integral as shown in (10). At this point, both sides of the equation are being multiplied by the integral of $I_O(t)$ and hence it's dropped resulting in (11). Solving for the constant k yields (2).

V. Rapid Capacitor Charger Hardware

Previously, a number of rapid capacitor chargers were developed and extensively discussed in the scientific literature [6]. However, a new hardware platform was developed to test the new end-of-charge detection mechanism. Fig. 3 shows the new hardware. Before construction of the new hardware platform the circuit was tested outside of the capacitor charger with bench-top equipment. A function generator was used to simulate the output of the current transformer. Fig. 4 shows the input triangle wave and the voltage across the capacitor C_1. As it can be seen in this figure, the hardware-based circuit works identically to the simulated circuit. This shows that the idea is a viable option to indirectly measure the capacitor bank voltage.

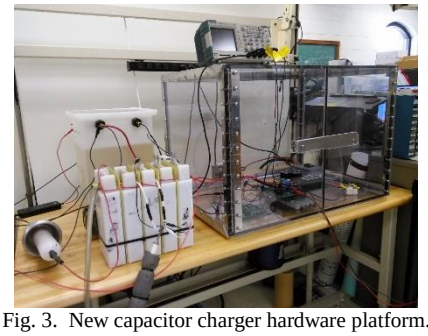

Fig. 3. New capacitor charger hardware platform.

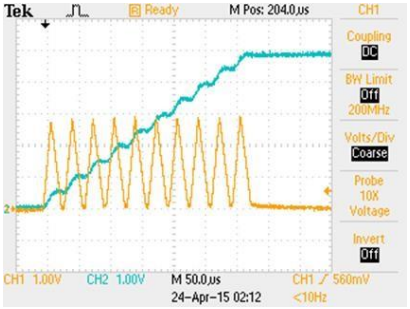

Fig. 4. Testing of the proposed hardware-based method.

VI. Conclusions and Future Work

A new hardware-based method was presented in this paper. The feasibility of this method was studied with the use of simulations and prototype hardware. Detailed derivations to indirectly calculate the output capacitor bank voltage were shown and an example was discussed. The results obtained from the prototype hardware used in the proposed approach were shown to behave identically as the simulated circuit. This proves that the proposed method is a viable alternative to accurately detect the end of charge voltage.

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