Design of inductive pulsed current generator based on solid-state Marx adder

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***Abstract*—This paper presents a novel design of a pulsed current generator using an inductor as energy-storage component based on solid-state Marx adder, in which the structure of the basic unit in solid-state Marx adders is changed. After two times of energy conversion, this current generator produces pulses with a good flat, a fast-rising edge and a fast-falling edge, regardless of the impact that the resistive load changes in a certain range. The design principles are described and the control method is also given. The feasibility of the design was validated in experiments.**

Keywords—solid-state Marx adder; inductor; pulsed current generator; resistive load

I. INTRODUCTION

The circuit structures of solid-state Marx adder have been mature now, which can produce unipolar pulses or polar pulses as behavior of single pulse or repetition frequency [1]. Nevertheless few studies can be found about pulse current generators, especially using an inductive storage to constitute circuits. Compared to high-voltage generators, pulsed current generators with high pulsed voltage can be used in many applications of pulsed power techniques, like the driver of accelerator, surface treatment of materials, ion source and so on.

Most of the pulsed current supplies are formed by pulsed voltage sources and series resistors, whose output current will be effected by varying loads. To produce current of fixed value, it is requisite that a voltage source which can quickly and dynamically adjust output voltage. In this way it brings great difficulties to the design of the circuits and control system.

It is quite obvious that one current supply containing an inductor as energy storage component will be a better choice, because the inductive current cannot leap immediately even though the loads are fluctuating. Meanwhile, the circuit systems may be exposed to the risk of overvoltage caused by the inductor. So the overvoltage protection of the inductor cannot be negligible.

In this paper, an inductive pulsed current generator was designed, which can generate square current pulses with high voltage. The output current waveforms have excellent parameters. This design mainly focuses on the processes of inductance energy changing and ensures that inductive current always has a continuous path. So far, a module which can generate pulses of current 10 A and voltage 20 kV has been manufactured. In further eight modules will be connected to generate pulses of current 10 A and voltage 150 kV.

II. CIRCUIT PRINCIPLE

A. Circuit structure

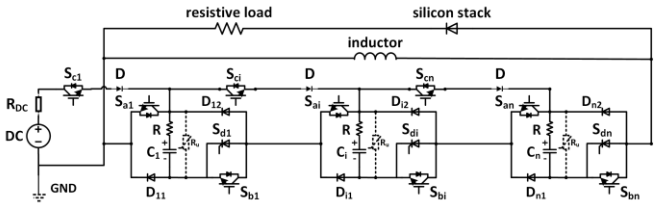

Fig. 1. Circuit structure

Fig. 1 shows the circuit structure of one module with three units of the inductive pulsed current generator. The switches in the same position of each unit are synchronous. Switches S_{ai}, S_{bi} and S_{ci} are Insulated Gate Bipolar Transistors (IGBTs). Capacitor C_i is an energy storage capacitor in unit and resistor R is the equivalent series resistor (ESR) of C_i. D, D_{i1} and D_{i2} are fast recovery epitaxial diodes (FREDs). Thyristor S_{di} is in the same position of switch S_{bi}. A resistive load, a silicon stack and an inductor are also included. Piezoresistor R_u which is used to protect capacitor C_i from overvoltage is not necessary.

A module of the pulsed current generator that can produce pulses of voltage 20 kV and current 10 A contains 24 units and each energy storage capacitor in the unit should be charged to ~1000 V. Other important parameters of the inductor, the capacitors and the silicon stack will be calculated detailedly in the following chapter discussion.

B. Circuit operating process

The pulsed current generator has four operating processes: capacitance charging, inductance charging, load discharging and load current chopping. When the different types of switches switch on, the generator will enter the corresponding process. These four processes are strictly in accordance with the order of execution.

In the stage of capacitance charging, switches S_{ai} and S_{di} in this module switch off and switches S_{ci} and S_{bi} switch on. The charging path is shown in Fig. 2. In the actual circuit, the switching charging mode is adopted for charging the energy storage capacitors. Switches S_{ci} and S_{bi} synchronously act in 2 kHz.

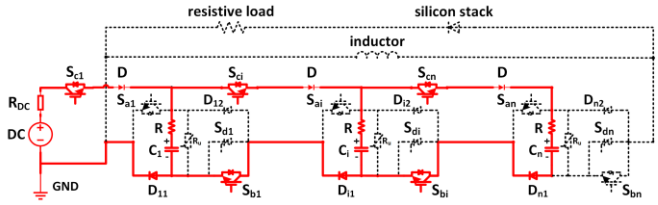

Fig. 2. Capacitance charging path

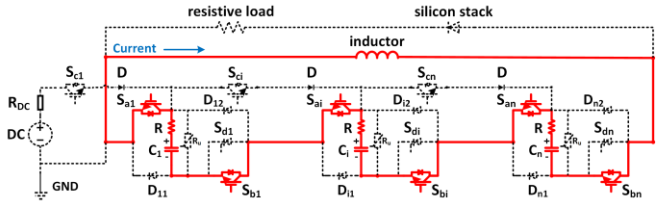

Fig. 3. Inductance charging path

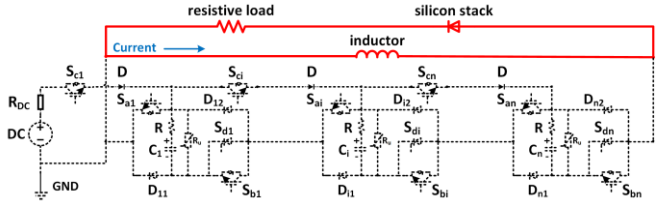

Fig. 4. Load discharging path

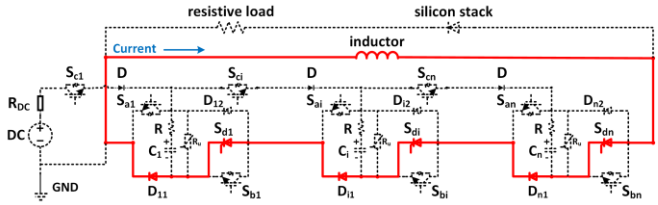

Fig. 5. Load current chopping path

When the capacitive voltage reaches the expected value, the generator will enter the next stage, inductance charging. In this stage Marx adder discharges to the inductor and the inductive current increases. Switches S_{ci} switch off, then after a short delay switches S_{ai} switch on to make all of capacitors in series. Fig. 3 presents the inductance charging path which is an overdamped RLC circuit.

Switches S_{ai} and S_{bi} switch off at the same time when the inductive current reaches the expected value. If the value of resistive load is within a certain range, all the inductive current will flow to the load. The ideal load discharging path is shown in Fig. 4. However, when the resistive load is larger than a certain value, the partial inductive current will return to the capacitors of Marx adder. This situation is expressed in the following chapter discussion.

The circuit will enter the stage of load current chopping when all the thyristors S_{di} switch on. If the ESR of all thyristors is much smaller than the resistive load, the inductive current will change to new path, shown in Fig. 5. Using thyristors can simplify the design of drivers. Compared with IGBT, the switch off signals for thyristors are not needed because the thyristors can turn off automatically when the current reduces to nearly zero [2].

III. Discussion

Some necessary parameters need to be calculated to ensure the circuit can operate as expected and to ensure the output performance can be expected. In simple terms, the inductance of the inductor affects the top drop of current pulses. The time of inductance charging determines the inductive current and the amplitude of the final output current. The interval between load discharging and load current chopping is the pulse width of the current pulse on load. Furthermore, the parameters of some types of switches will affect the output pulses. All of the above will be discussed in detail in this chapter.

A. Circuit parameter calculation

The inductance of the inductor should be determined first because the inductor is the only factor that influences the top drop of the output current pulse except the resistance of load, under the condition that the pulse width is changeless. The path of load discharging shown in Fig. 4 can be equivalent to an RL circuit with the inductive current (i_L) given by

$$i_L(t) = i_0 \cdot \exp\left[-\left(R_{load} + R_L\right)/L\right] \tag{1}$$

where t is the discharge time or pulse width, R_{load} is the load resistance, R_L is the ESR of the inductor, L is the inductance, and i_0 is the initial inductive current.

If the maximum top drop (D) and pulse width (t_w) have been demanded, L can be calculated by

$$L \geq -\frac{R_{load} + R_L}{\ln(1-D)} t_w \tag{2}$$

The inductive current is the final current produced to the load, so the charging time in the stage of inductance charging determines the amplitude of pulsed current. When IGBT switches S_{ai} and S_{bi} are switching on, the inductance charging path shown in Fig. 3 can be equivalent to an RLC circuit. The inductive current is zero at the initial time of each inductance charging. The inductive current (i_L) at different charging time (t) can be calculated by [3]

$$i_L(t) = \frac{U_0}{\omega L}\left(-\frac{R}{2L}t\right)\sin(\omega t), \omega = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \tag{3}$$

where U_0 is the initial output voltage of Marx adder. R is the sum of all series resistance in the loop, namely R_L, switching conduction impedance and all the ESR of capacitors. The output voltage of Marx adder (U_C), that equals the sum of all the capacitive voltage, decreases in the meantime. The voltage U_C can be also calculated by

$$U_C(t) = U_0\left[\frac{\alpha}{\omega}\sin(\omega t) + \cos(\omega t)\right]\exp(-\alpha t) \tag{4}$$

where U_0 and ω are the same as Eq. (3), and $\alpha = R/2L$.

Fig. 6 presents the tendency of i_L and U_C with the charging time (t) increasing. It is forbidden to reach and across the time point (t_f) where U_C reduces to zero and meanwhile i_L reaches the maximum value.

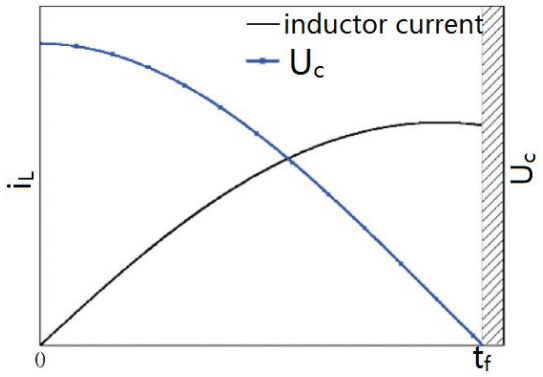

Fig. 6. The relation of i_L and U_C with charging time (t)

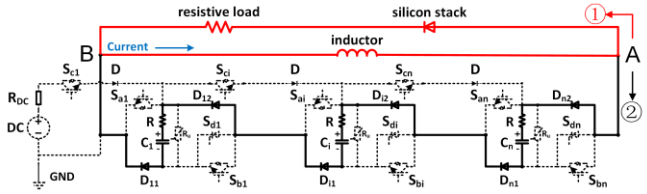

Fig. 7. Two potential paths for inductive current in load discharging

In the stage of load discharging, there are two potential paths for the inductive current shown in Fig. 7. Path 1 includes the resistive load and silicon stack; Path 2 includes diodes D_{i1}, D_{i2} and storage capacitors. Setting point B zero potential reference, the voltage at point A changes from the output voltage of Marx adder (U_C) to the inductive voltage ($U_L = R_{load} \cdot i_L$) during the operation process is switching from inductance charging to load discharging. All the inductive current will pass the Path 1 under the condition that the final potential at point A, namely U_L, is lower than the voltage of all the capacitors in series, which equals U_C. This condition is described as

$$U_C(t_c) \geq U_L = R_{load} i_L(t_c) \tag{5}$$

where t_c is the time that Marx adder charges the inductor.

The inductive current will pass both of Path 1 and Path 2 if the load resistance or the output current is too huge. The potential at point A will be limited at U_C by the capacitors in series. In this situation, the current on load (i_{load}) and the current returning to Marx adder (i_{fb}) are presented as

$$\begin{aligned} i_{load} &= \frac{i_L(t_c) R_c + U_C(t_c)}{R_{load} + R_c} \\ i_{fb} &= \frac{i_L(t_c) R_{load} - U_C(t_c)}{R_{load} + R_c} \end{aligned} \tag{6}$$

where R_C is the sum of all the ESR of capacitors. Because R_C is small enough to ignore, Eq. (6) can be simplified to

$$\begin{aligned} i_{load} &= U_C(t_c)/R_{load} \\ i_{fb} &= i_L(t_c) - U_C(t_c)/R_{load} \end{aligned} \tag{7}$$

The pulse width of the current pulse released to load depends on the interval between two adjacent processes, load discharging and load current chopping.

In the last stage of the processes, all the thyristors S_{di} switch on to provide a low-impedance path for the inductive current. If the loop impedance is much less than the load, there will be little current leaking to the load. The turn-on time of thyristors plays a decisive role in the speed of the falling edge of current pulse.

B. Control sequence

Each operating process corresponds to different groups of switches switching on. The duration of each process will determine the parameters of the final current pulse on the resistive load. Fig. 8 describes the actions of all the switches and some waveforms of key parameters. In this figure, high level means that the switch is switching on or that the vector of the waveform is positive. If not, it means that the switch is switching off or that the vector of the waveform is negative.

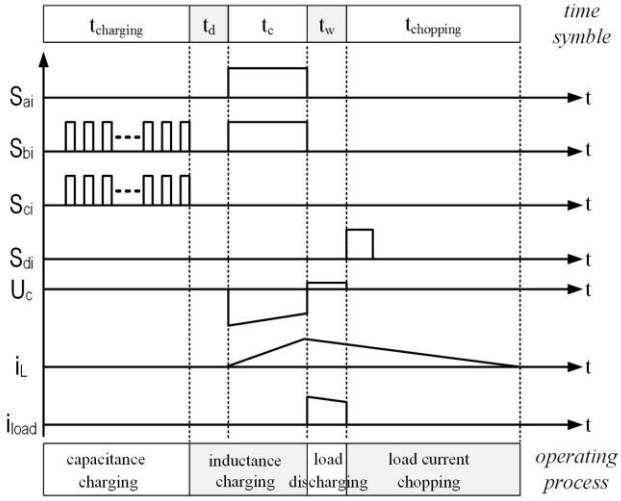

Fig. 8. Switches acting and waveforms of important parameters during each operating process

In Fig. 8, $t_{charging}$ is the time that low-voltage DC power charges the storage capacitors, which needs to last until the capacitive voltage has reach expected value. The delay time (t_d) between two processes of capacitance charging and inductance charging is set to protect the low-voltage DC power. Symbol t_c is the time that Marx adder charges the inductor, which determines the inductive current. Symbol t_w is the internal between two processes of load discharging and load current chopping, which equals the pulse width of current pulse released to the load. To obtain pulses with less top drop, it is estimated for t_w to be limited within 20 μs. Load current chopping is a long-running process because the impedance is generally small in the RL circuit. Thus $t_{chopping}$ is a millisecond time in usual.

Some necessary insulation and isolation measures have been taken in the control system to protect the low-voltage logic devices [4].

IV. EXPERIMENT RESULTS

The module which can produce pulses of 20 kV and 10 A contains series equivalent capacitance 557 nF and an inductor 350 mH. By measuring, all the ESR of capacitors and ESR of inductor are 216.8 Ω in total. All waveforms were acquired under the condition that Marx adder produced 20 kV voltage.

Fig. 9 presents a complete discharging process. Throughout, the inductive current is continuous so the entire circuit has no risk of overvoltage. Because of the distributed capacitance of the silicon stack, there is a spike pulse in the resistive load current when Marx adder generates a falling edge.

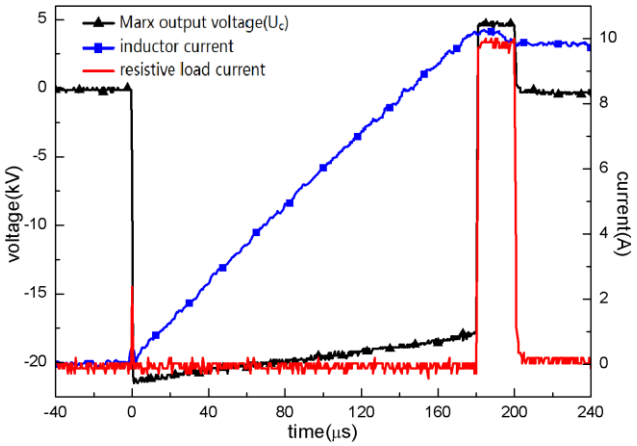

Fig. 9. A typical waveform of the current generator

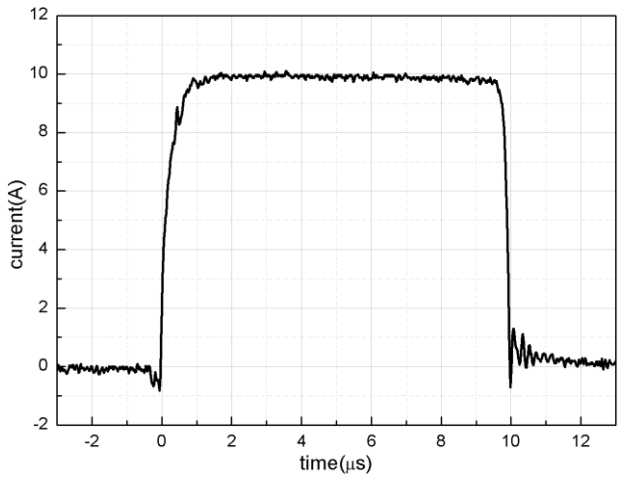

Fig. 10. Waveform of current pulse of 10 A and 10 μs on 1.2 kΩ resistor

A typical output current pulse on the resistive load produced by the current generator is presented in Fig. 10. The amplitude of current pulse on 1.2 kΩ load is 10 A instead of 16.7 A and the pulse width is 10 μs. The current pulse with a good flat (top drop < 5%) has rapid rising edge ~650 ns and falling edge ~250 ns.

By adjusting the time that Marx adder charges the inductor, the amplitude of current pulse on resistive load can be simply changed. Fig. 11 gives five waveforms of current pulses with different amplitudes on 1 kΩ resistive load. In the actual circuit, the amplitude of current pulse can be calculated by

$$i_L(t) = 25.5 \cdot \exp(-310t) \cdot \sin(2243.6t) \qquad (8)$$

where i_L is the amplitude of current pulse and t is the time that Marx adder charges the inductor.

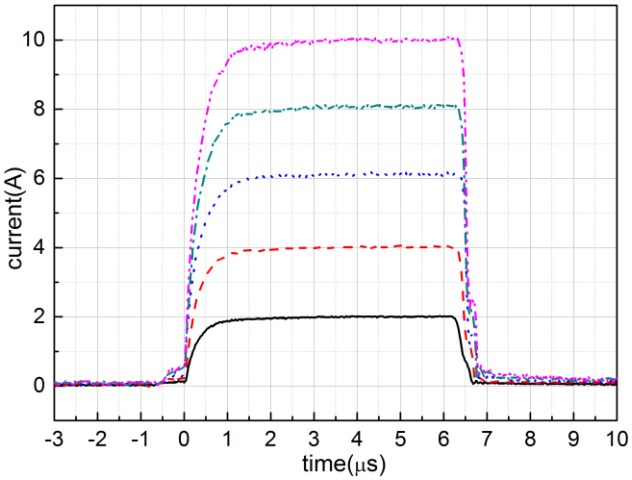

Fig. 11. Several waveforms of current pulses with different amplitudes on 1 kΩ resistive load

As a result of the existence of distributed capacitance in the generator, the partial inductive current will be provided to the distributed capacitance for reverse charge when the inductive current begins to flow to the resistive load. Therefore, the rising edge of current pulse on load becomes slower, especially when the output current becomes smaller.

V. CONCLUSION

In this paper, a design of inductive pulsed current generator was expounded. Its circuit principle and control sequence were described. A module was manufactured which can produce current pulses with maximum 10 A and maximum 20 kV on resistive loads in a certain range. The circuit ensures the inductive current always has a continuous path, so the system can operate safely. The inductive pulsed current generator has the following advantages. Composed of solid-state devices, it can be controlled by low-voltage logic devices through isolated drivers. The parameters of the output pulses can be easily regulated by changing the switching time. The generator can produce square pulsed current with high voltage to drive large resistive loads at kilohm scale. There is no risk of overvoltage because the output voltage can be limited under the output voltage of Marx adder. Besides, several of the same module can be cascaded to provide larger current and higher voltage for driving larger resistive loads. In the future plan, eight modules will be connected to generate pulses of current 10 A and voltage 150 kV.

ACKNOWLEDGEMENT

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