TCT measurements of HV-CMOS test structures irradiated with neutrons

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E-TCT measurements with HVCMOS structures from 3 different foundries made on different substrate resistivities:

1. **AMS**: $10 \, \Omega \text{cm}$ and $20 \, \Omega \text{cm}$

2. **X-FAB**: $100 \, \Omega \text{cm}$

3. **LFoundry**: $2000 \, \Omega \text{cm}$

All devices are made on **p-type** substrates

These structures are investigated as candidates for tracking detectors at HL-LHC
E-TCT setup:

Detector connection scheme:

Passive devices (no amplifier in the pixel):
- observe induced current pulses on collecting electrode on the scope
- collected charge: integral of the pulse in 25 ns
AMS: 10 $\Omega$cm, 20 $\Omega$cm

CCPDv2 (HV2FEI4) chip, AMS 0.18 $\mu$m process:

→ active device: output of the amp in the n-well observed on the scope
  
  • substrate resistivity 10 $\Omega$cm
  • max bias 60 V

CHESS1 chip, AMS 0.35 $\mu$m process:

→ passive device
  
  • substrate resistivity 20 $\Omega$cm
  • max bias 120 V

Back plane not processed

→ bias connected from the top of the chip

More detail:
I. Perić et al., NIMA582 (2007) 876-885
I. Perić et al., NIMA765 (2014) 172-176
I. Peric et al., 2015 JINST 10 C05021.
**LFoundry: 2000 Ωcm**

- 150nm CMOS
- 2 kΩcm p-type bulk
- HV process, max bias > 100 V
- Thinning and back side metallization possible

More detail:
- Piotr RYMASZEWSKI et al., *Prototype active silicon sensor in LFoundry 150nm HV/HR-CMOS technology for ATLAS Inner Detector Upgrade* (TWEPP 2015), **2016 JINST 11 C02045**
  [https://indico.cern.ch/event/357738/session/9/contribution/200](https://indico.cern.ch/event/357738/session/9/contribution/200)

**CCPDLF_VB chip**

Two versions:

- without back side (BP) metallization  
  → substrate bias from top
- with BP  
  → substrate bias from the back plane

Measurements done with structures **A** and **F** on **CCPDLF_VB** chip  
→ see slides from F. Hügging from this morning
**X-FAB: 100 Ωcm**

- X-FAB Trench SOI 0.18 um
- p-type bulk, 100 Ωcm
- max bias 300 V
- no back side processing (bias from TOP)

More detail:
- S. Fernandez et al., *Charge Collection Properties of a Depleted Monolithic Active Pixel Sensor using a HV-SOI process* (TWEPP 2015), *JINST* 11 C0106
  [https://indico.cern.ch/event/357738/session/9/contribution/3](https://indico.cern.ch/event/357738/session/9/contribution/3)
- slides of M. Backhaus from this morning session

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**XTB02 chip**

![Diagram of XTB02 chip]

- Buried oxide
- Laser Beam direction
E-TCT, charge collection profile, AMS (20 Ωcm)

Fluence steps: 2e14, 5e14, 1e15, 2e15, 5e15, 1e16

- charge collection width increases with fluence up to ~ 2e15 n/cm²
  ➔ concentration of initial acceptors falls with irradiation faster than new acceptors are introduced ➔ space charge concentration falls
- charge collection width falls with fluences above ~ 2e15 n/cm²
  ➔ initial acceptor removal finished, space charge concentration increases with irradiation
- at 1e16 charge collection region still larger than before irradiation
  ➔ similar behaviour also in CCPDv2 chip (10 Ohm-cm)
E-TCT, charge collection profiles, Lfoundry, X-FAB

Irradiated up to $1e15$ n/cm$^2$

**X-FAB (100 Ohm-cm)**

- Large increase of charge collection width after $1e14$ and $5e14$
  - $\Rightarrow$ effective acceptor removal in X-FAB

**LFoundry (2000 Ohm-cm)**

- Charge collection width doesn’t increase with irradiation
  - $\Rightarrow$ these measurements show no effective acceptor removal effect in LFoundry
  - $\Rightarrow$ some difference between Back Plane and no Back Plane samples at highest fluence
Charge profile width vs bias voltage

Fit: \[ \text{Width}(V_{\text{bias}}) = w_0 + \sqrt{\frac{2\varepsilon_0}{e_0 N_{\text{eff}}}} V_{\text{bias}} \]

- \( w_0 \) and \( N_{\text{eff}} \) free parameters
- works for AMS and LFoundry
- X-FAB: can’t fit with \( \sqrt{V_{\text{bias}}} \)
  - estimate \( N_{\text{eff}} \) from width at \( \sim 100 \text{ V} \)
\( N_{\text{ef}} \) vs fluence

AMS and X-FAB:

- acceptor removal

\[
N_{\text{eff}} = N_{\text{eff}0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g \cdot \Phi_{eq}
\]

Radiation introduced deep acceptors: \( g \sim 0.02 \text{ cm}^{-1} \)

\( N_c \cdot N_{\text{eff}0} \) and \( c \) free parameters, 
\( g \) fixed to 0.02

LFoundry: no removal (\( N_c \sim 0 \)), fit:

\[
N_{\text{eff}} = N_{\text{eff}0} + g \cdot \Phi_{eq}
\]

\( N_{\text{eff}0} \) and \( g \) free

G. Kramberger et al., submitted to JINST
I. Mandić et al., 27th RD50 workshop

**Graphs:**
- **CHESS1**
  - \( N_c/N_{\text{eff}0} \approx 1 \)
  - \( c = 0.36 \times 10^{-14} \text{ cm}^2 \)
- **CCPDv2**
  - \( N_c/N_{\text{eff}0} \approx 1 \)
  - \( c = 0.57 \times 10^{-14} \text{ cm}^2 \)

- **CHESS**
  - \( N_c/N_{\text{eff}0} \approx 1 \)
  - \( c \sim 0.36 \times 10^{-14} \text{ cm}^2 \)
- **HV2FEI4**
  - \( N_c/N_{\text{eff}0} \sim 0.97 \)
  - \( c \sim 0.57 \times 10^{-14} \text{ cm}^2 \)
- **XFab**
  - \( N_c/N_{\text{eff}0} \sim 0.7 \)
  - \( c \sim 1.8 \times 10^{-14} \text{ cm}^2 \)
- **LF**
  - \( N_c/N_{\text{eff}0} \sim 0 \)
  - \( g_c = (0.03 \pm 0.01) \text{ cm}^{-1} \)
Effective acceptor removal

- **AMS (20 Ωcm, \(N_{A0} \sim 10^{15} \text{ cm}^{-3}\)):** \(c \sim 4 \cdot 10^{-15} \text{ cm}^{-2}\), \(N_c/N_{\text{eff0}} \sim 1\)

- **X-FAB (100 Ωcm, \(N_{A0} \sim 10^{14} \text{ cm}^{-3}\)):** \(c \sim 2 \cdot 10^{-14} \text{ cm}^{-2}\), \(N_c/N_{\text{eff0}} < 1\)

- **LFoundry (2000 Ωcm, \(N_{A0} \sim 6 \cdot 10^{12} \text{ cm}^{-3}\)), no effective acceptor removal observed in this study ➔ probably because \(N_c/N_{\text{eff0}} \ll 1\)
Charge collection profile - annealing

Measurement before and after 80 minutes at 60 C
→ 10% to 20% increase of charge collection width after annealing
Measurements with pixel array: AMS (20 Ωcm)
Bias = 120 V, all 9 pixels connected to readout, charge (25 ns)

- gaps before irradiation
- guard smaller after 2e15 (larger depleted region)
- gaps better seen again after 1e16
**LFoundry**, Structure F, all pixels read out

→ no efficiency gaps between pixels

No BP, 40 V, $\Phi = 0$

Structure F, 3x3 pixels,
125 μm x 33 μm

BP, 40 V, $\Phi = 0$

No BP, 50 V, $\Phi = 1\text{e}15$

BP, 50 V, $\Phi = 1\text{e}15$
X-FAB: 100 Ωcm

XTB02 chip

- pitch 100 μm
- n-well: 40 μm x 50 μm

⇒ “logic” (space for CMOS circuits for active device) and n-well should be at same potential
X-FAB: 100 $\Omega$cm

- 4x4 pixel array, all n-wells connected to readout

Before irradiation

After 2e14 n/cm²

- high collection under n-wells
- low charge between but E-field not zero
- large pulses with small integral
  - looks like “logic” acts as collecting electrode (AC coupled)
KDetSim simulation

• KDetSim - a ROOT based detector simulation package by G. Kramberger ([link](http://www-f9.ijs.si/~gregor/KDetSim/))
  (presented at 27th RD 50 Workshop)

• link to the software: [http://www-f9.ijs.si/~gregor/KDetSim/](http://www-f9.ijs.si/~gregor/KDetSim/)

- drift of electrons stops on the oxide surface
- bipolar pulse induced on the readout electrode $\rightarrow$ integral in 25 ns = 0
Efficiency gaps smaller at longer integration times

- Laser under n-well

25 ns time scale:
- 25 ns integration
- CCE at V bias = 200 V
- Reflections
- $\Phi = 5 \times 10^{14}$

1 μs time scale:
- 1 μs integration
- CCE at V bias = 200 V
- Tail larger when laser under logic (red curve)
- Slow electrical discharge $\rightarrow$ lateral current under the oxide layer

- Tail larger when laser under LOGIC
- Integral $\sim 0$

- Slow electrical discharge $\rightarrow$ lateral current under the oxide layer
Summary

• Edge-TCT measurements with test structures made on 3 different substrate resistivities:
  • AMS : 10 and 20 Ωcm
  • X-FAB: 100 Ωcm
  • LFoundry: 2000 Ωcm

• large increase of charge collection width after irradiation with neutrons observed in AMS and X-FAB
  • dependence of charge collection width with fluence consistent with effective acceptor removal
  • indication that acceptor removal in X-FAB less complete than in AMS

• X-FAB:
  • increase of charge collection width with bias voltage after irradiation faster than sqrt(V)
  • efficiency gaps between pixels after irradiation (at short (25 ns) integration times)
    → parasitic (temporary) charge collection by the “logic” electrode

• LFoundry: charge collection width decreases with increasing fluence
  → effective acceptor removal not observed
  → $N_{eff}$ introduction rate on high side
  • no significant charge collection gaps between pixels in the array
  • indication of effect of back plane contact at highest fluence (1e15 n/cm²)