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BRUNO KESSLER

3D sensors: status at FBK

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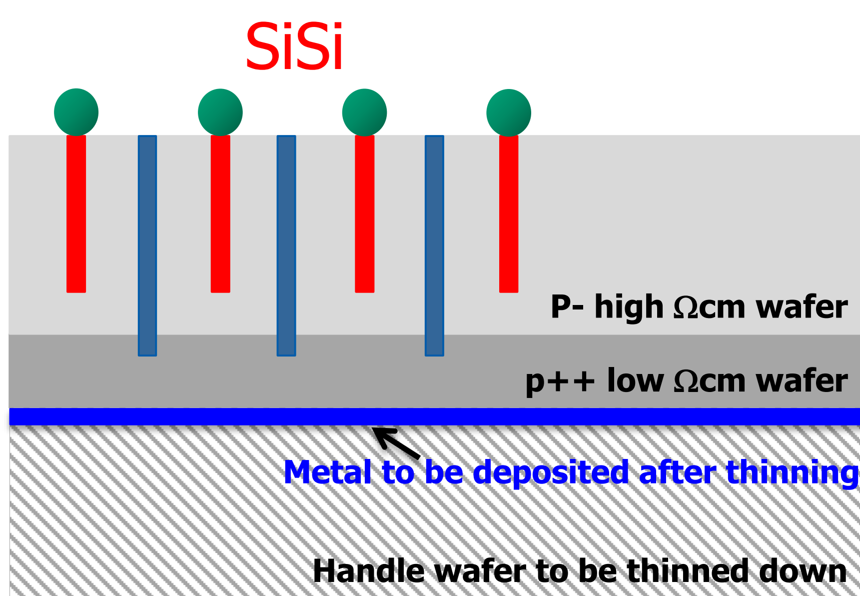
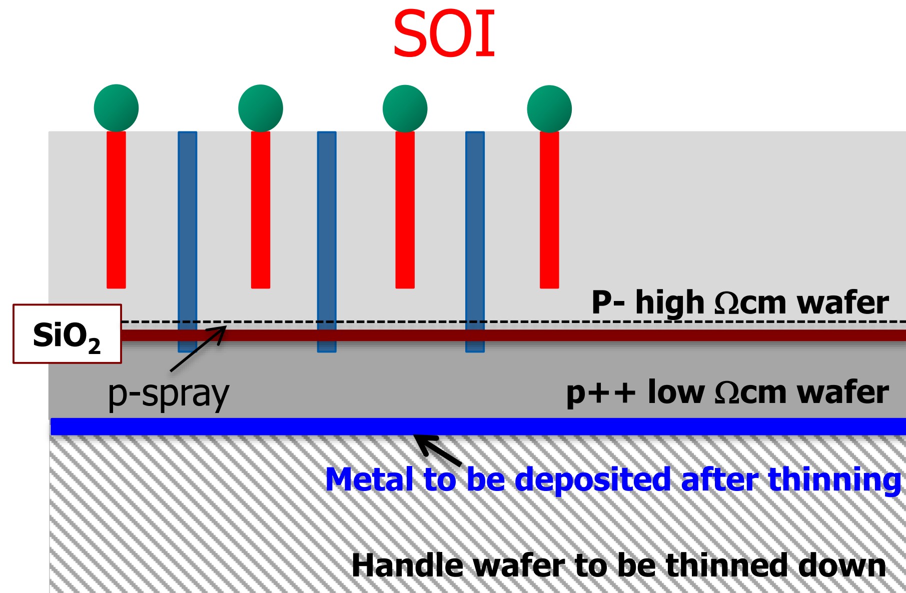
New single-side approach to 3D pixels

Double-sided process not favoured for thin sensors, especially on 6" wafers





- Thin sensors on support wafer: SiSi or SOI → Substrate qualification
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high V_{bd})
- Reduction of hole diameters to ~5 um
- Holes (at least partially) filled with poly-Si

Process Tests

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Etching test p-columns

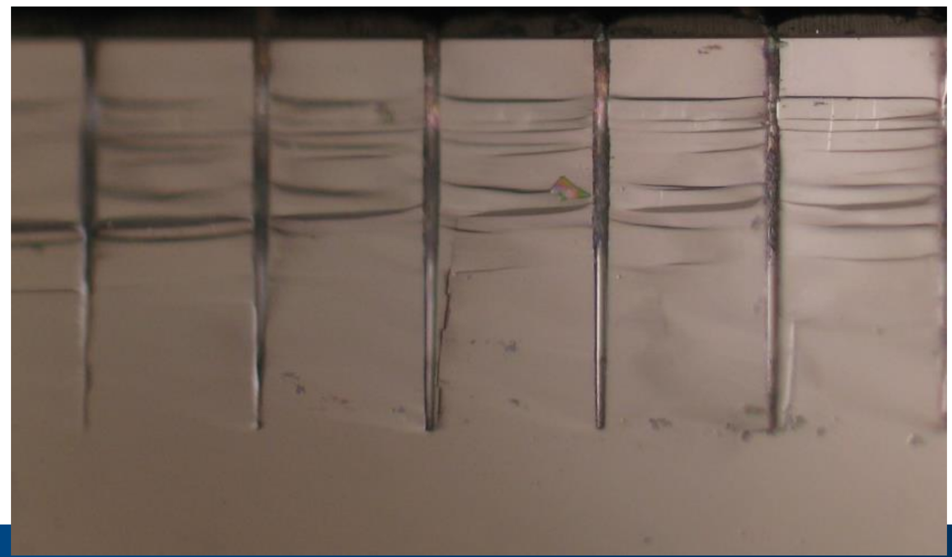
p-holes > 130 µm

70′ SDE+10′ HER

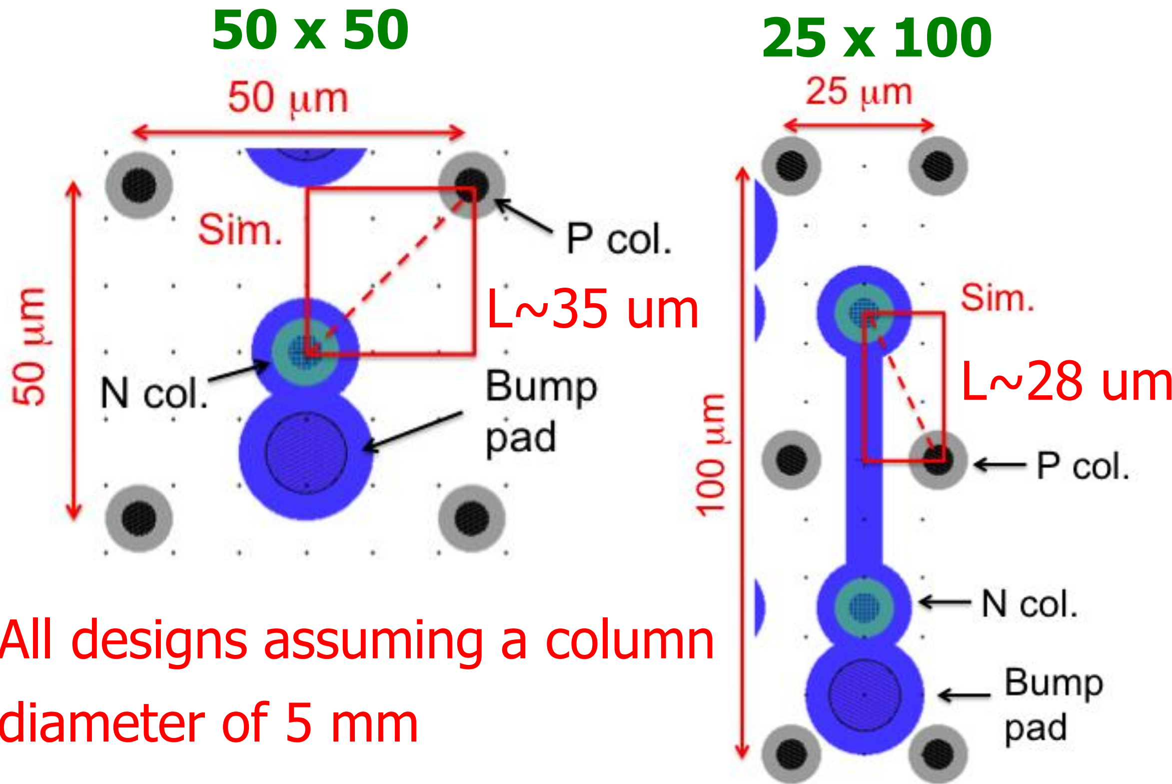
Position	depth (um)	Width at top	Width at bottom
c	**160**	5.3	4.0
t	159	5,5	2.25
f	156	5,8	3.2
dx	157	5, 5	2.9
sx	**155**	4.85	2.6

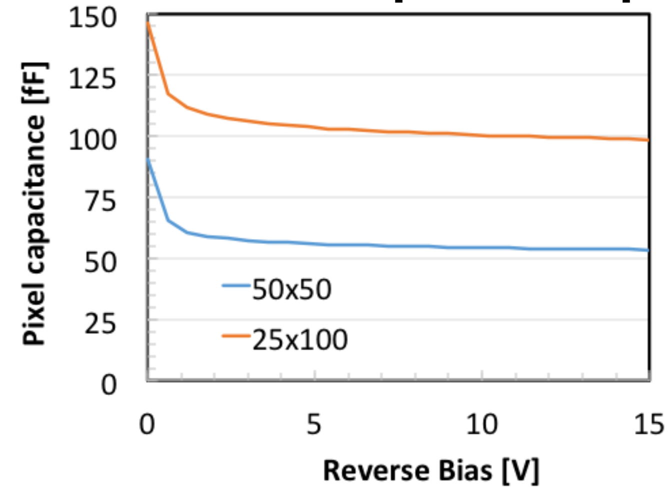
p-holes > 100 µm
43′ SDE + 10′HER

Position	depth (um)	Width at top	Width at bottom
c	**117**	4,7	3,2
t	117	4,4	3,2
f	114	4,7	3,2
Dx	115	5,2	3,2
Sx	**114**	4,8	2.4

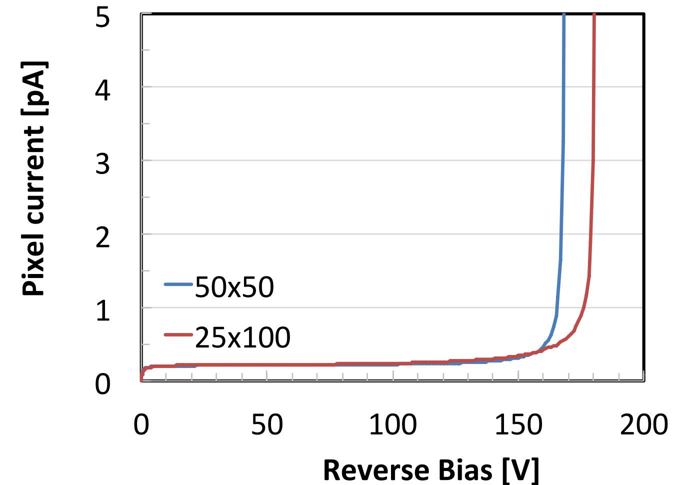


New 3D pixels: design and simulations





All designs assuming a column diameter of 5 mm



- 50x50 design safe, 25x100 is difficult … too little clearances (new ideas for bump pad to be tested)
- Capacitance compatible with RD53 specs
- Initial breakdown voltage high enough

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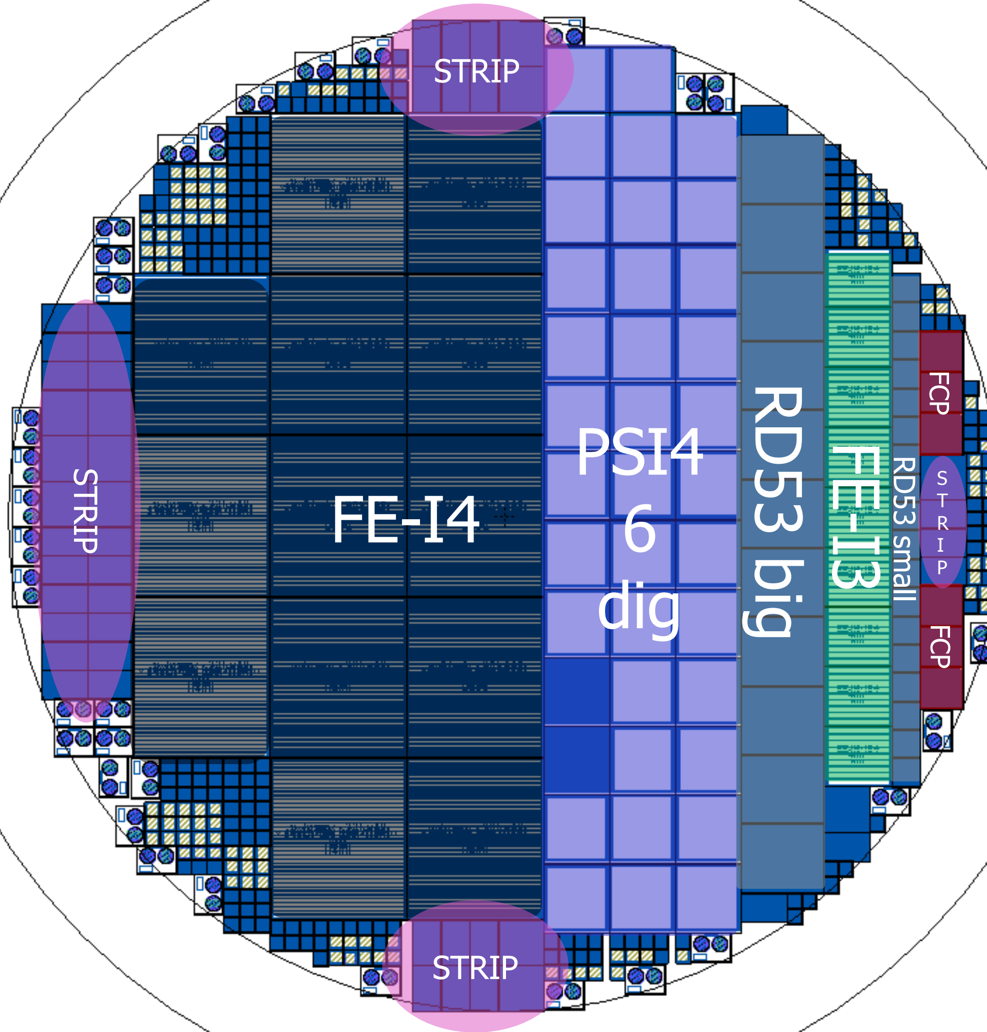
3D Pixel Wafer Layout

Final version



Many different pixel geometries and pitch variations:

- FE-I4
  - 50 x 250 (2E) std
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
  - 25 x 500 (1E)
- FE-I3
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- PSI46dig
  - 100 x 150 (2E and 3E) std
  - 50 x 50 (1E and 2E)
  - 50 x 100, 100 x 100 (2E + 4E)
  - 50 x 100, 100 X 150 (2E + 6E)
  - 25 x 100 (1E and 2E)
- FCP
  - 30 x 100 (1E)
- RD53
  - 50 x 50 (1E)
  - 25 x 100 (1E)
  - 25 x 100 (2E)

+ Test structures (strip, diodes, etc)

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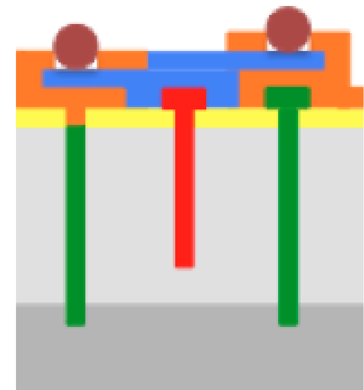
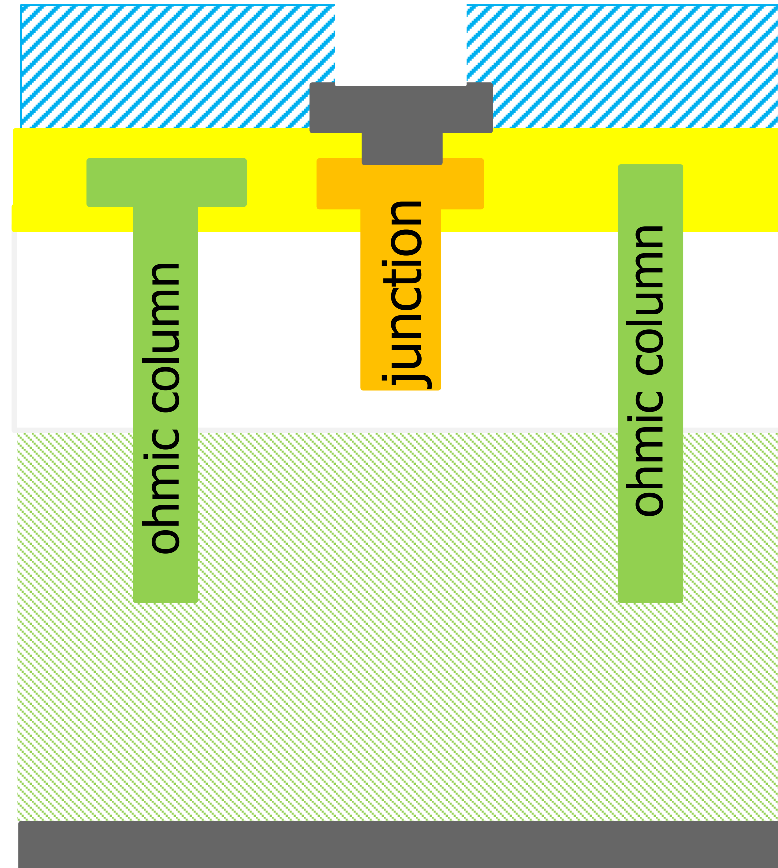
Fabrication status at FBK

- First 3D batch (15 SiSi DWB wafers) aborted at the end of October 2015 due to problem with Boron doping of ohmic columns
- Four wafers (3D_rec) completed anyway to check all relevant process steps
- A new 3D batch (10 SiSi DWB wafers) re-launched in November 2015, now being completed:
  - 3 wafers 100μm thick, p-columns with poly “cap”
  - 2 wafers 100μm thick, p-columns without poly “cap”
  - 3 wafers 130μm thick, p-columns with poly “cap”
  - 2 wafers 130μm thick, p-columns without poly “cap”
- First two wafers (with poly cap.) being tested.



Thin 3D section scheme

with poly CAP



without poly CAP

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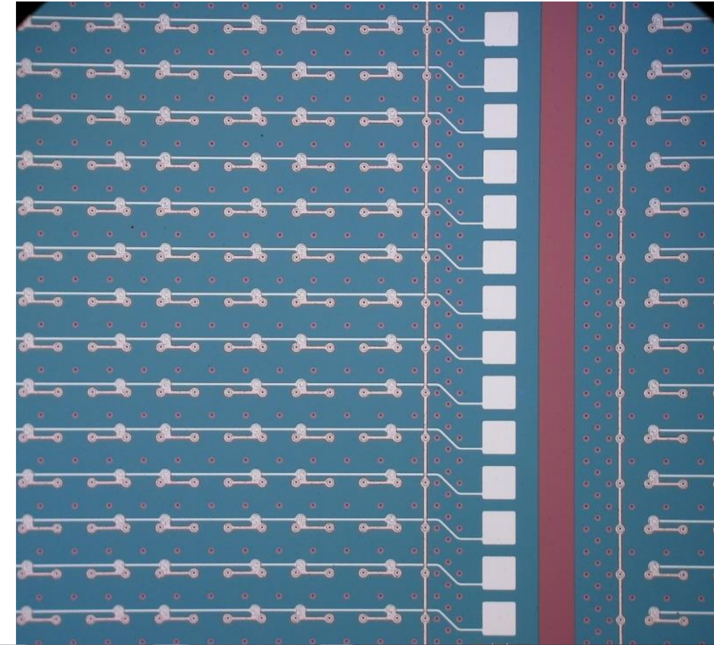
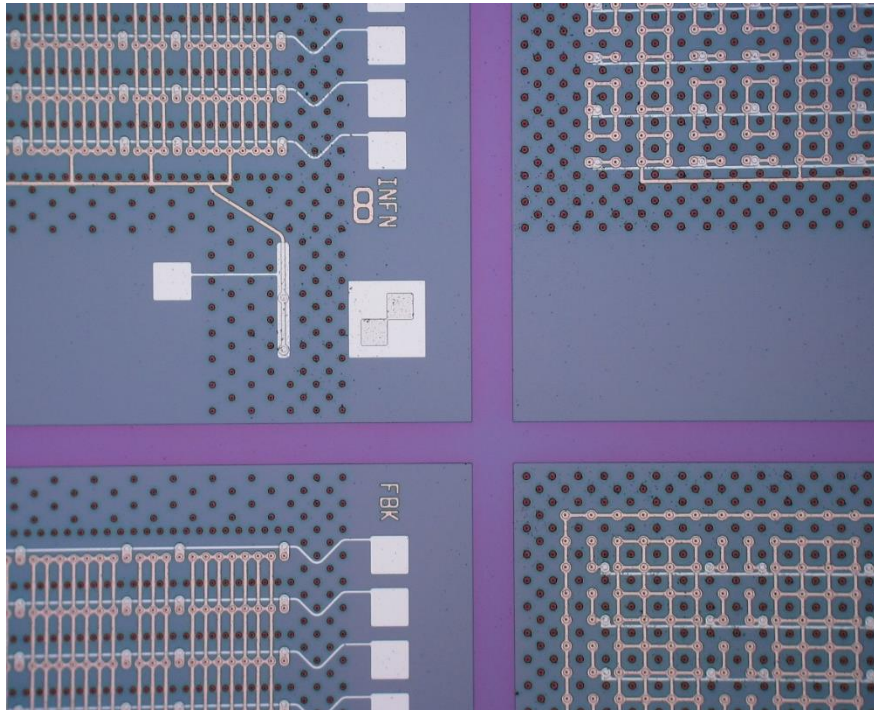
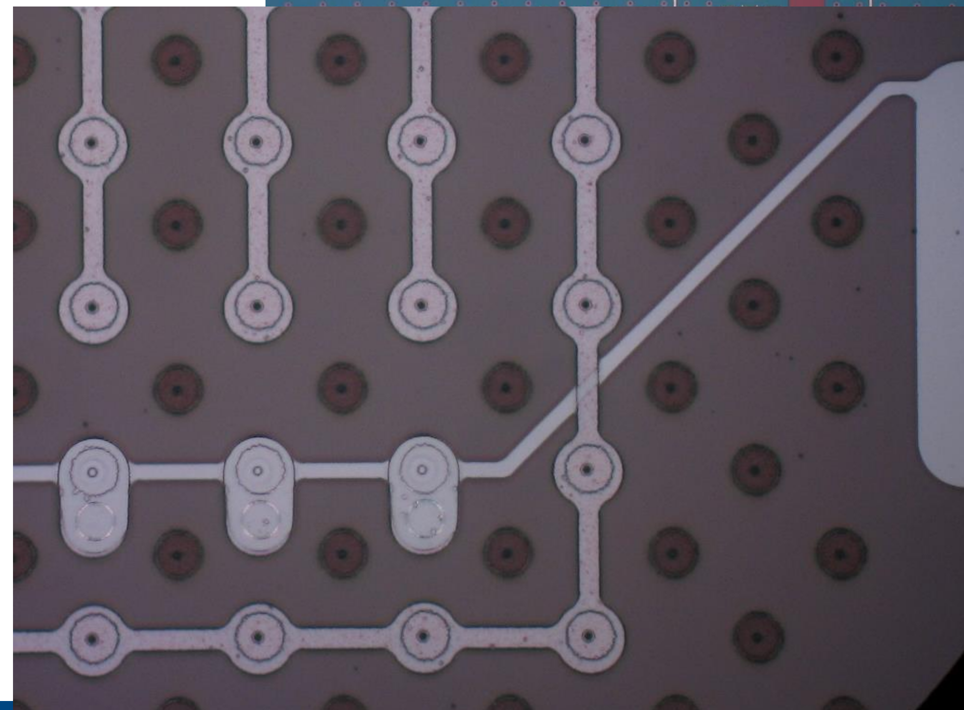
A few pictures

- Wafers with temporary metal
- Good lithographical quality







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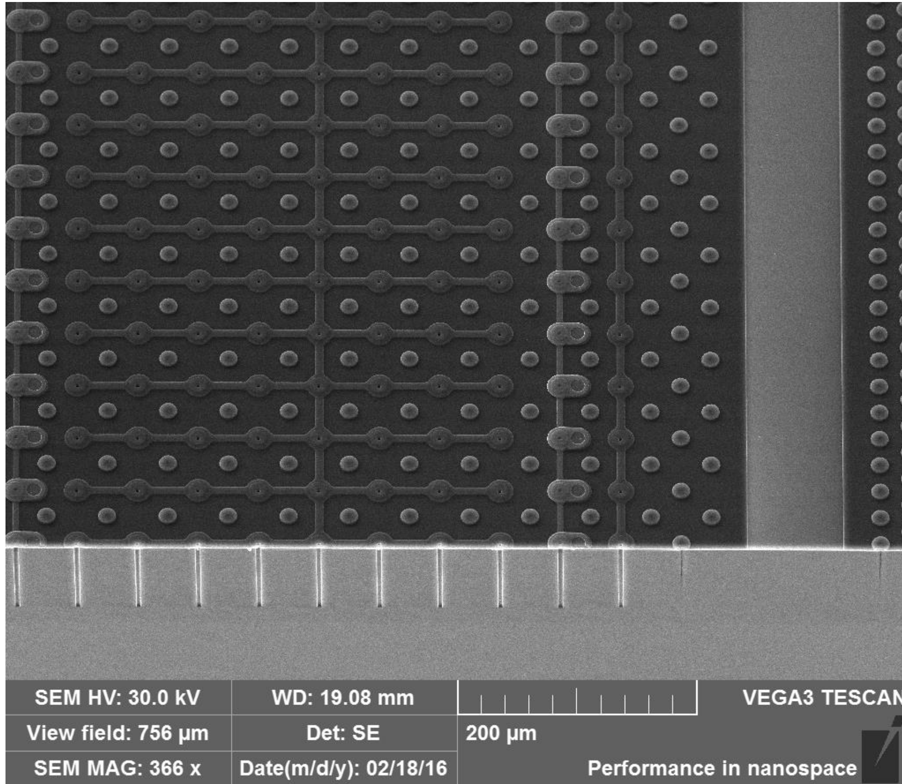
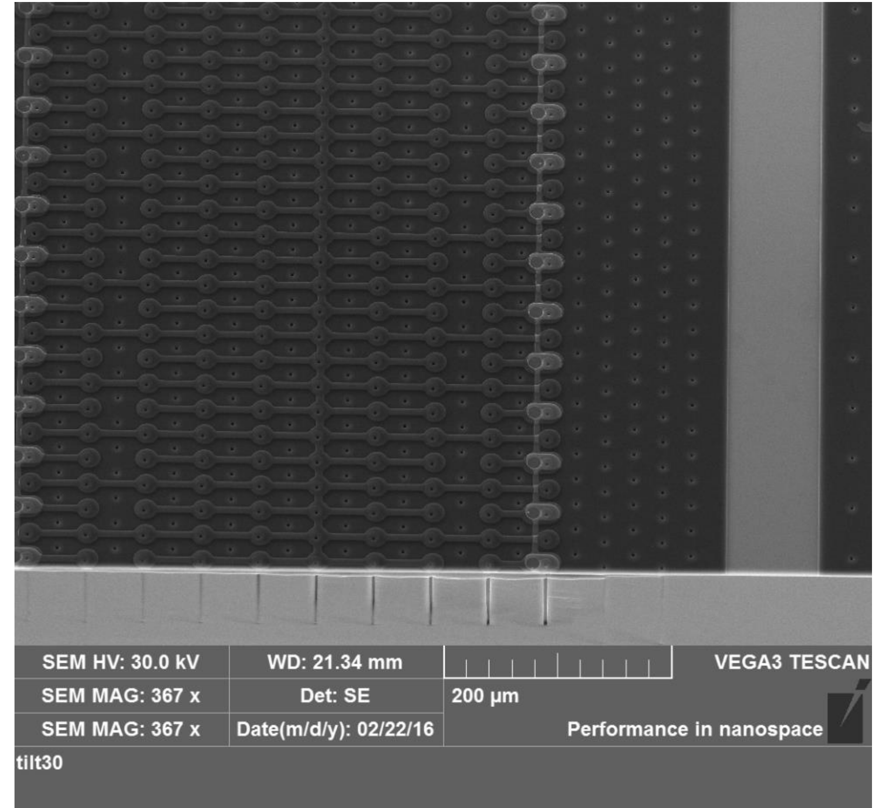
SEM Pictures (1)





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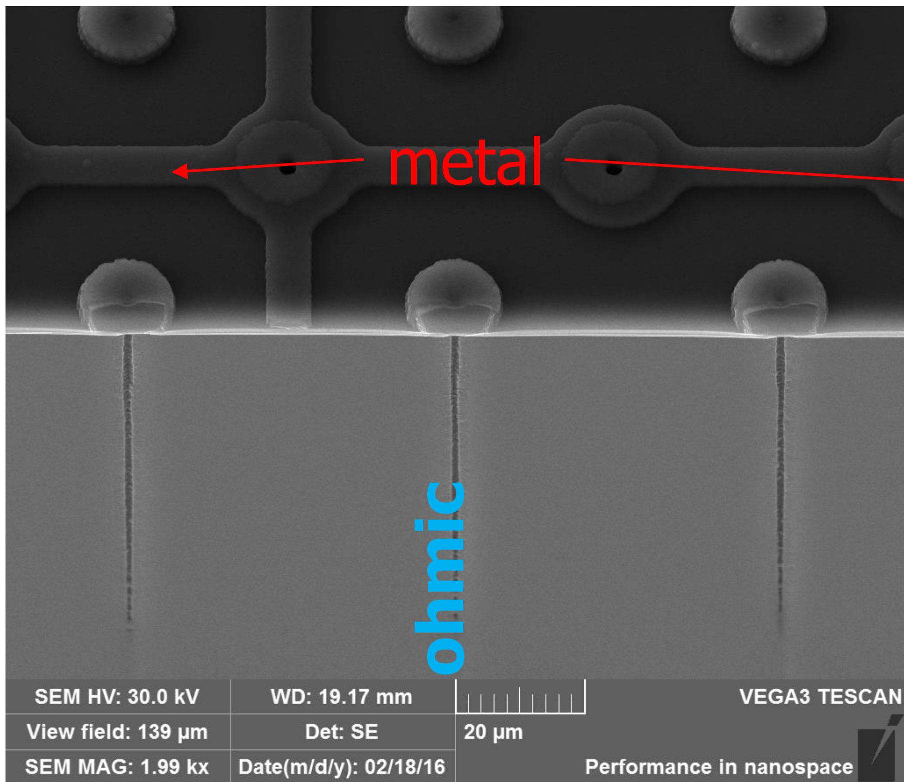
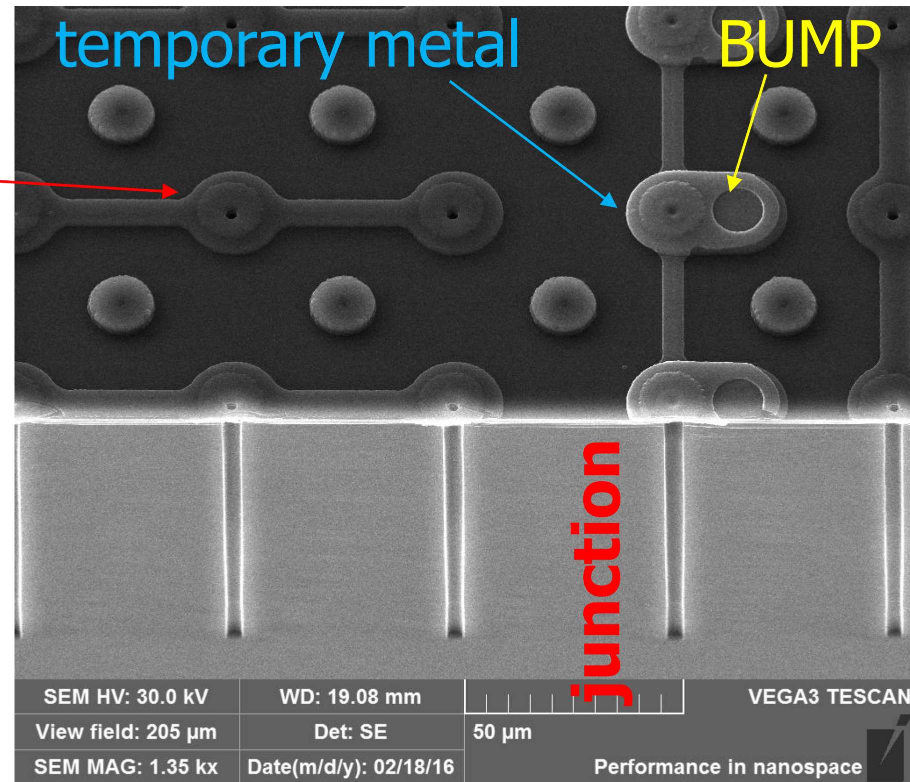
SEM Pictures (2)





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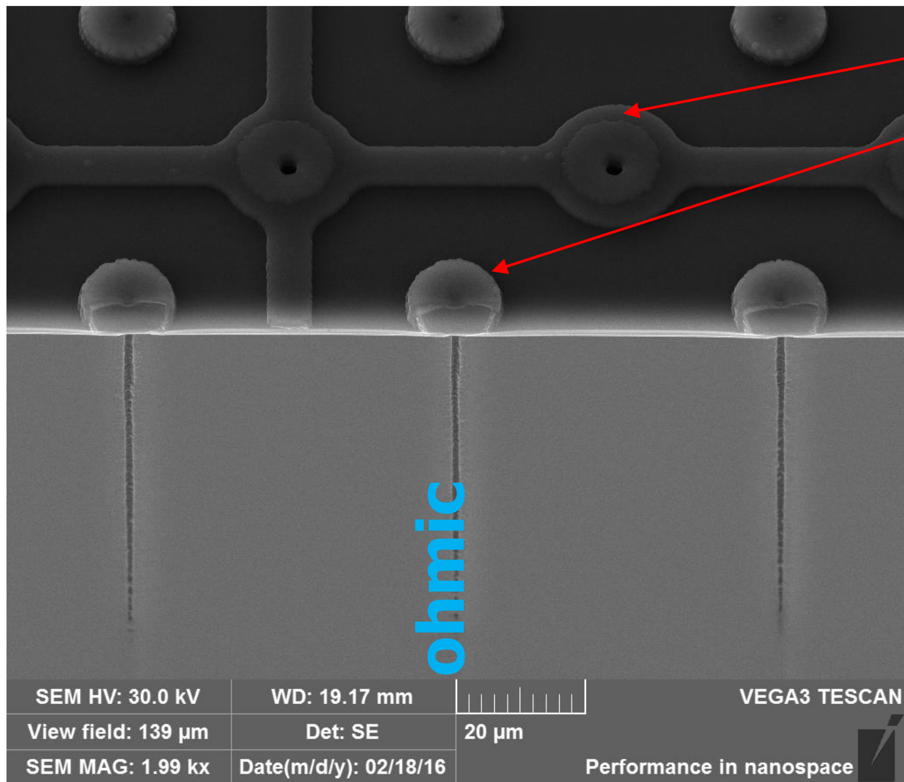
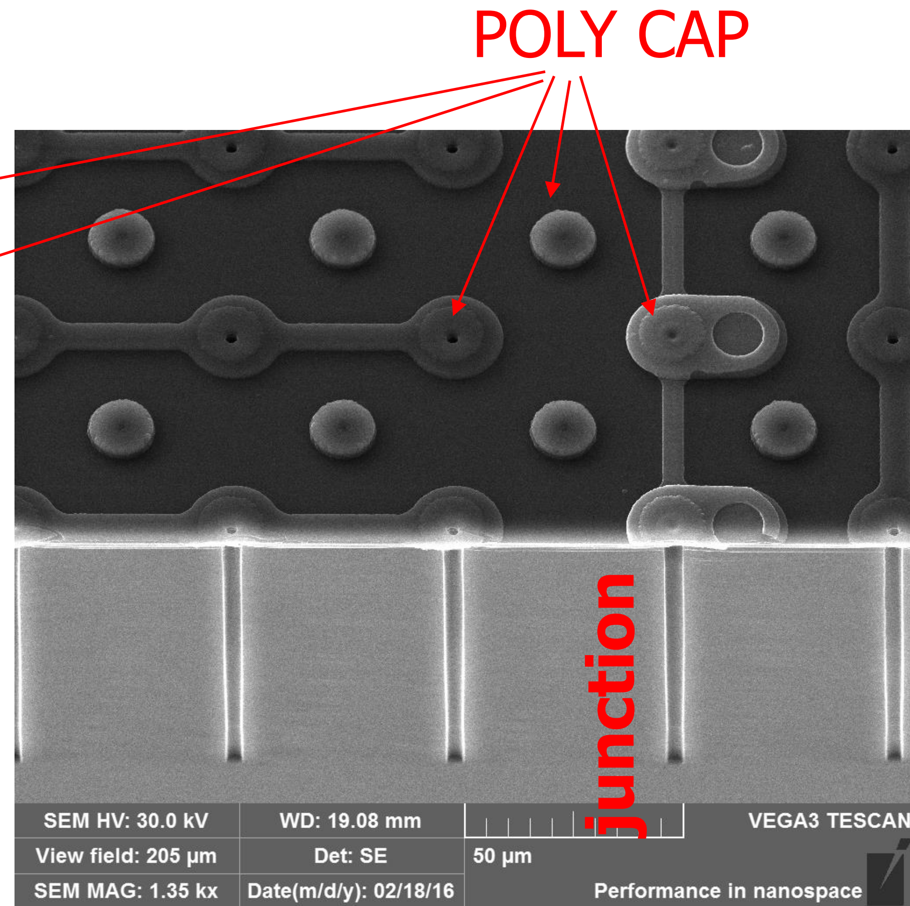
SEM Pictures (3)

POLY CAP





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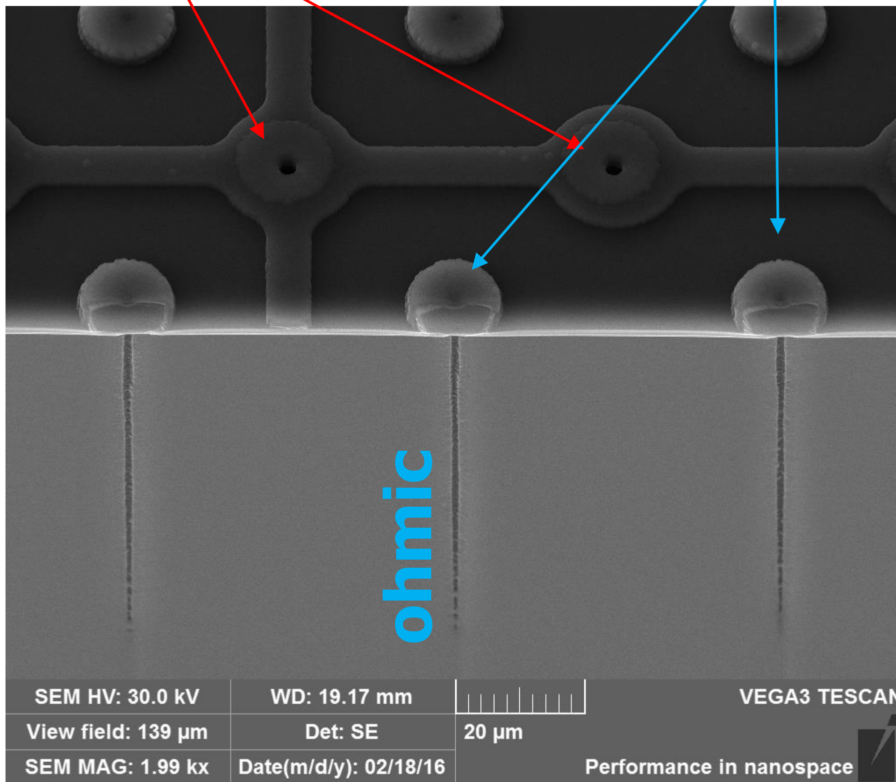
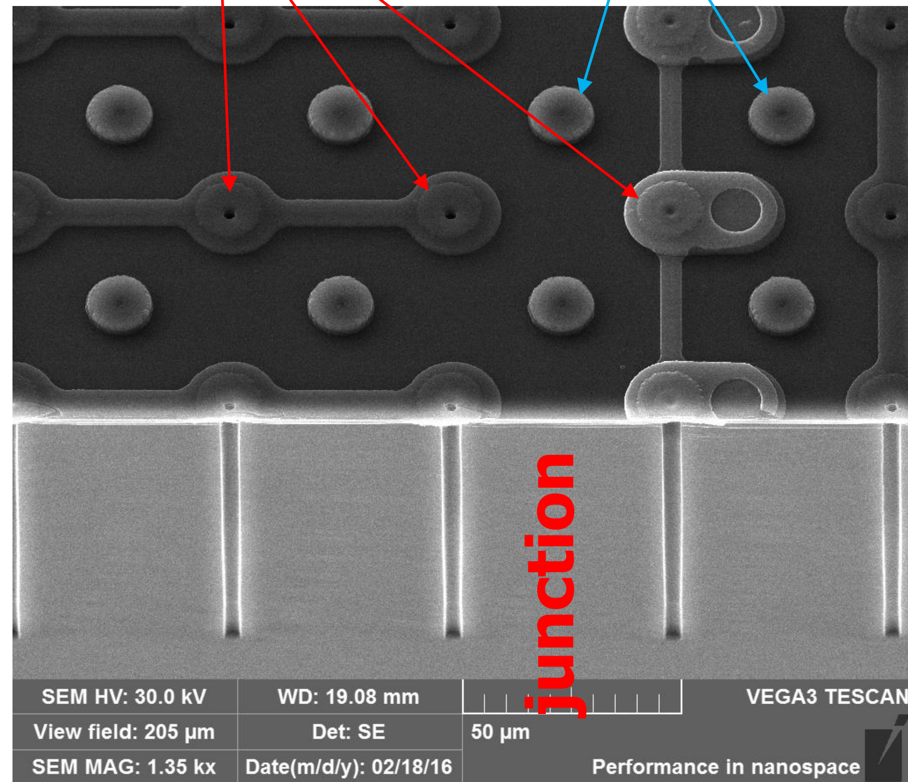
SEM Pictures (4)

Junction Ohmic Junction Ohmic





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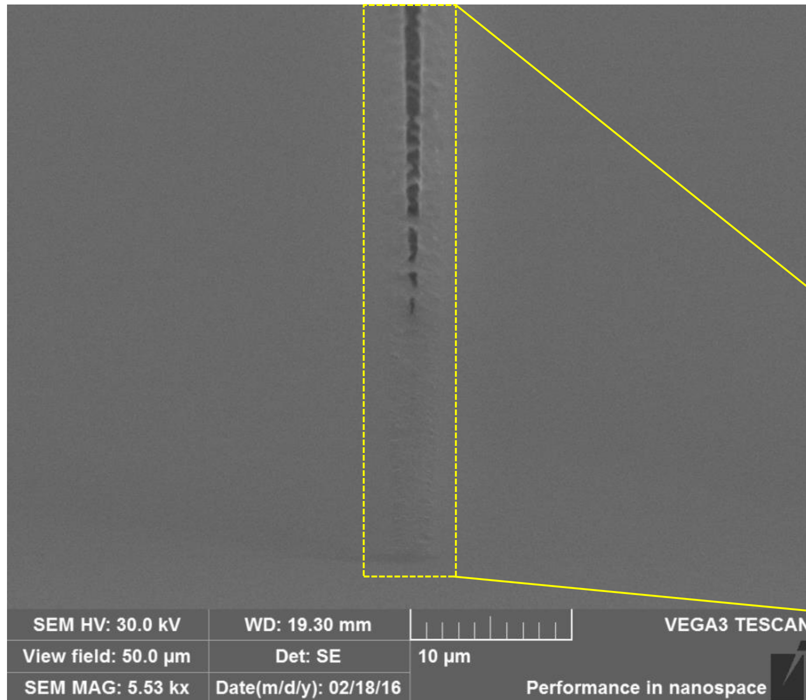
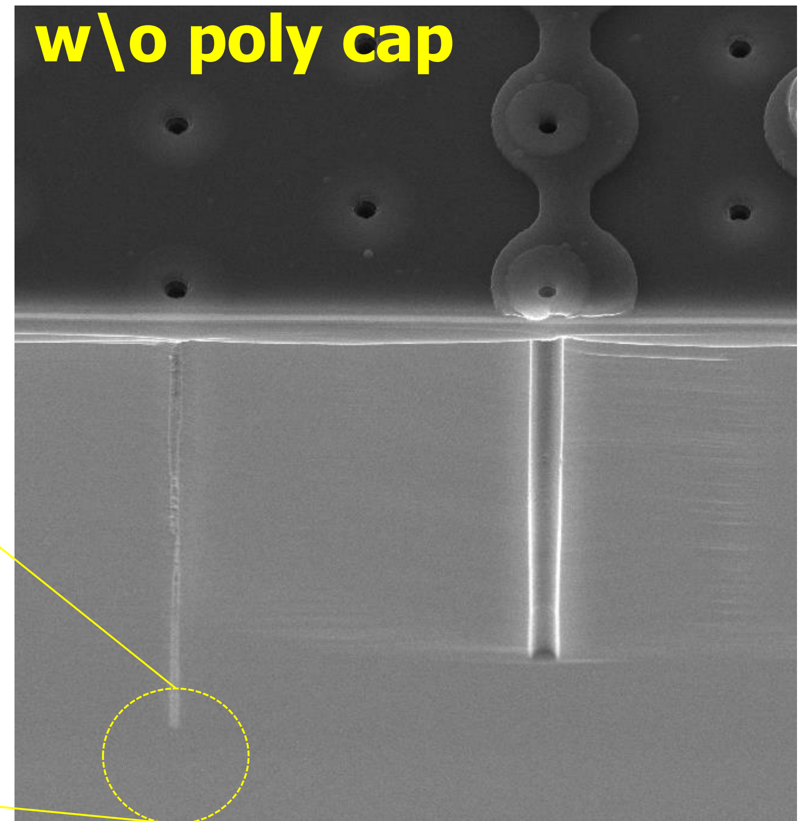
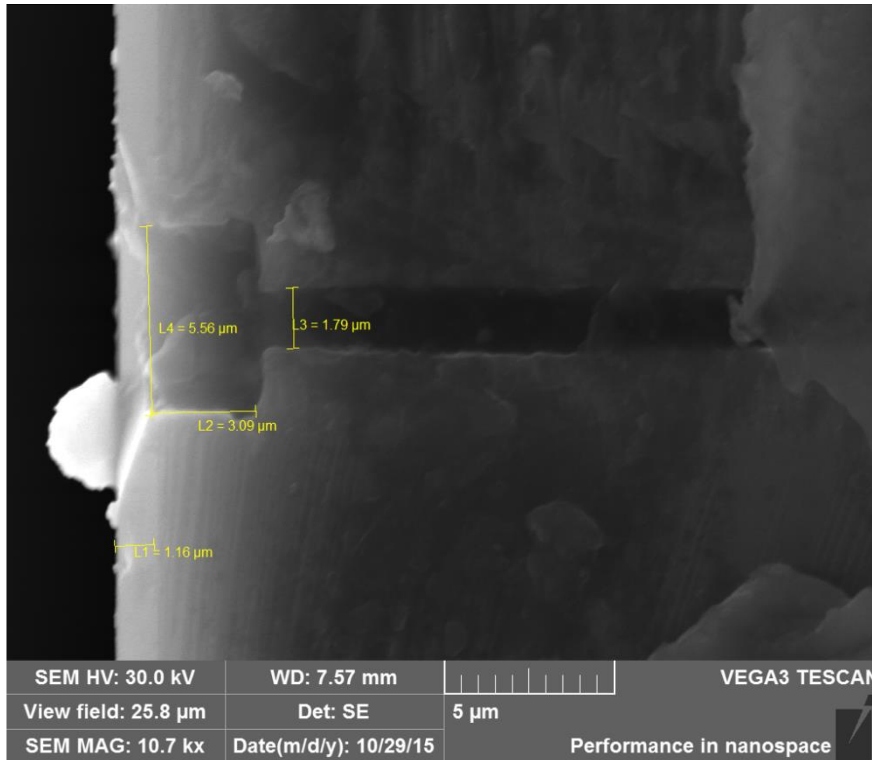
Ohmic & Junction Column

Filled (partially) with polysilicon

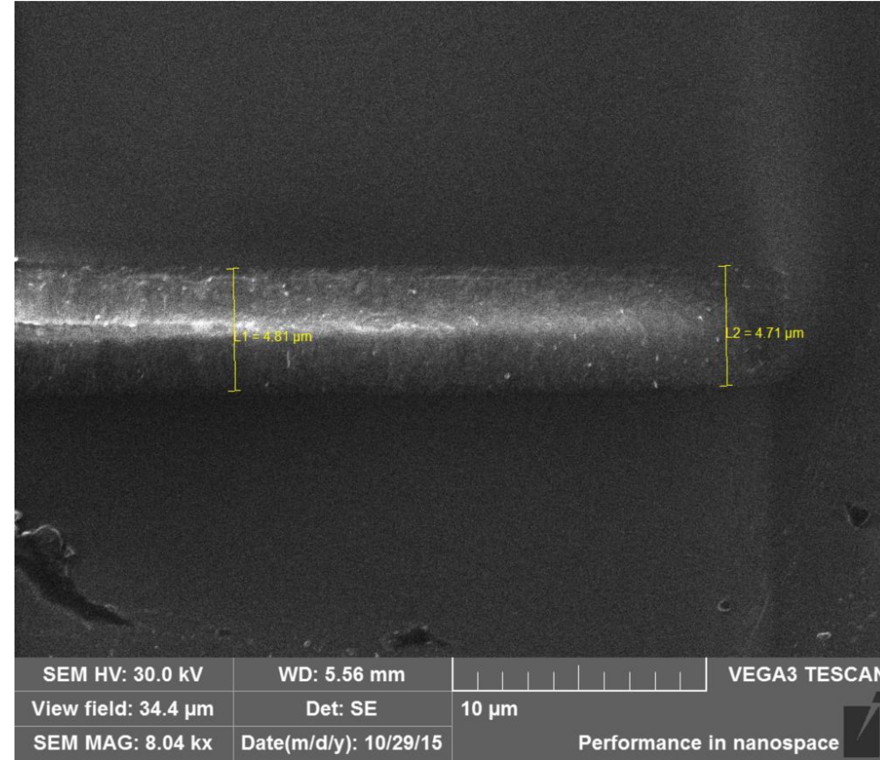




P column etching/poly filling details (w/o poly cap)



Column opening



Column end

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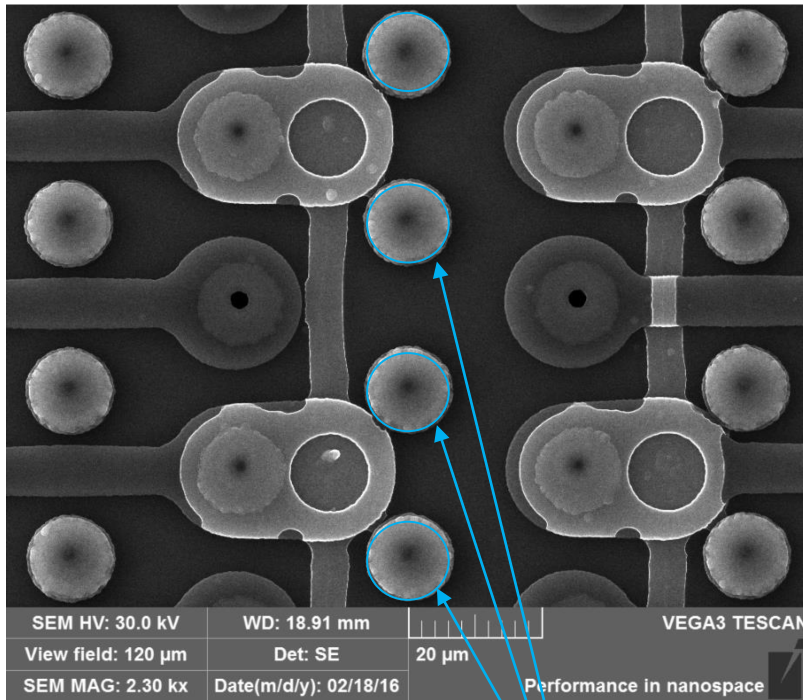
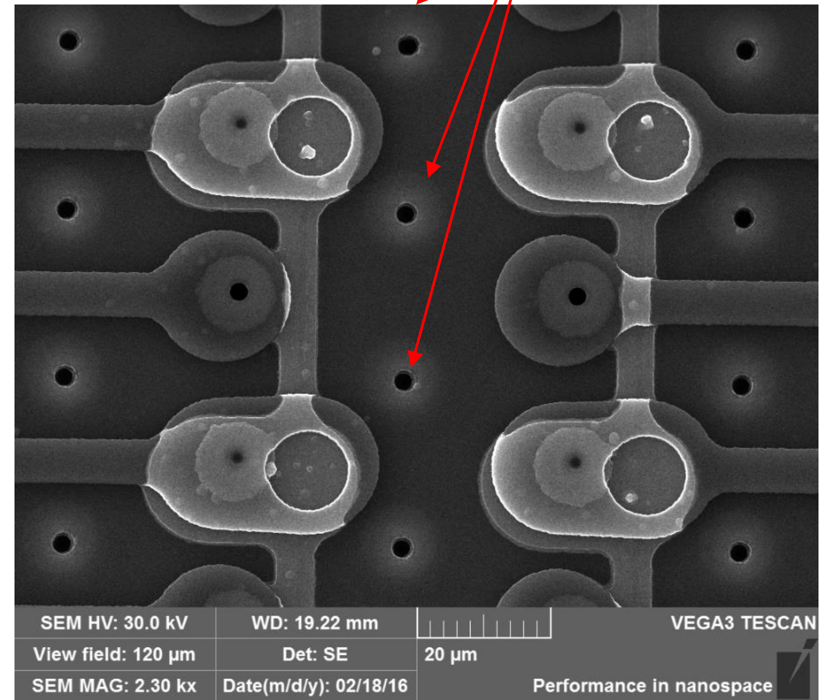
SEM Pictures on «TEST WAFERS»

W or W\O poly cap

without poly cap





with poly cap

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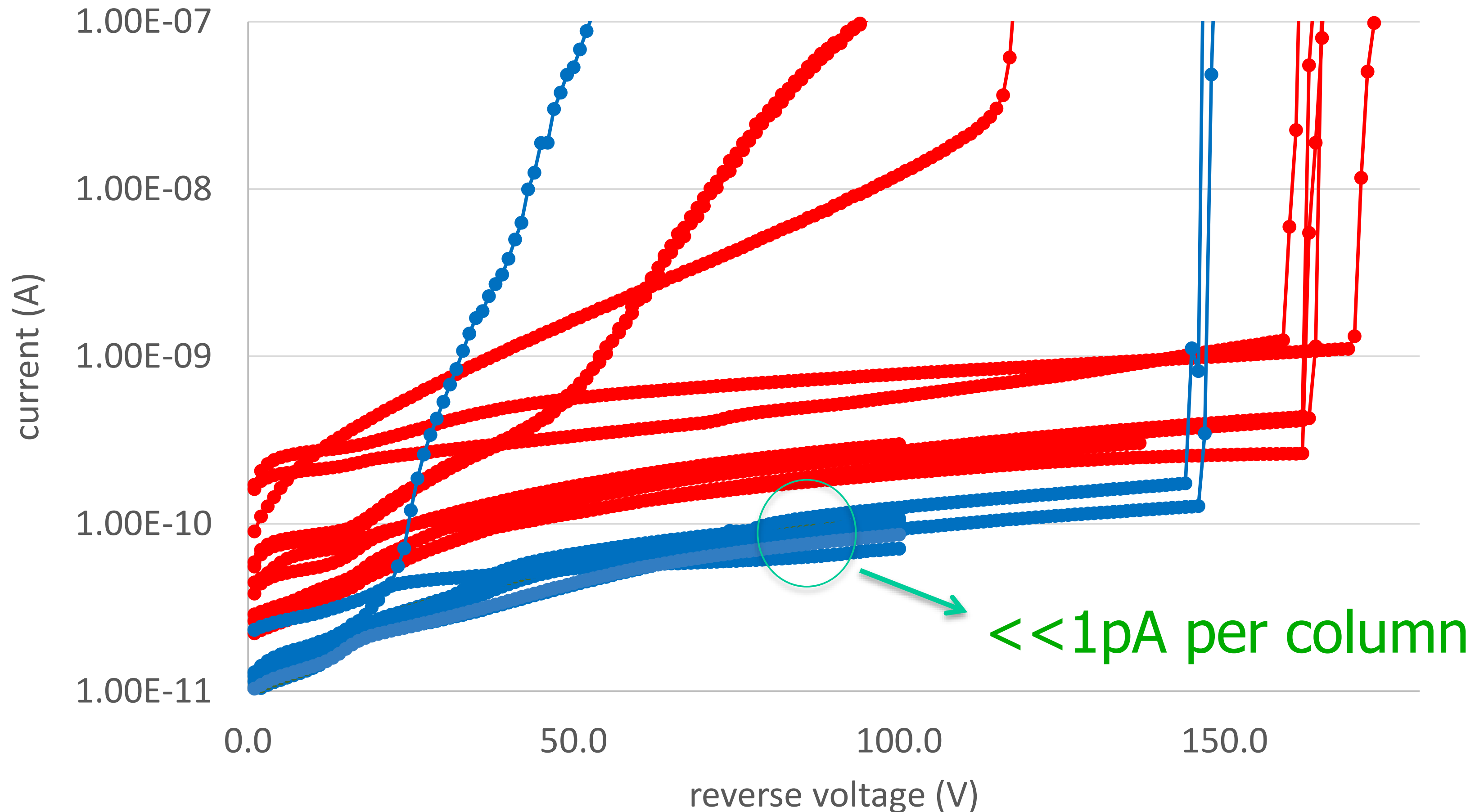
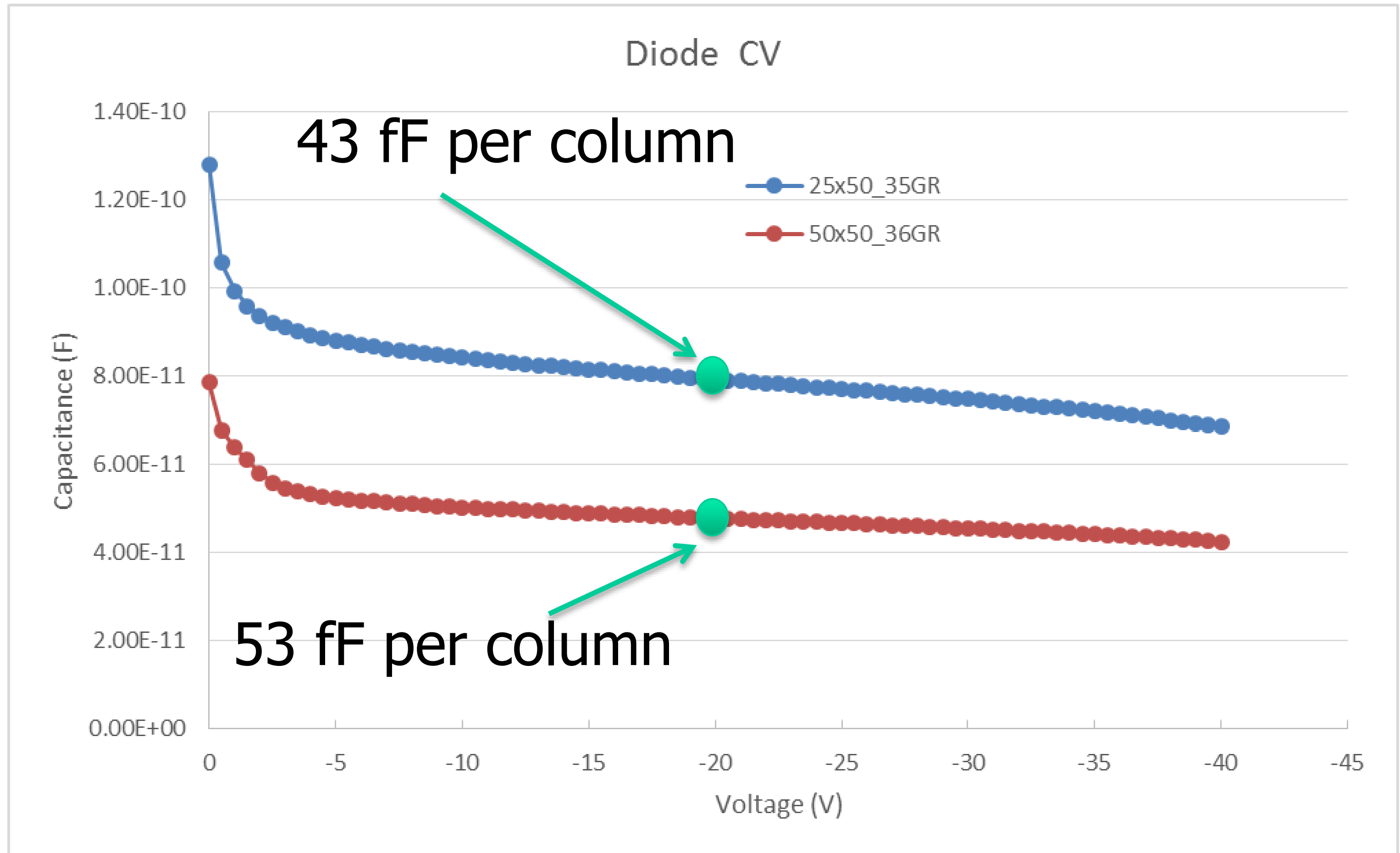
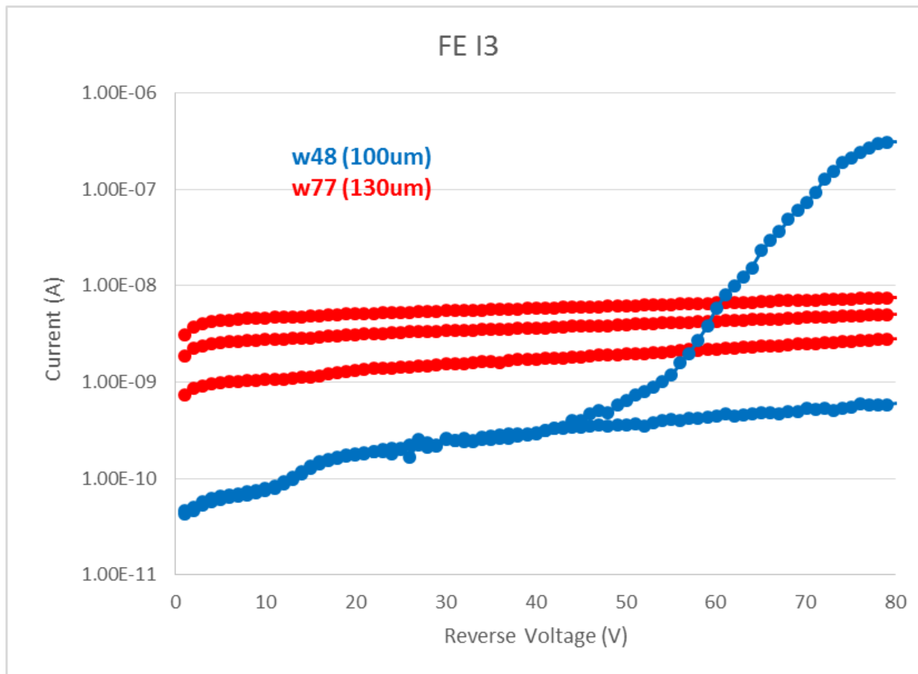
Preliminary test results (1): diode IV

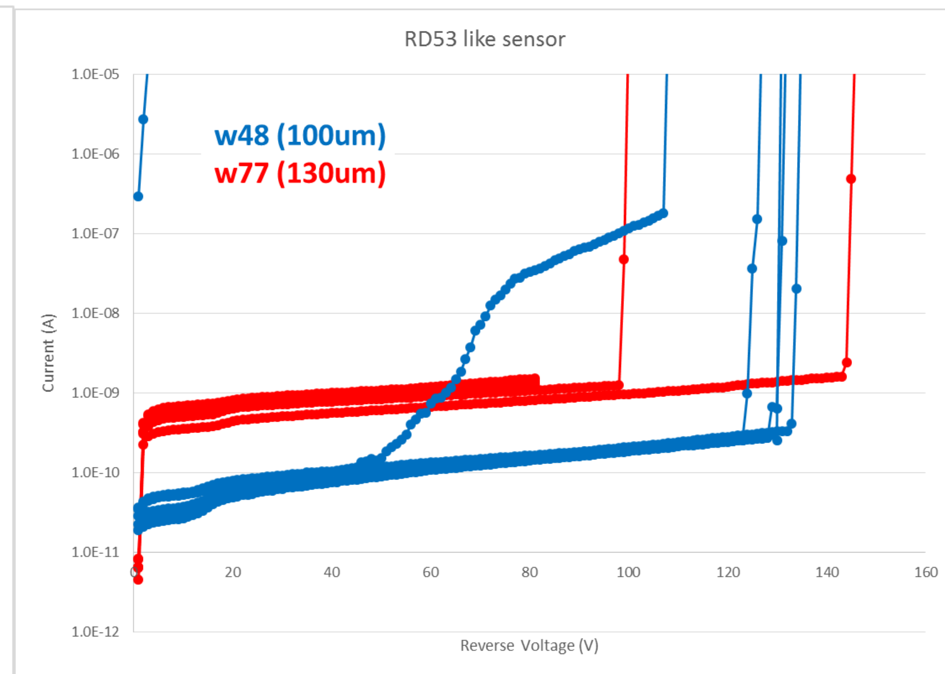


Preliminary test results (2) diode CV



Preliminary test results (3)
sensor IV





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Conclusions and next steps

- Complete the 3D process an all the wafers
- Automatic measurement on all devices\wafers
- Process analysis
- Definition of the next batch