The first reticle size HV-CMOS demonstrator for ATLAS pixel layers

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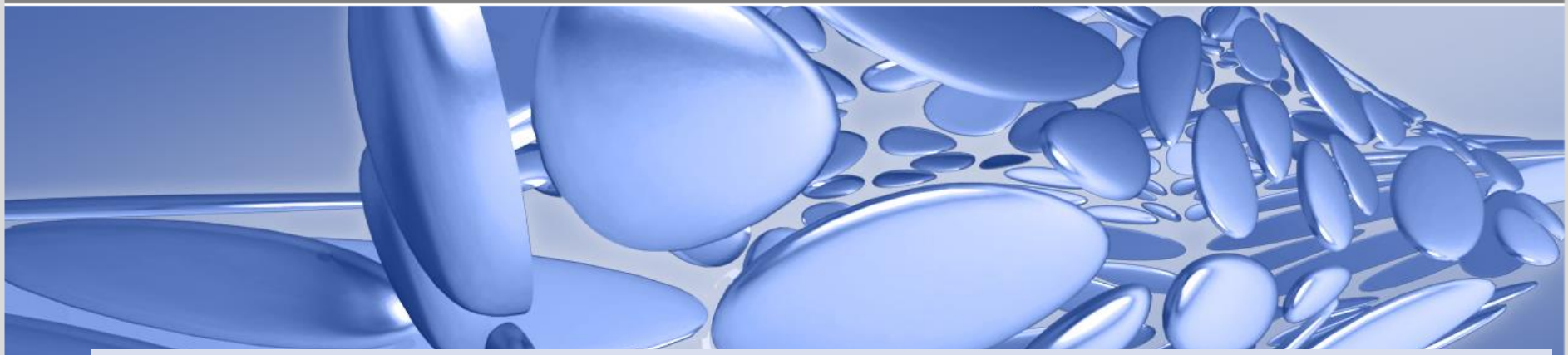
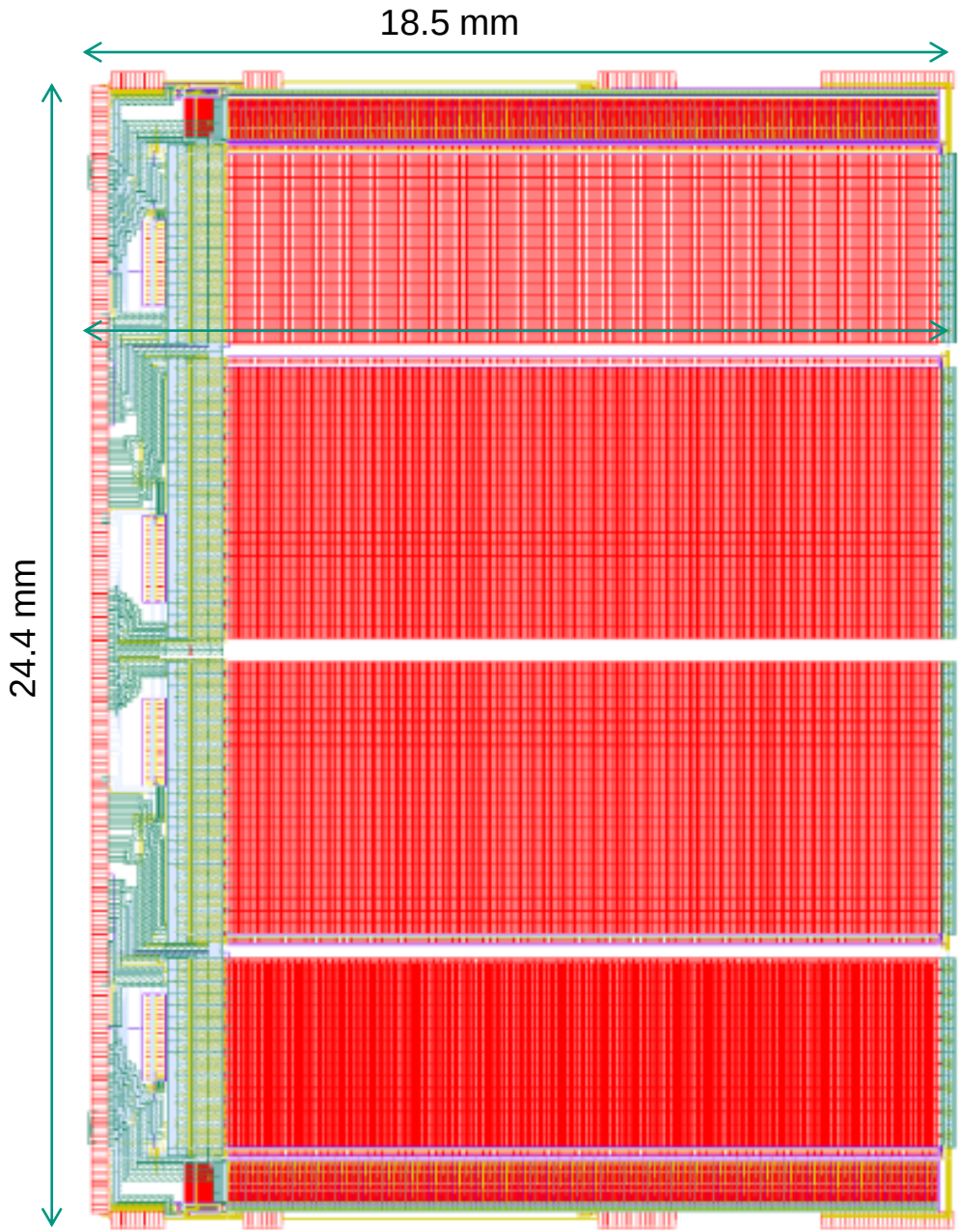
Design: Raimon Casanova Mohr, Eva Vilella Figueras, Roberto Blanco, Ivan Peric
for HVCMOS-Demonstrator collaboration*

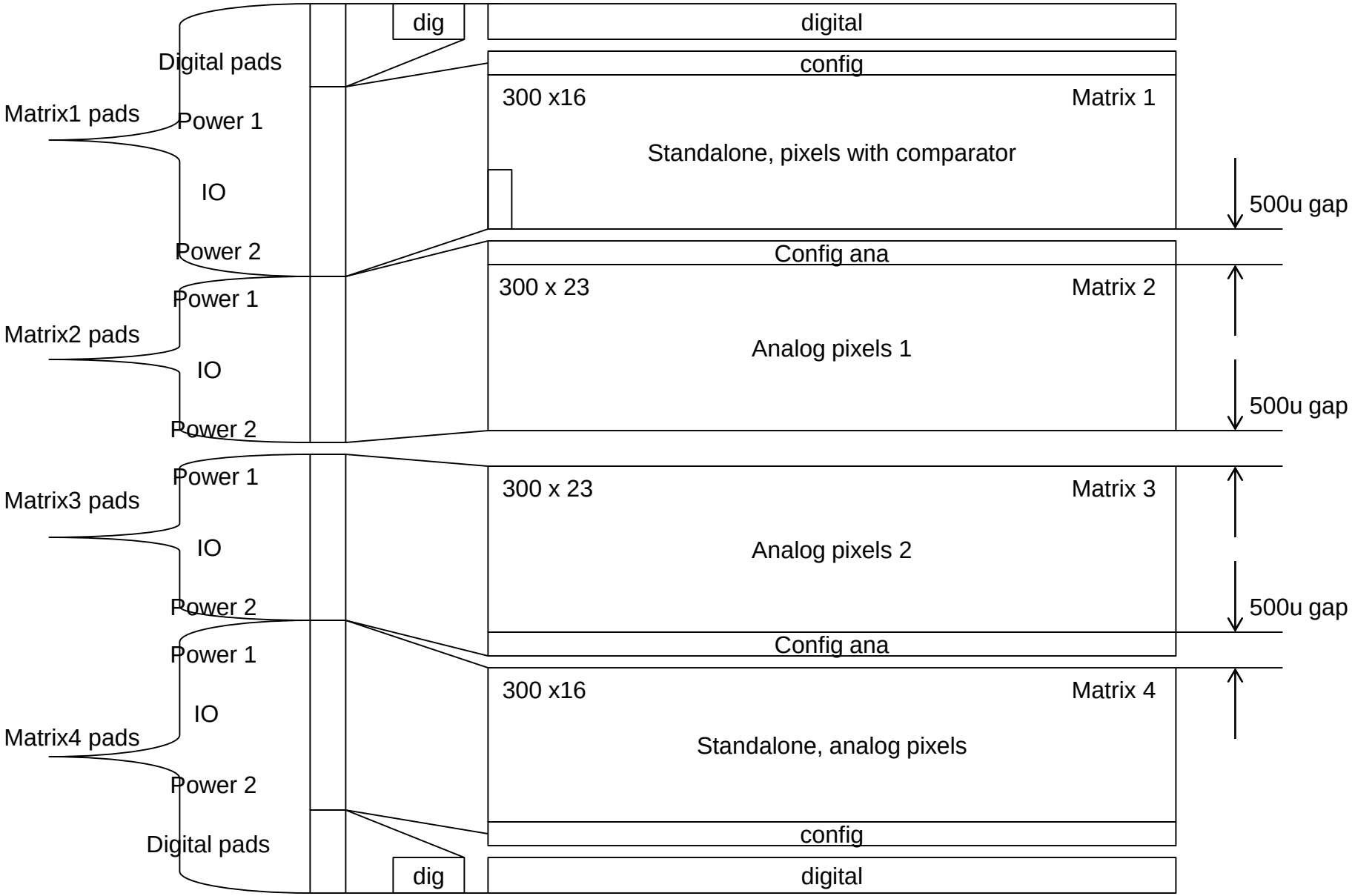


***University of Bern, IFAE Barcelona, CERN, University of Geneva, University of Liverpool and KIT**

- The first reticle size HV-CMOS demonstrator for ATLAS pixel layers has been produced as full mask run – producer **AMS**
- H35 HVCMOS technology (350 nm)
- **The design of the sensor and financing of its production have been done in collaboration between University of Bern, IFAE Barcelona, CERN, University of Geneva, University of Liverpool and KIT**

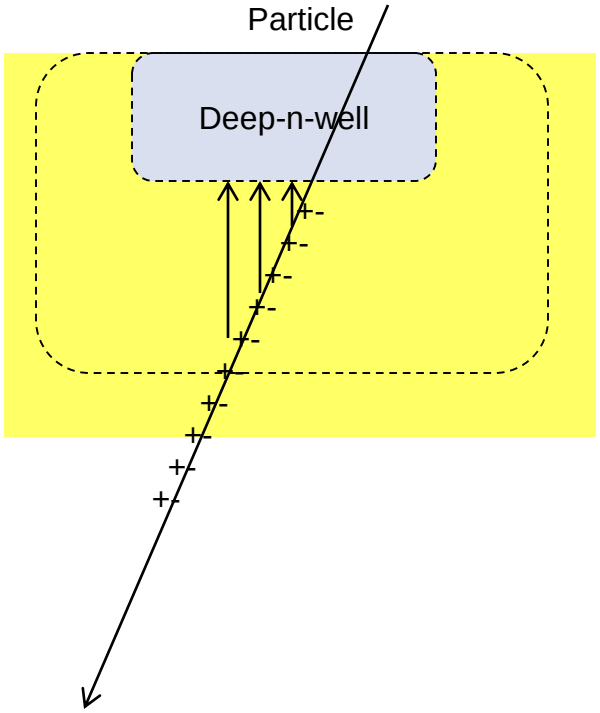

18.5 mm
24.4 mm

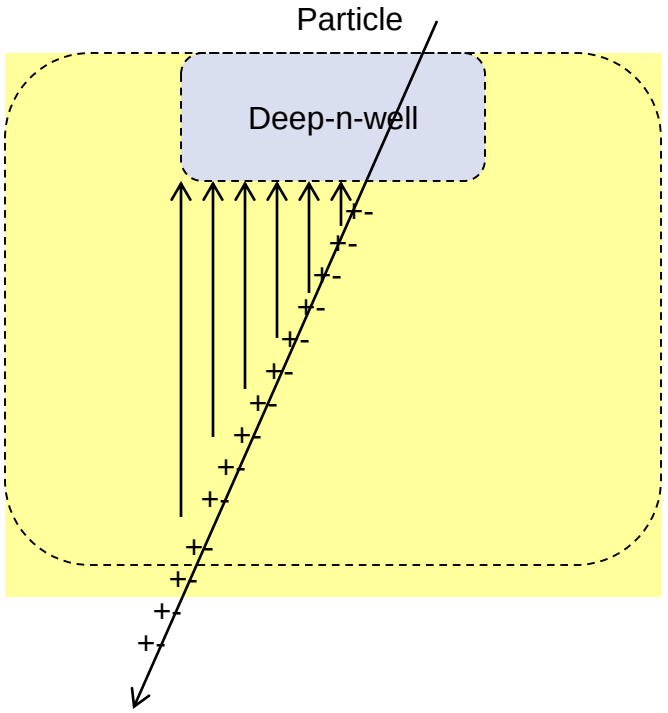
- The chips contain four pixel matrices which are independent and have separated pads


dig
digital
Digital pads
config
Matrix1 pads
Power 1
300 x16
Matrix 1
Standalone, pixels with comparator
IO
500u gap
Power 2
Config ana
Power 1
300 x 23
Matrix 2
Matrix2 pads
Analog pixels 1
IO
500u gap
Power 2
Power 1
300 x 23
Matrix 3
Matrix3 pads
Analog pixels 2
IO
Power 2
500u gap
Power 1
Config ana
300 x16
Matrix 4
IO
Matrix4 pads
Standalone, analog pixels
Power 2
config
Digital pads
dig
digital

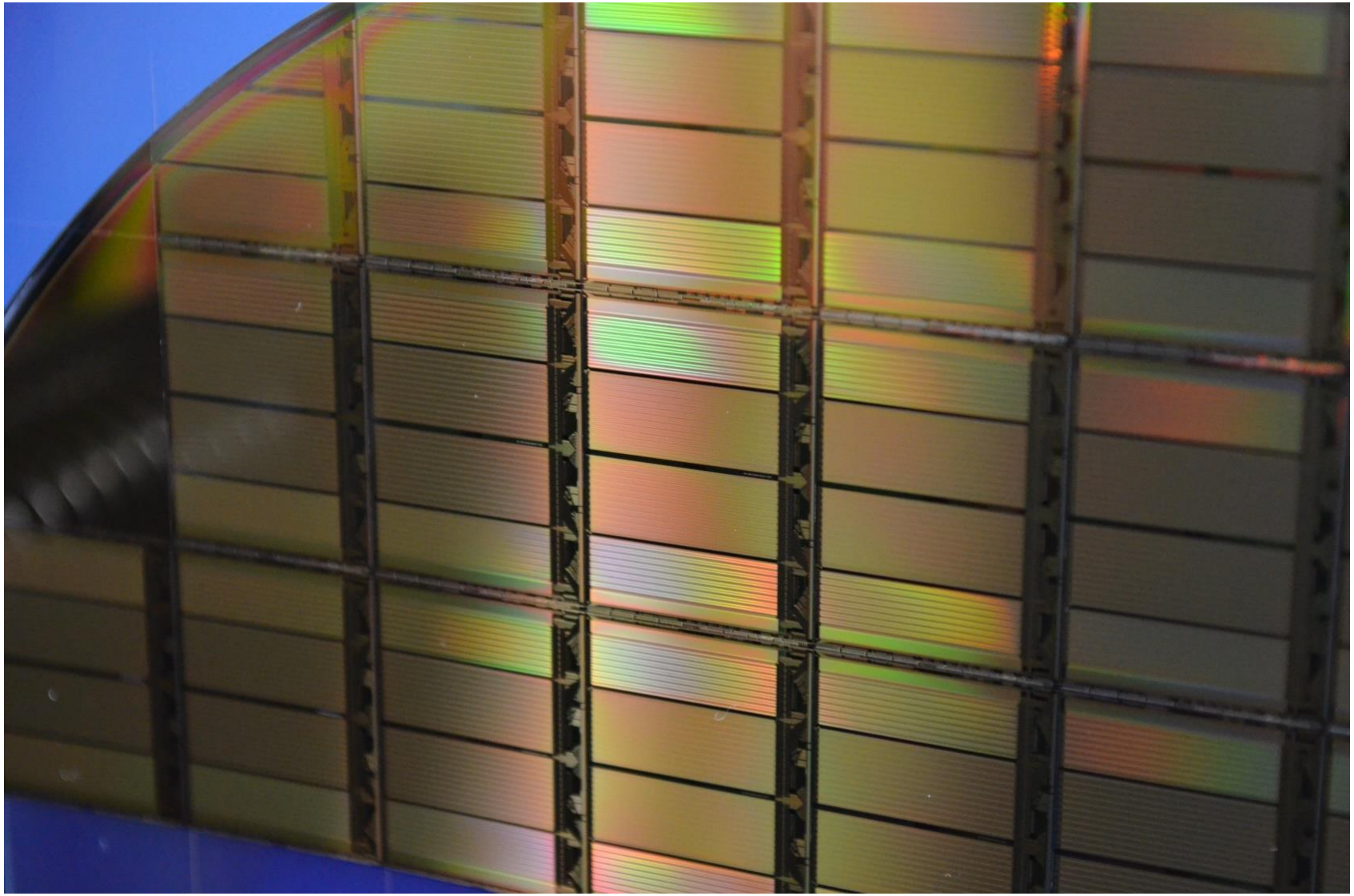
- The sensors have been produced on p-type substrates with four different substrate resistivities: 20, 80 (50-100), 200 (200-400) and 1000 (600-2000) Ωcm

- Substrates of higher resistivity can be used to increase the depleted region size

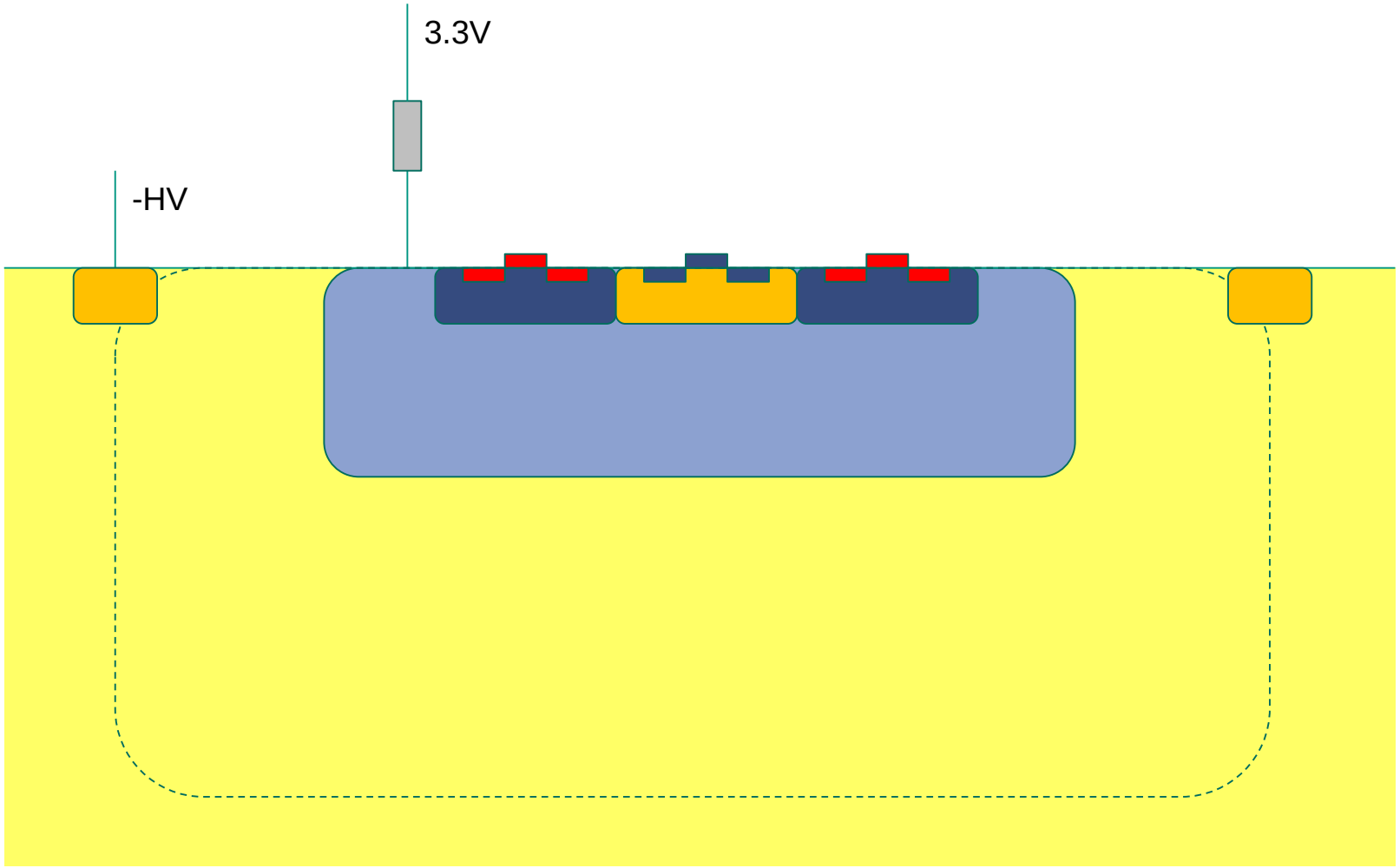




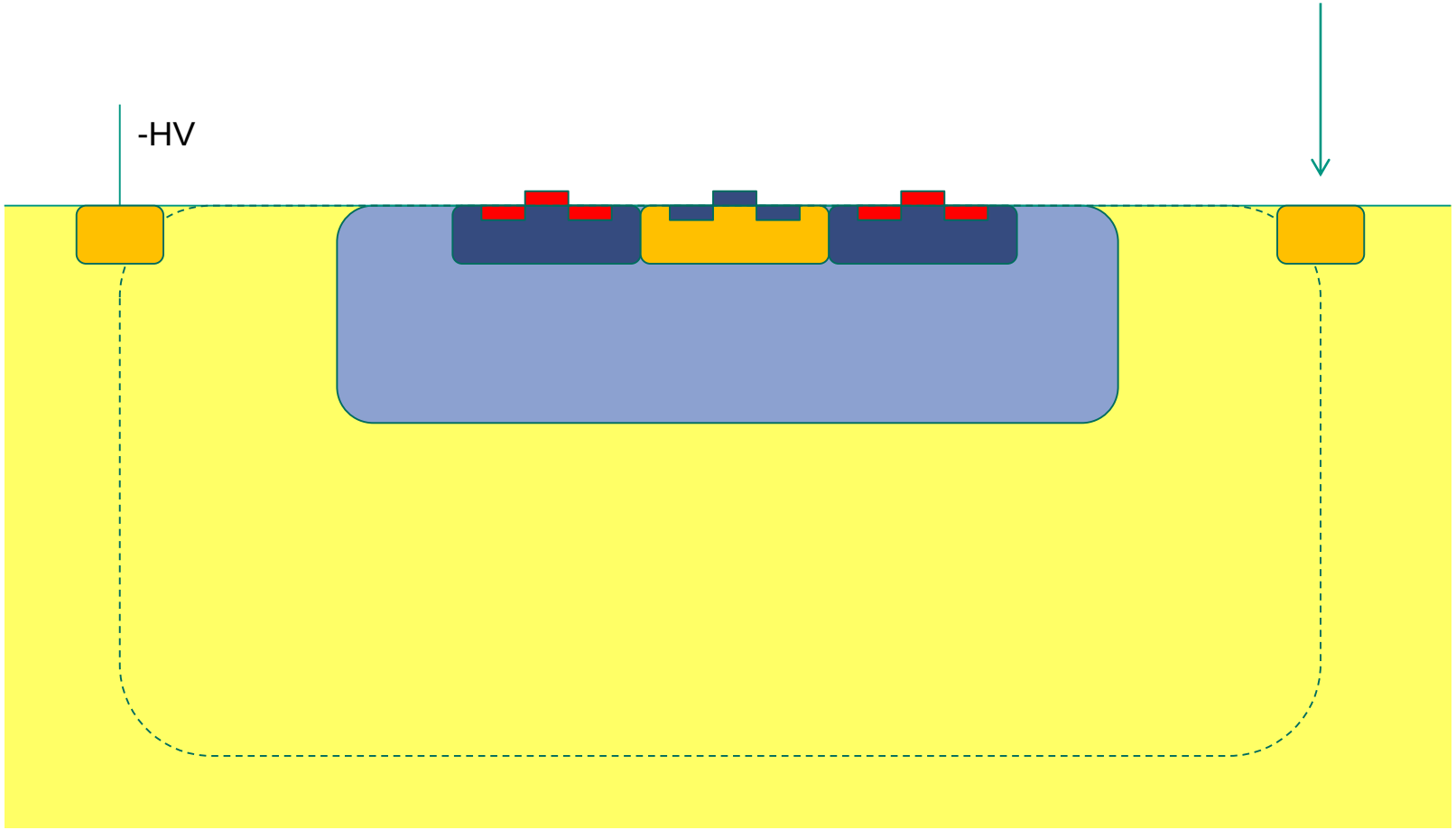
- Photograph of diced wafer



- The sensor structure is deep n-well in p-substrate, electronics is placed inside the deep n-well

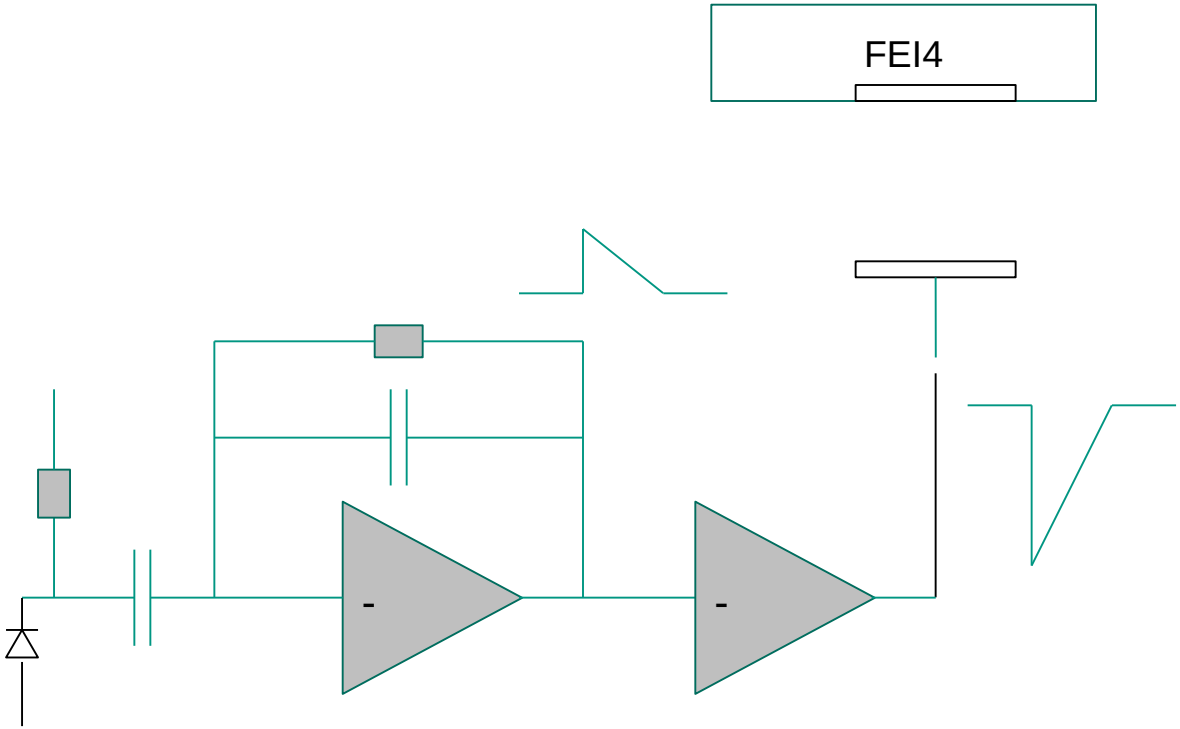


- The p-substrate contact is at the surface (p-well)
- Pixels are separated by p-well guard rings
- N-wells at the periphery are also separated by the p-type guard-rings
- There is a chip guard ring – p-well

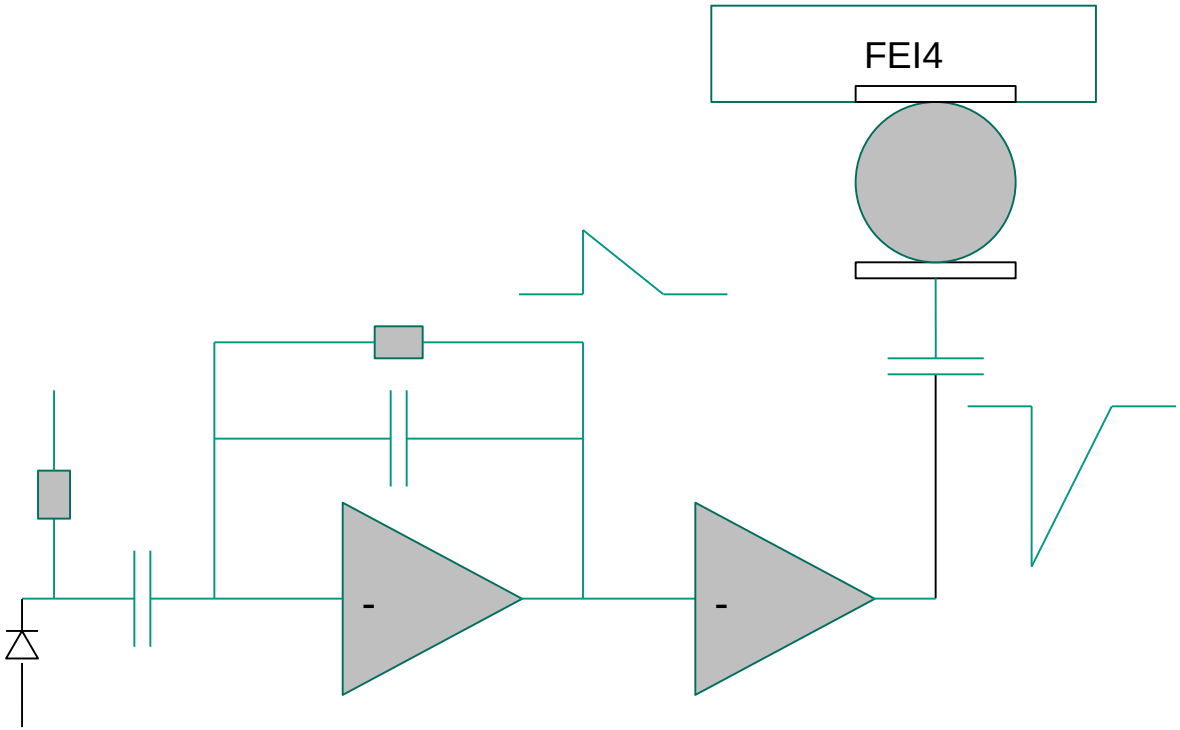


- Post processing of wafers is planned
- Thinning and backside contact
- Bump bonding
- TSV

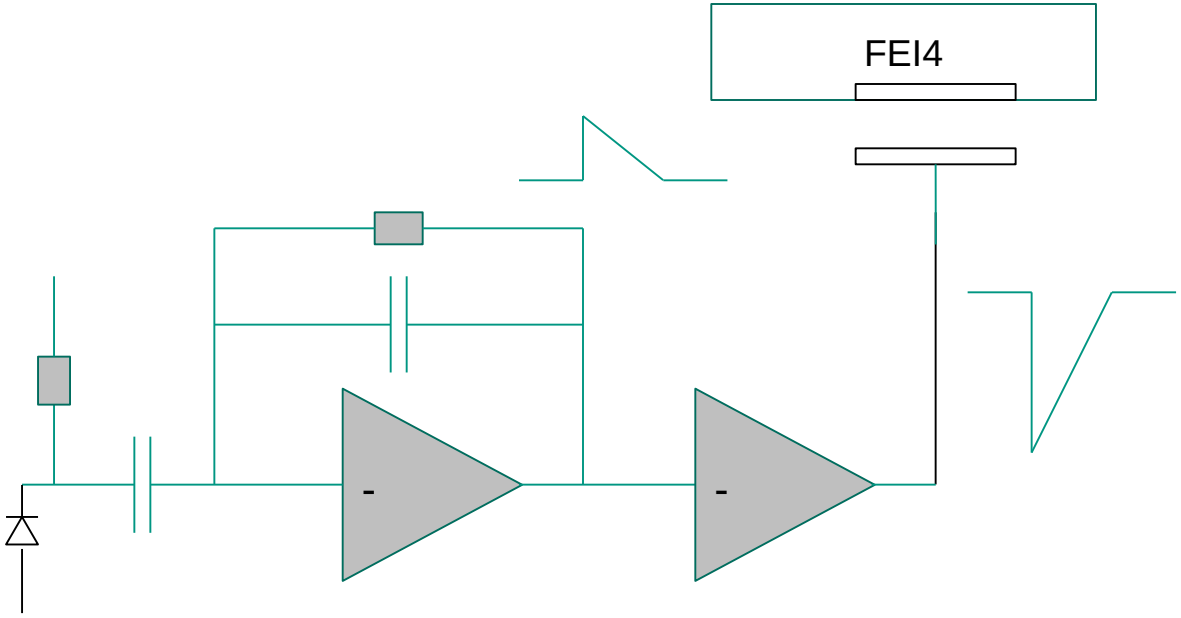
- The first two pixel matrices contain 300 x 23 analog pixels each, that can be bumped/capaciteively coupled to FEI4
- Pixel size 50 µm x 250 µm (equal for all matrices)
- The pixel electronics is based on charge sensitive amplifier (NMOS or PMOS input transistor)
- Second stage amplifier is added to generate negative signal
- The signal will be capacitively transmitted to FEI4



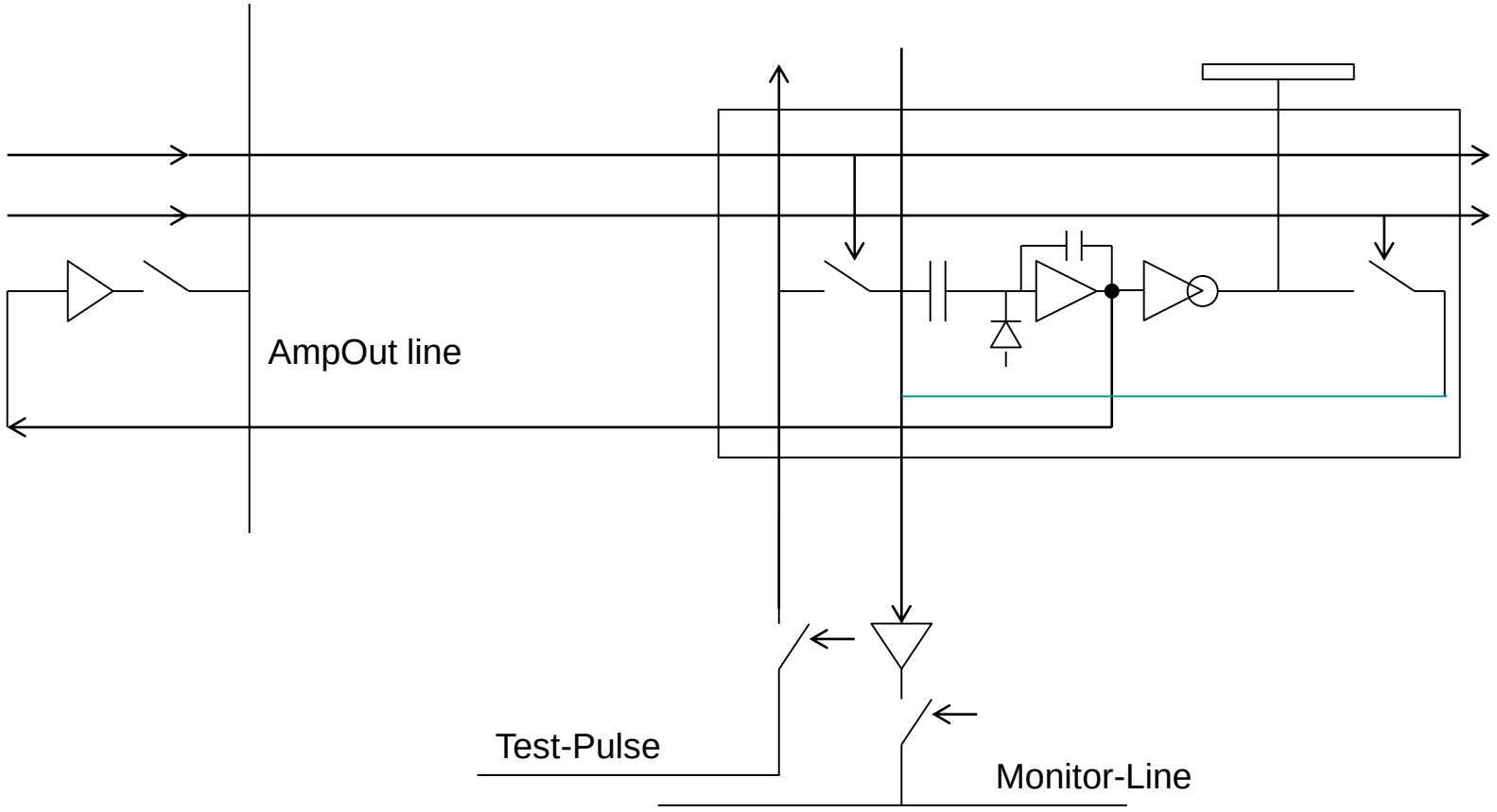
- Bumped FEI4 – on-chip capacitance between the 2nd amplifier output and the pad



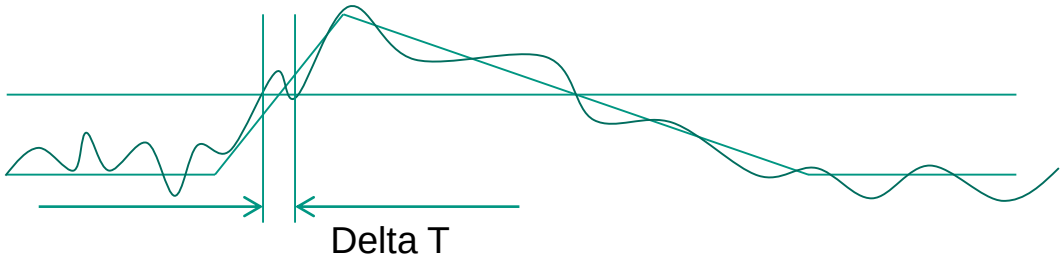
- Capacitively coupled FEI4 – pad connected to the 2nd amplifier output



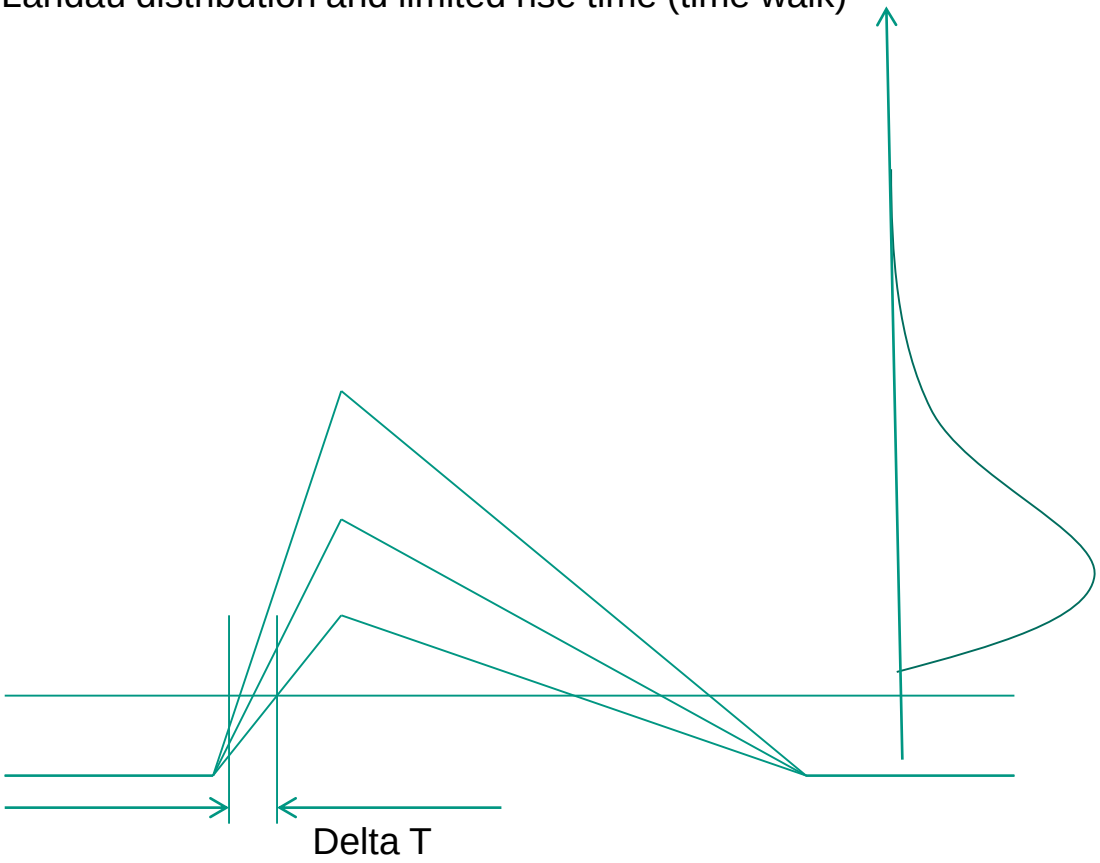
- Standalone measurements are possible
- Charge injection into selected pixel
- Monitor of amplifier outputs (second stage) of three chosen pixels
- 1st amplifier output in one pixel per row can be measured using AmpOut line



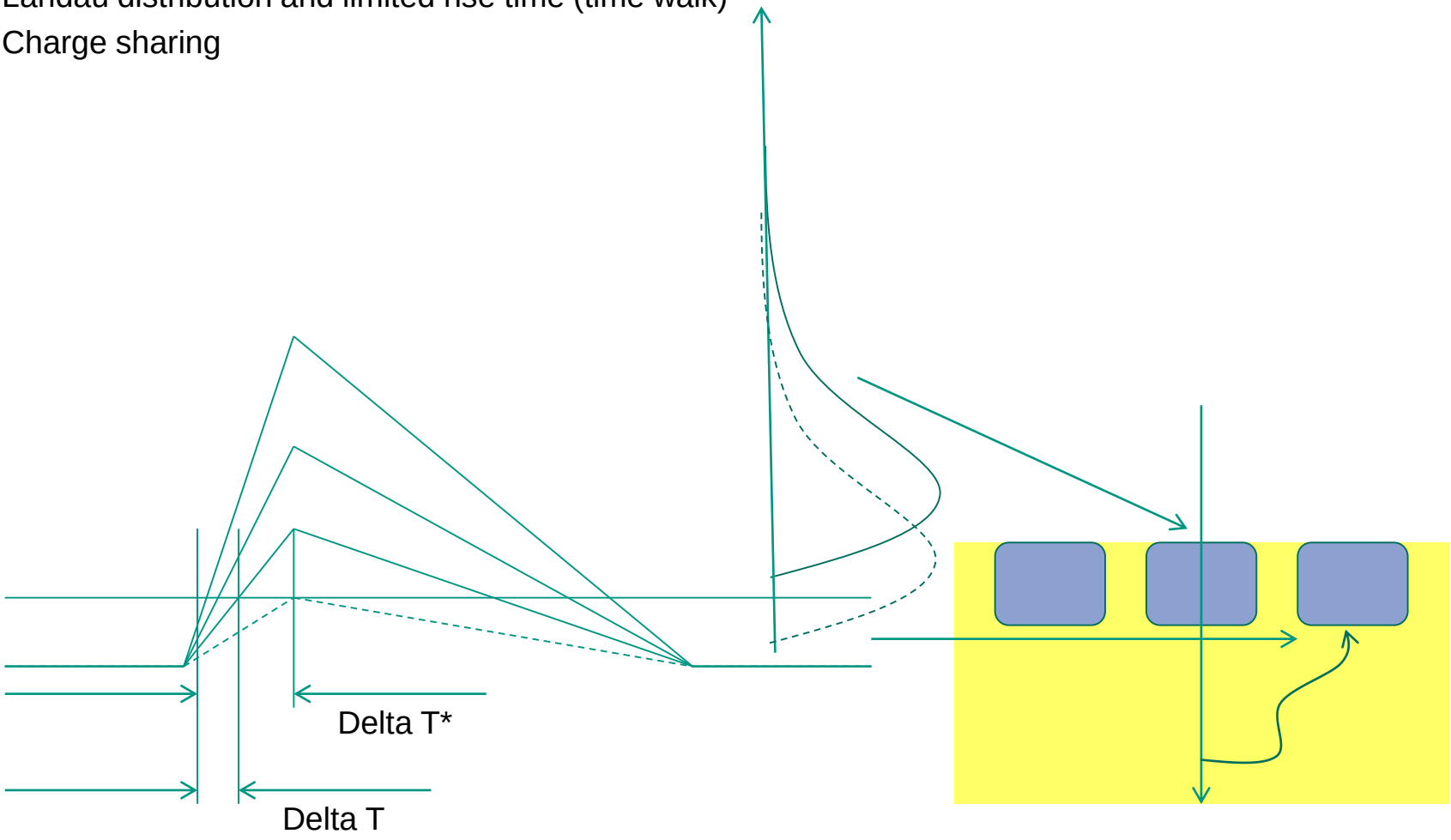
- Time resolution
- Time resolution mainly limited by
- Noise



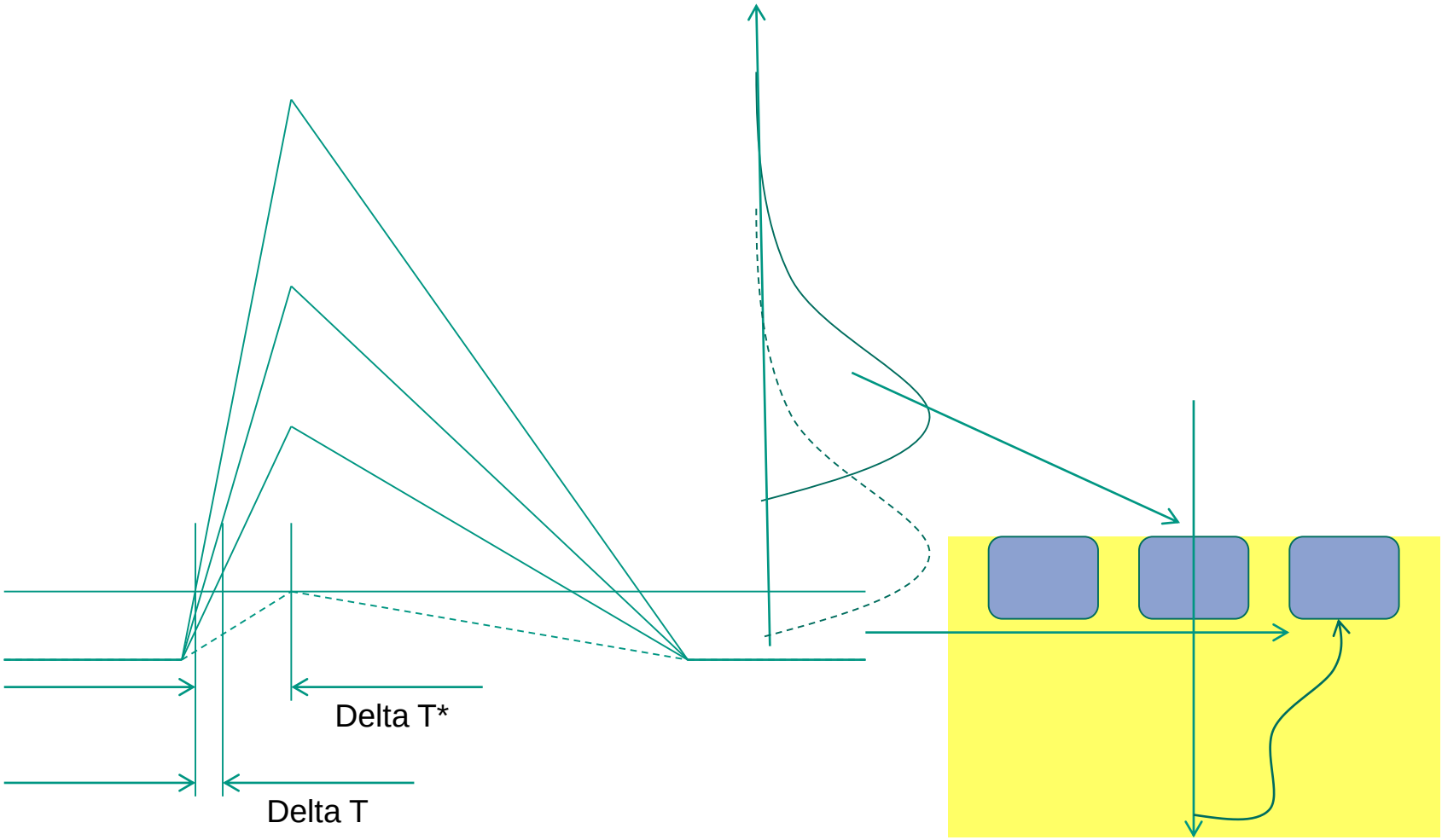
- Time resolution
- Time resolution mainly limited by
- Noise
- Landau distribution and limited rise time (time walk)



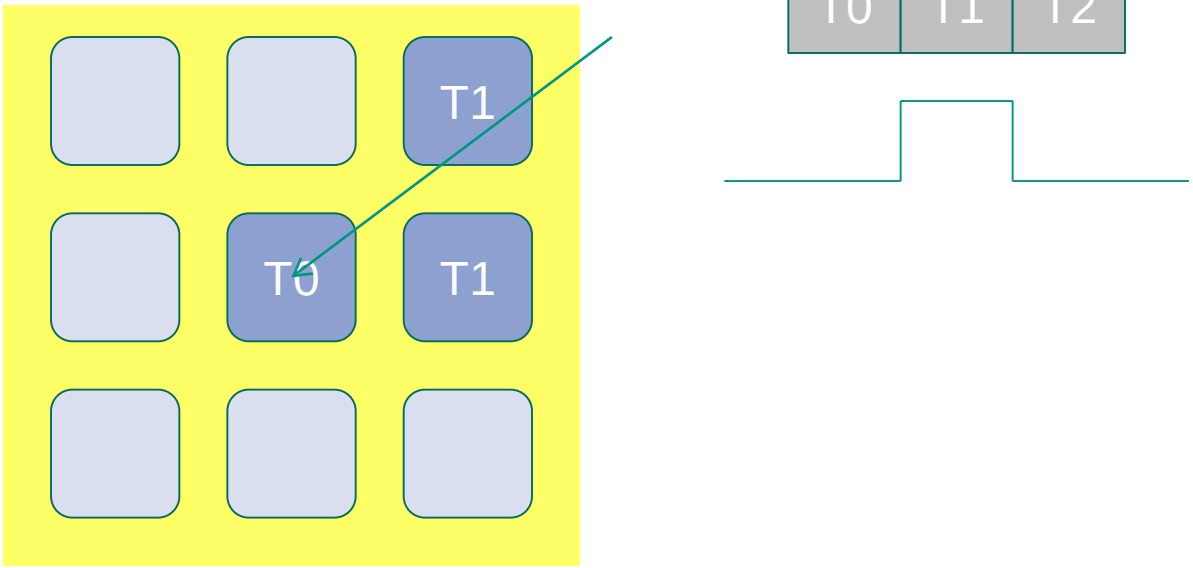
- Time resolution
- Time resolution mainly limited by
- Noise
- Landau distribution and limited rise time (time walk)
- Charge sharing



- The use of high res substrate will increase signal (unirradiated sensor) -> good for time walk
- However: charge sharing will be increased



- Possible problem – fake hits due to late signal generation in neighbor pixels



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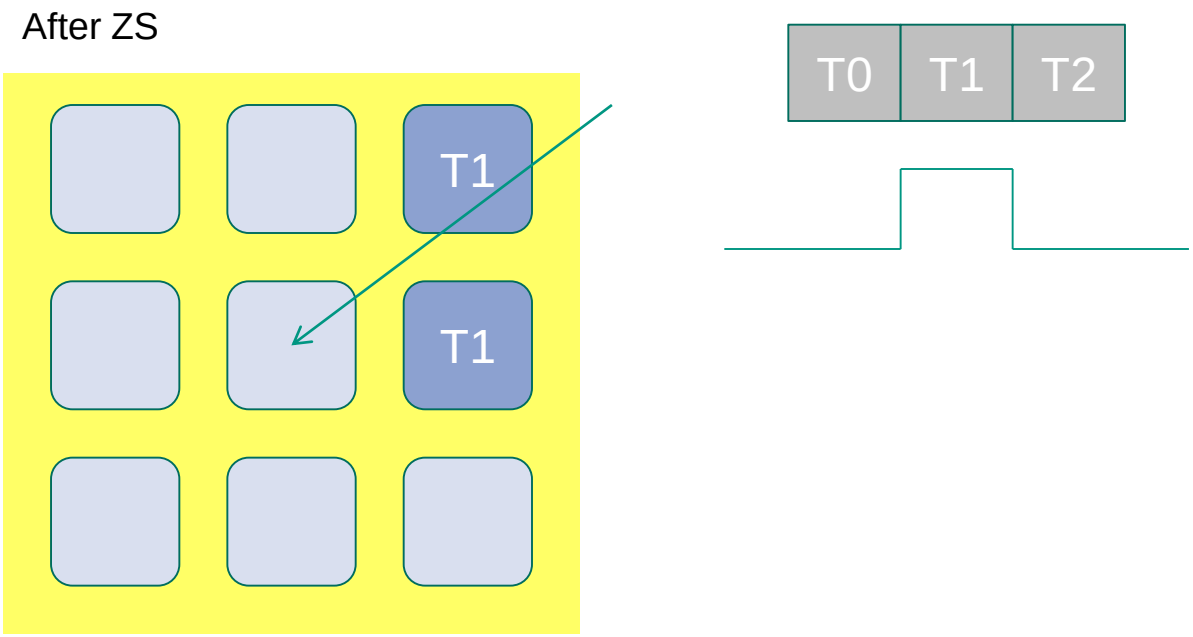
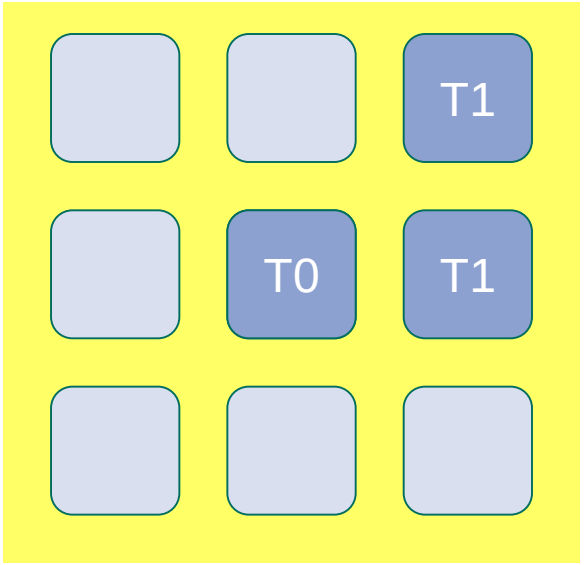
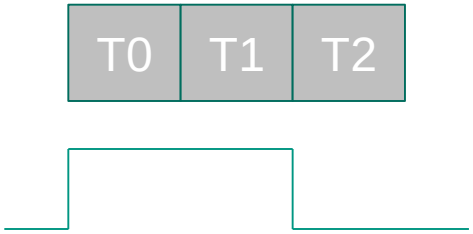


- Possible problem – fake hits due to late signal generation in neighbor pixels
- (Not so nice) remedy – increased trigger window.

After ZS

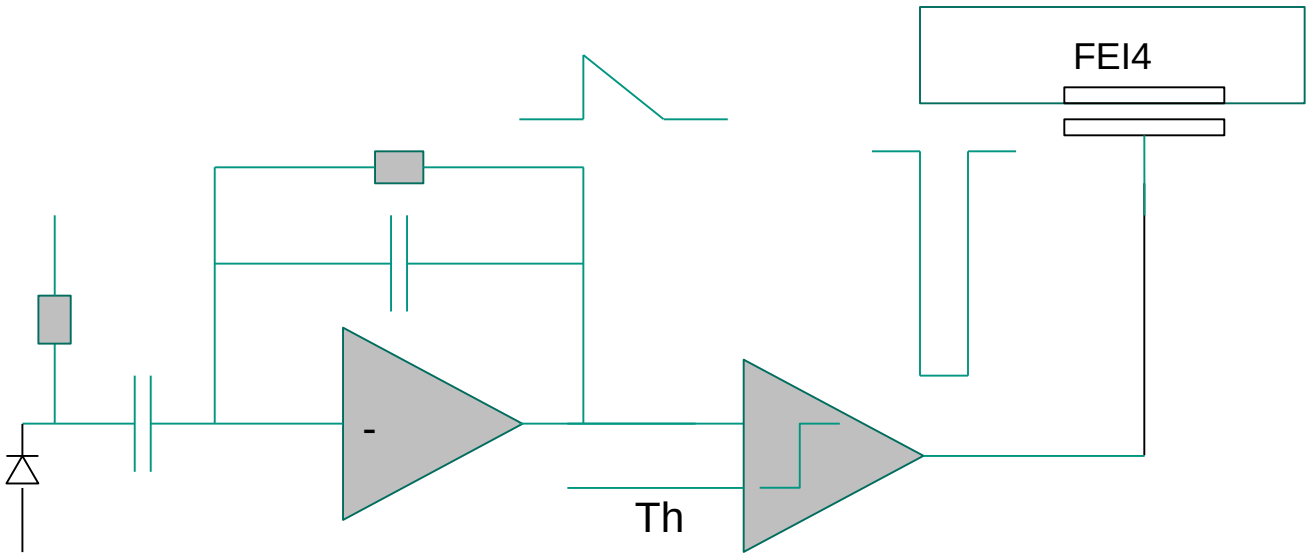




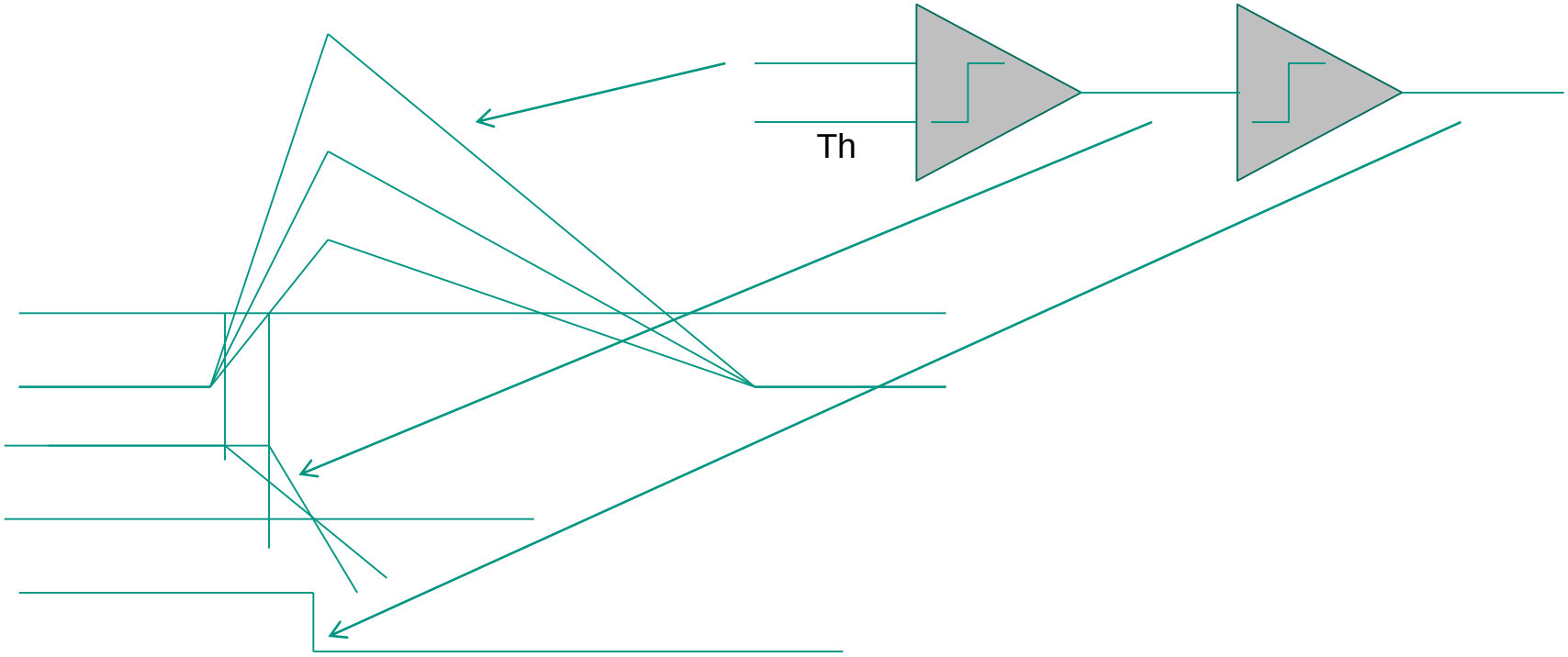
- Additional problem: signal amplitude after irradiation is unknown
- => We tried to improve time resolution for standard (low res signals) by designing clever electronics

- Analog pixels, time walk correction within FEI4 can be used
- If neighbor pixels produce consecutive time stamps, the time stamp of large hit (with larger ToT) is used

- Third matrix: 16 x 300 digital pixels
- Pixel electronics with comparator
- First version – standard comparator

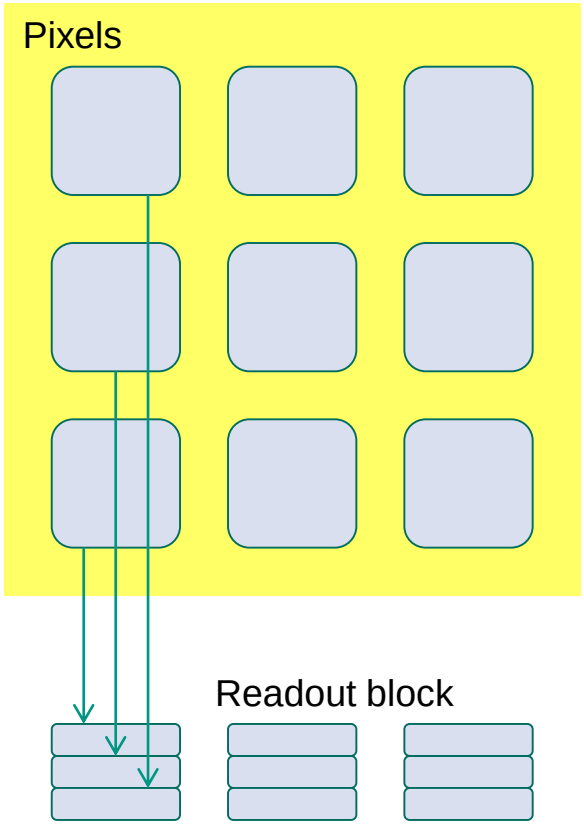


- Second version – time walk corrected comparator
- Larger signal overdrive – comparator output is slower
- Additional comparator produces corrected signal

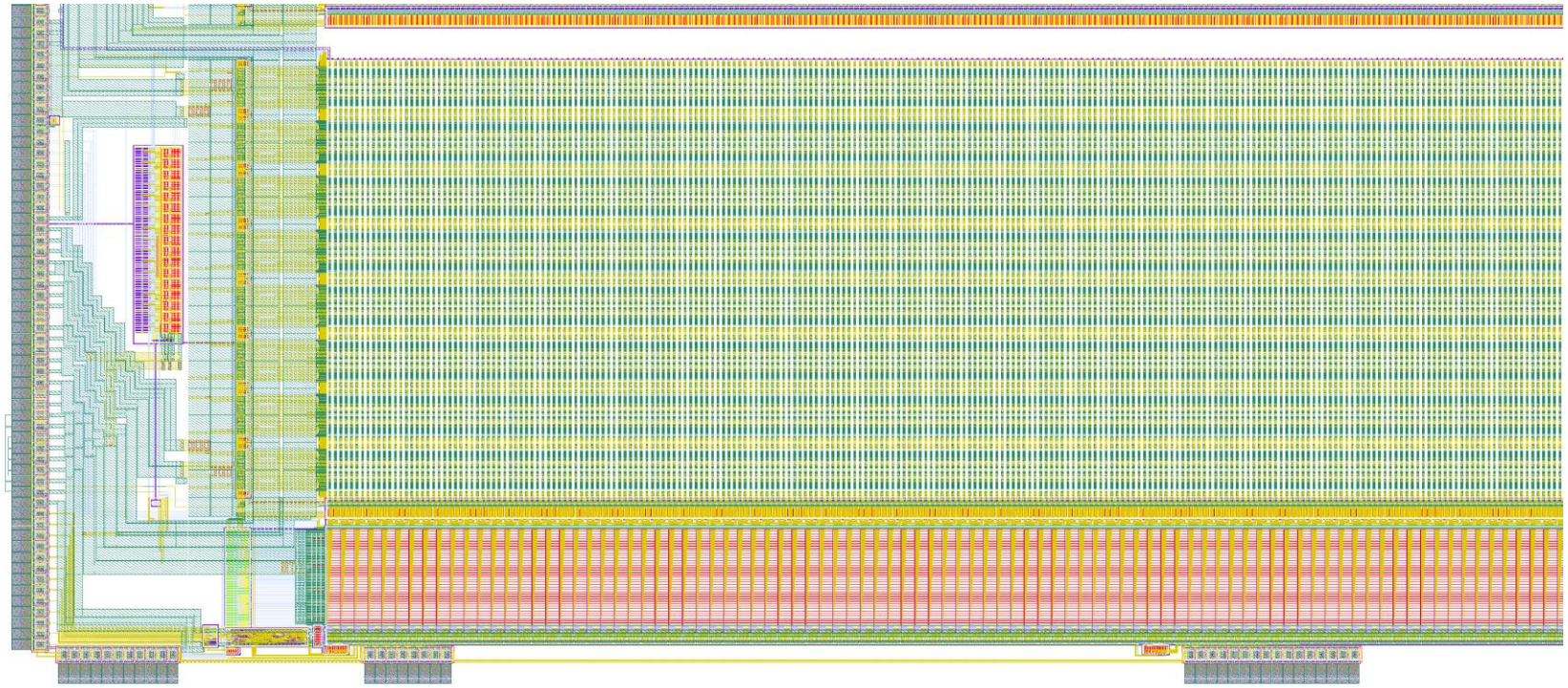


Digital pixel matrix with on-chip readout

- The matrix has attached on-chip readout block
- The pixels can be readout by FEI4 and also stand alone
- 1-1connection between every pixel and its readout cell
- TS is stored upon hit arrival, column drain readout
- Untriggered readout, 320MBit/s serializers

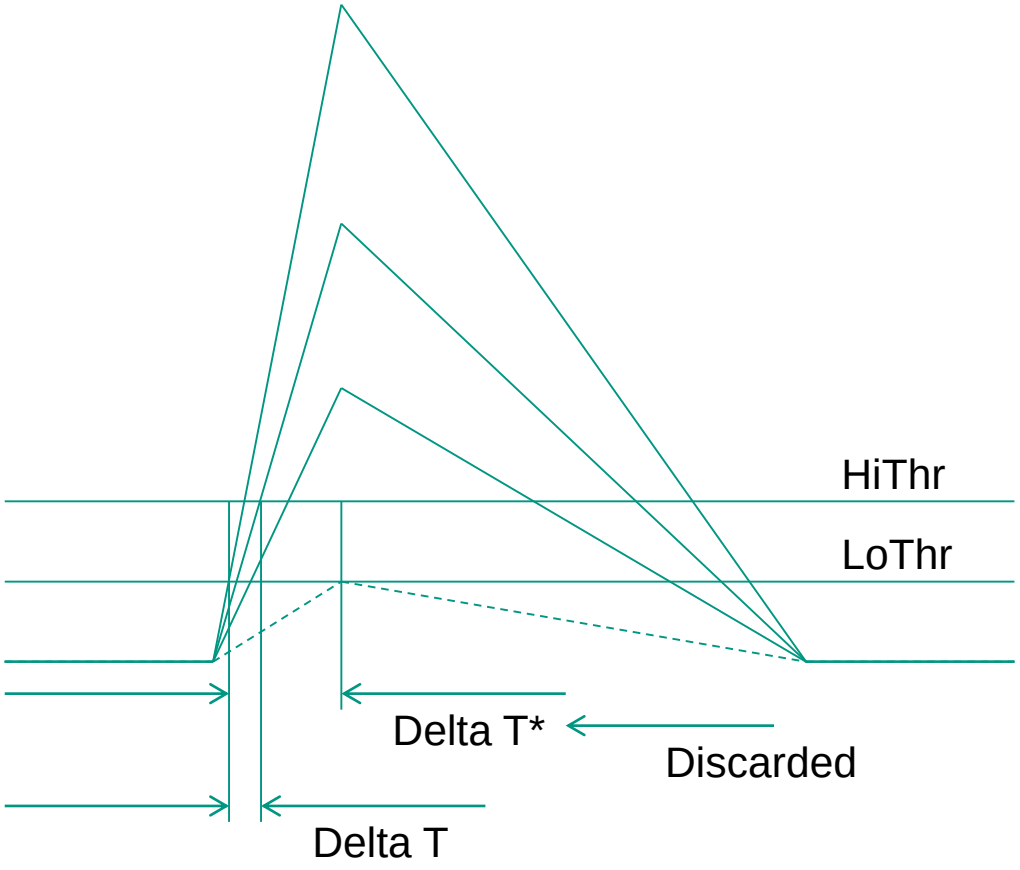


Digital pixel matrix with on-chip readout

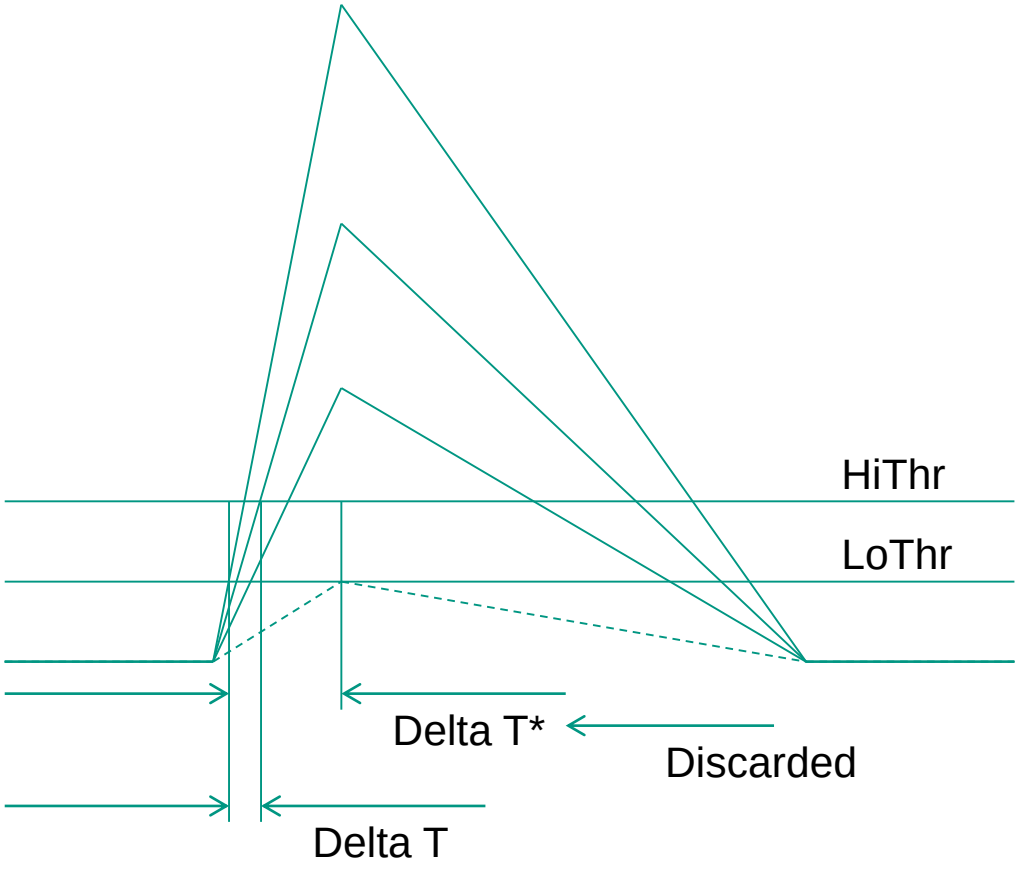


Analog pixel matrix with on-chip readout

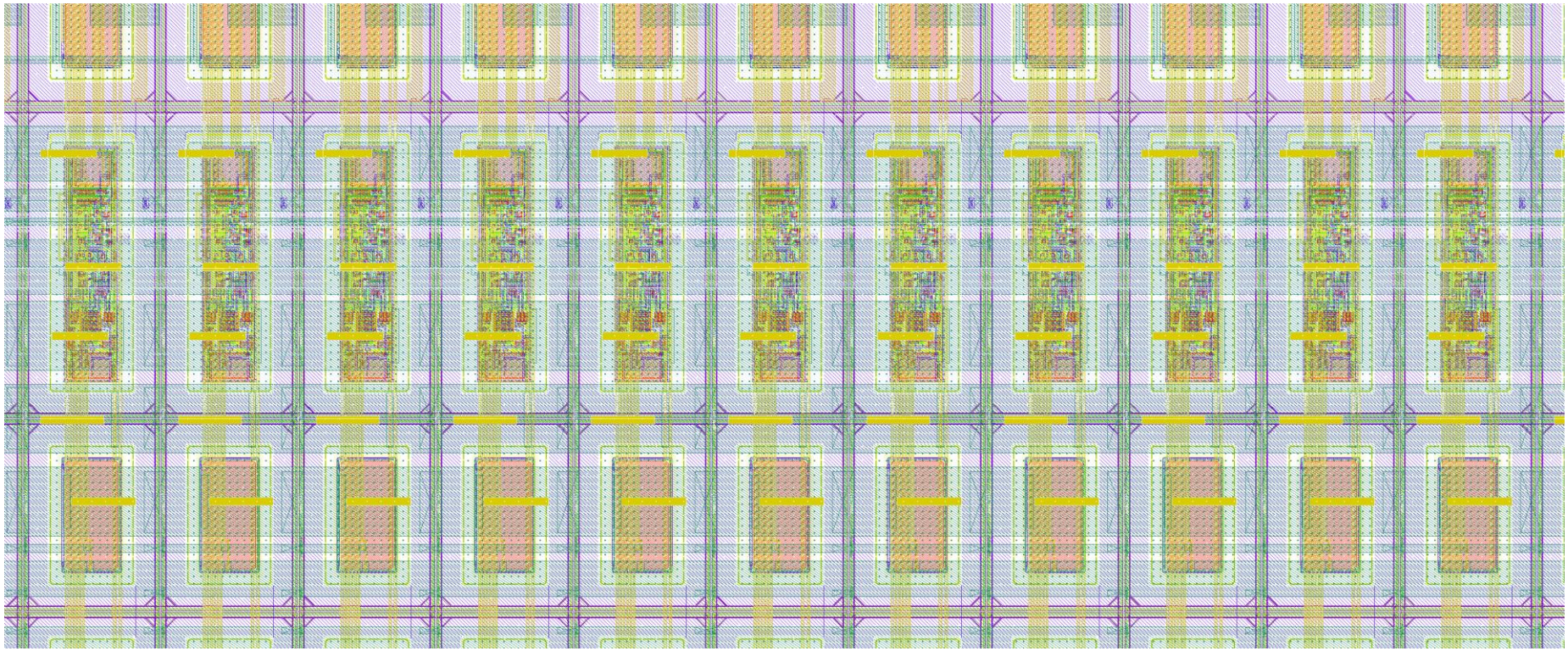
- Fourth matrix: 16 x 300 analog pixels with standalone readout
- 1-1connection between every pixel and its readout cell
- Two thresholds: TS is stored after crossing of lower threshold, readout is initiated only if the higher threshold is exceeded



- Two simulation procedures:
- Signal is swept within the range: 0.5 MPW -> 3 MPW
- Signal is swept: 0 -> 3MPW
- Threshold put at 6 x sigma noise
- Time walk is less than 25ns



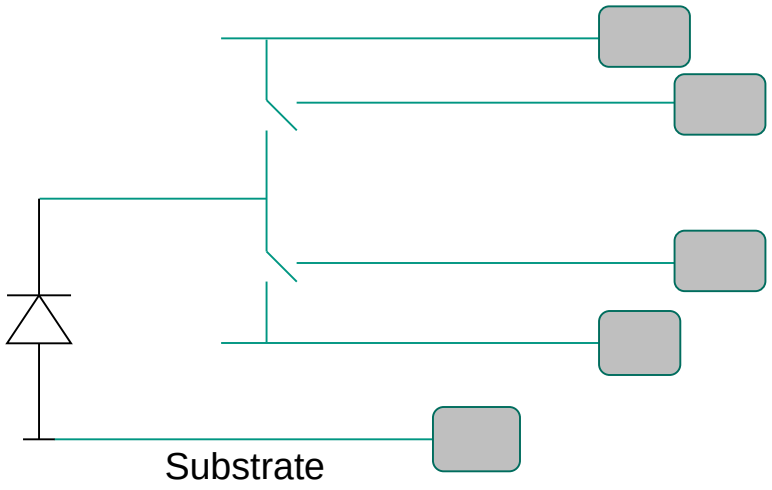
Analog pixel matrix with on-chip readout



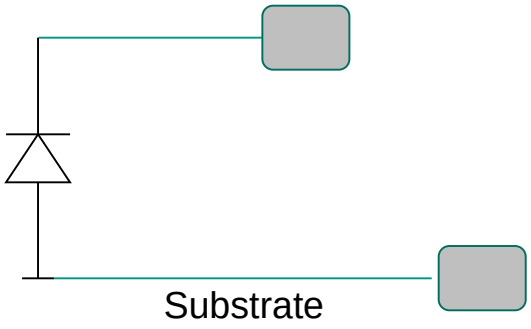
Test structures

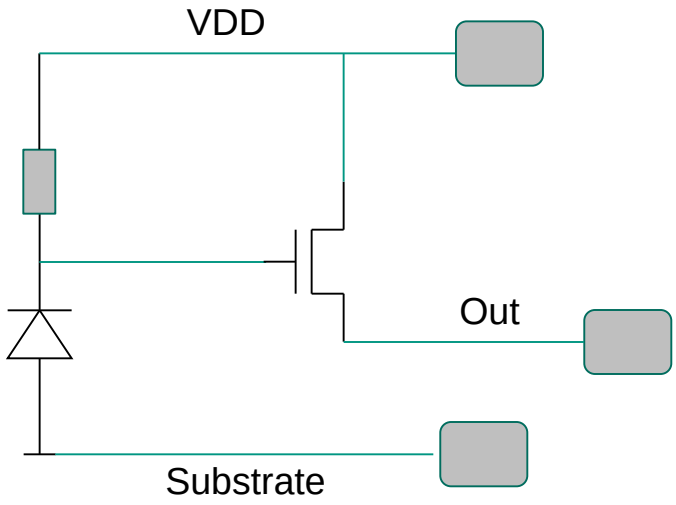
- Several test structures

- Structures for measurements of sensor capacitance

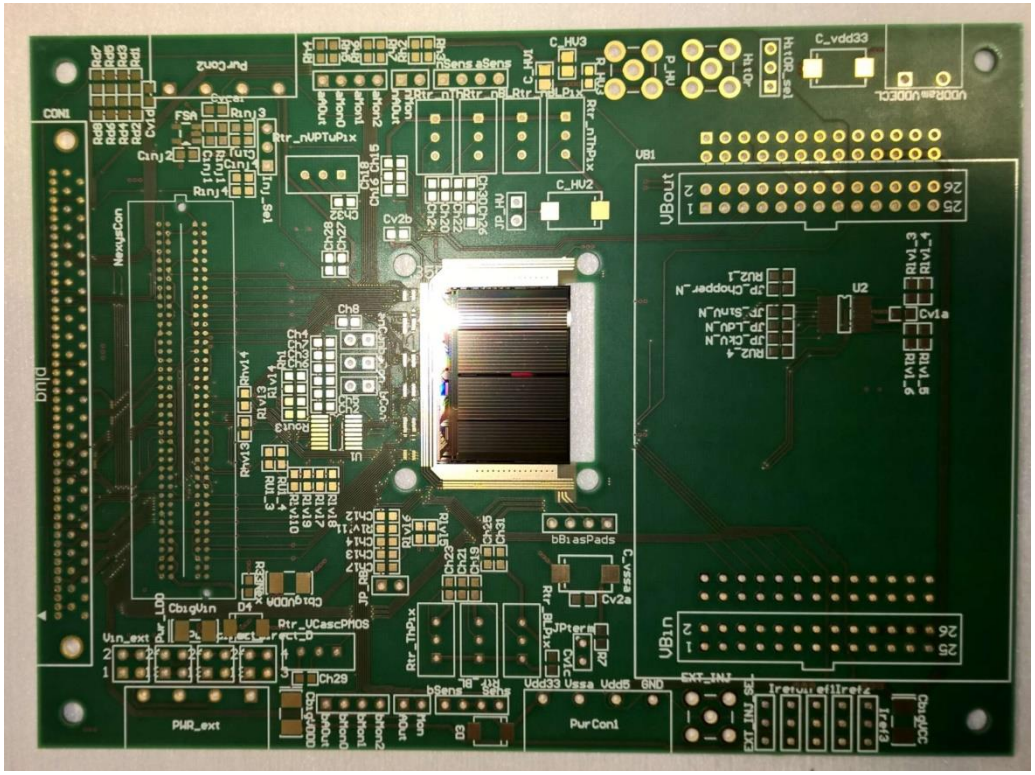


- Diodes for laser measurements
- Diodes with fast on-chip amplifier

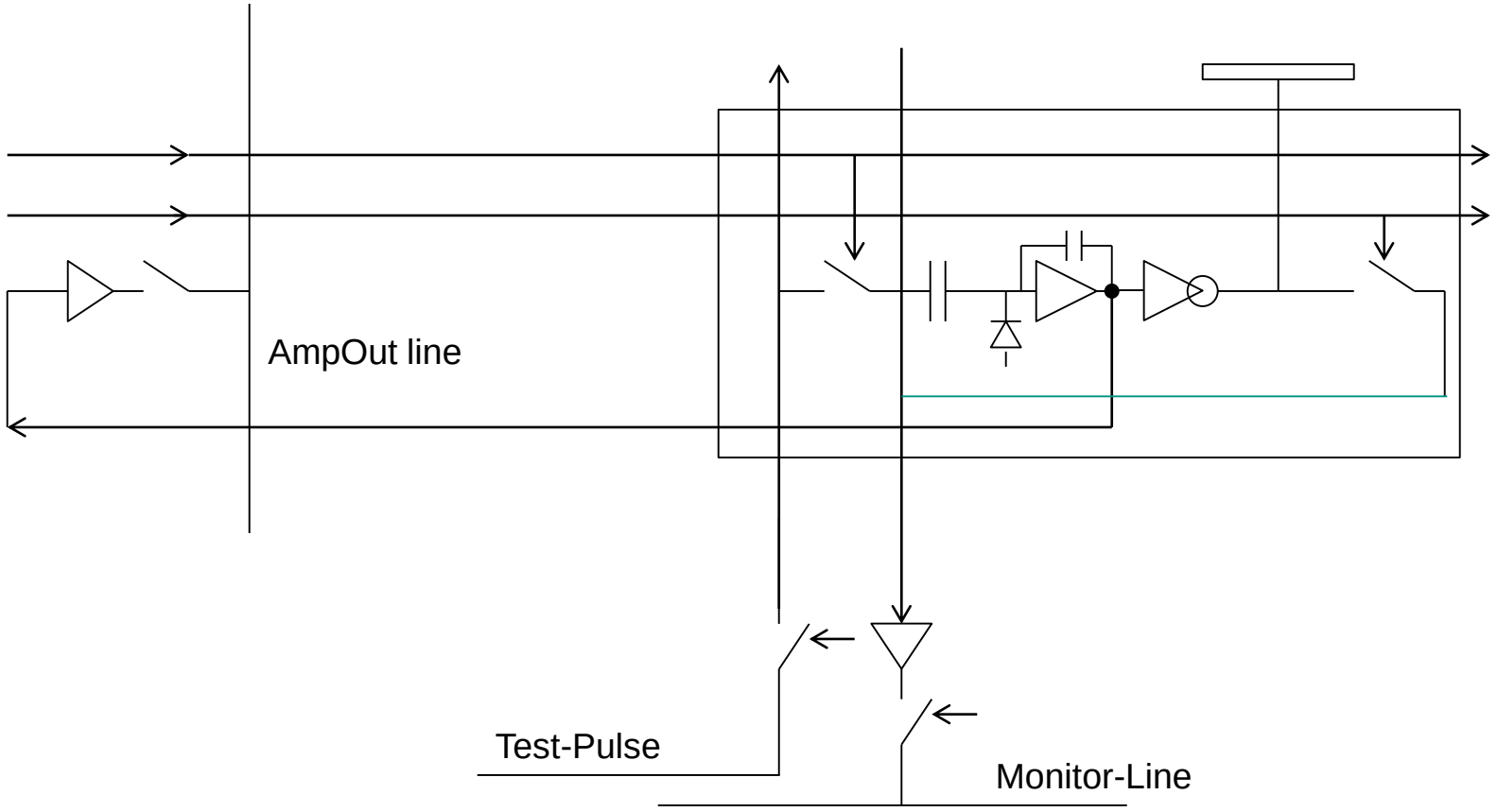


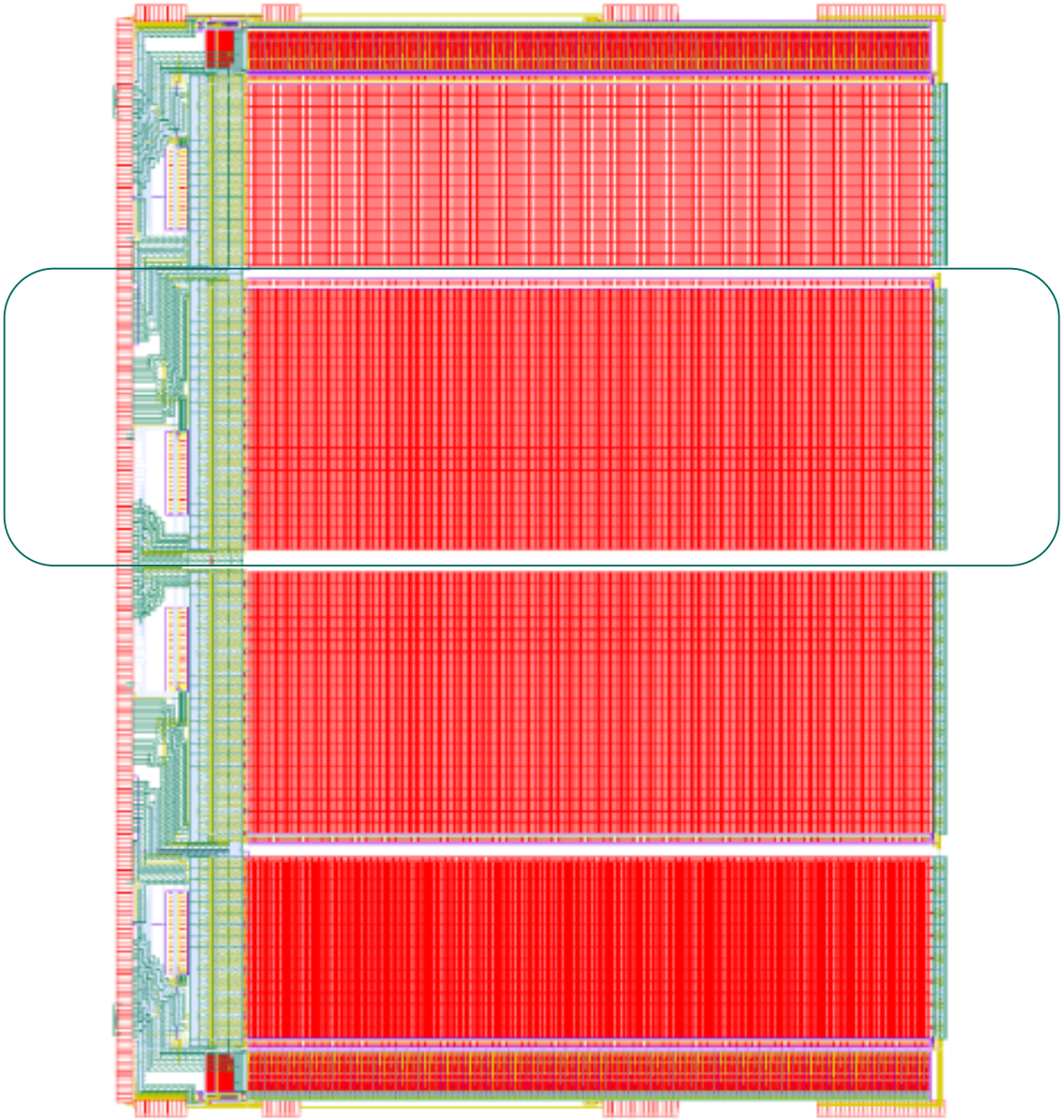


- PCB has been designed
- 1. HV sensor can be wire bonded alone
- 2. HV sensor with attached FEI4 can be both wire bonded
- PCB can be connected to GPAC/MultiIO system
- Nexys/Video evaluation board can be used for readout as well
- A version for Caribou system is planned

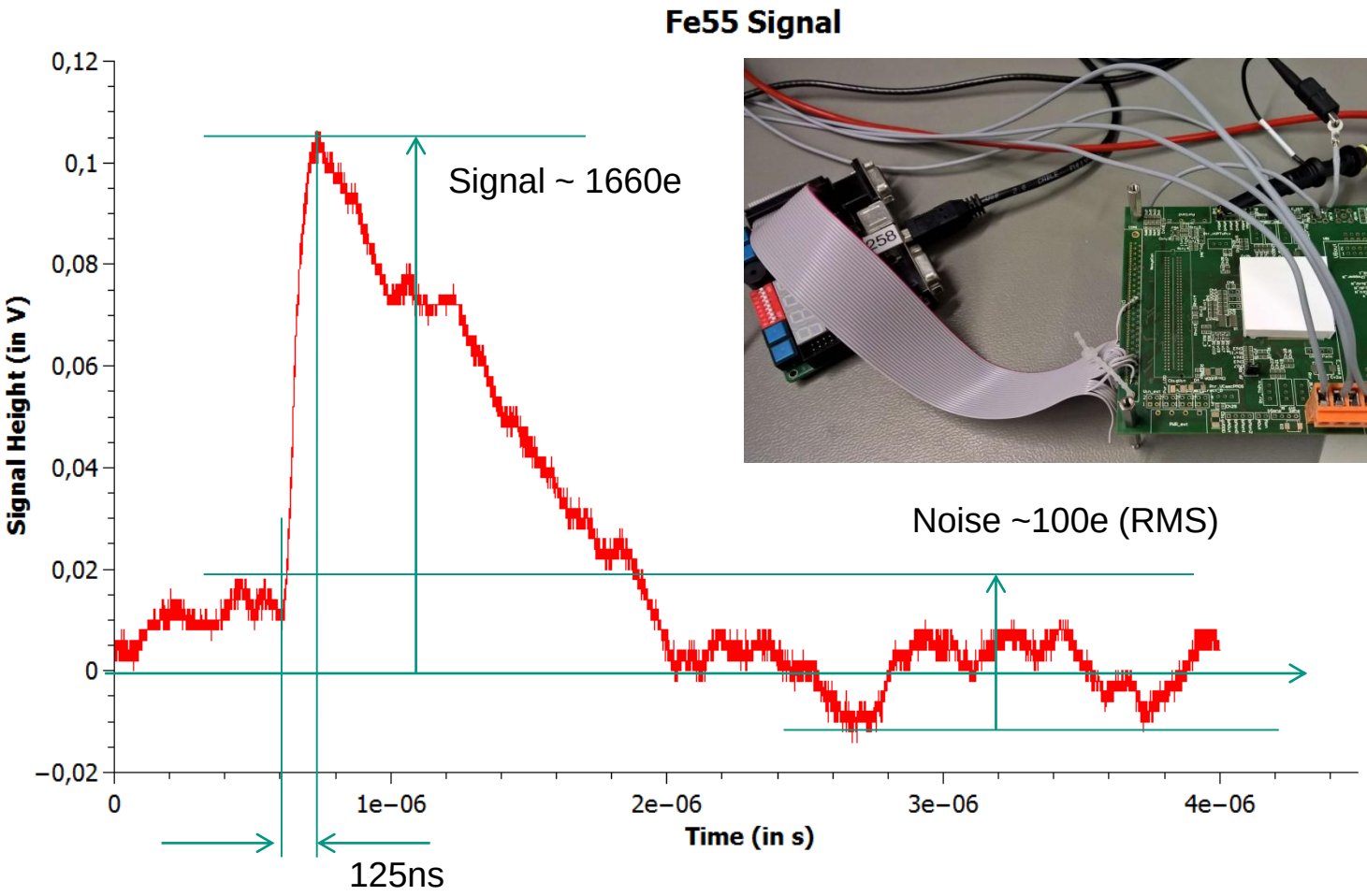


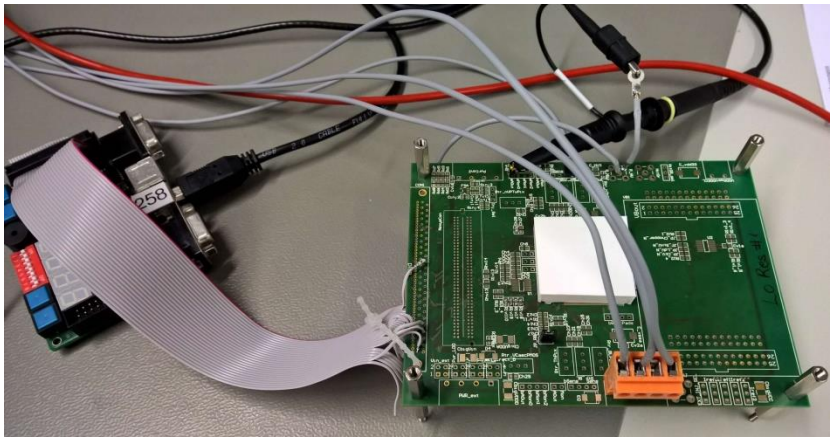
- Measurements done using AmpOut line of the NMOS analog matrix
- The chip is implemented on standard substrate – 20 Ω cm



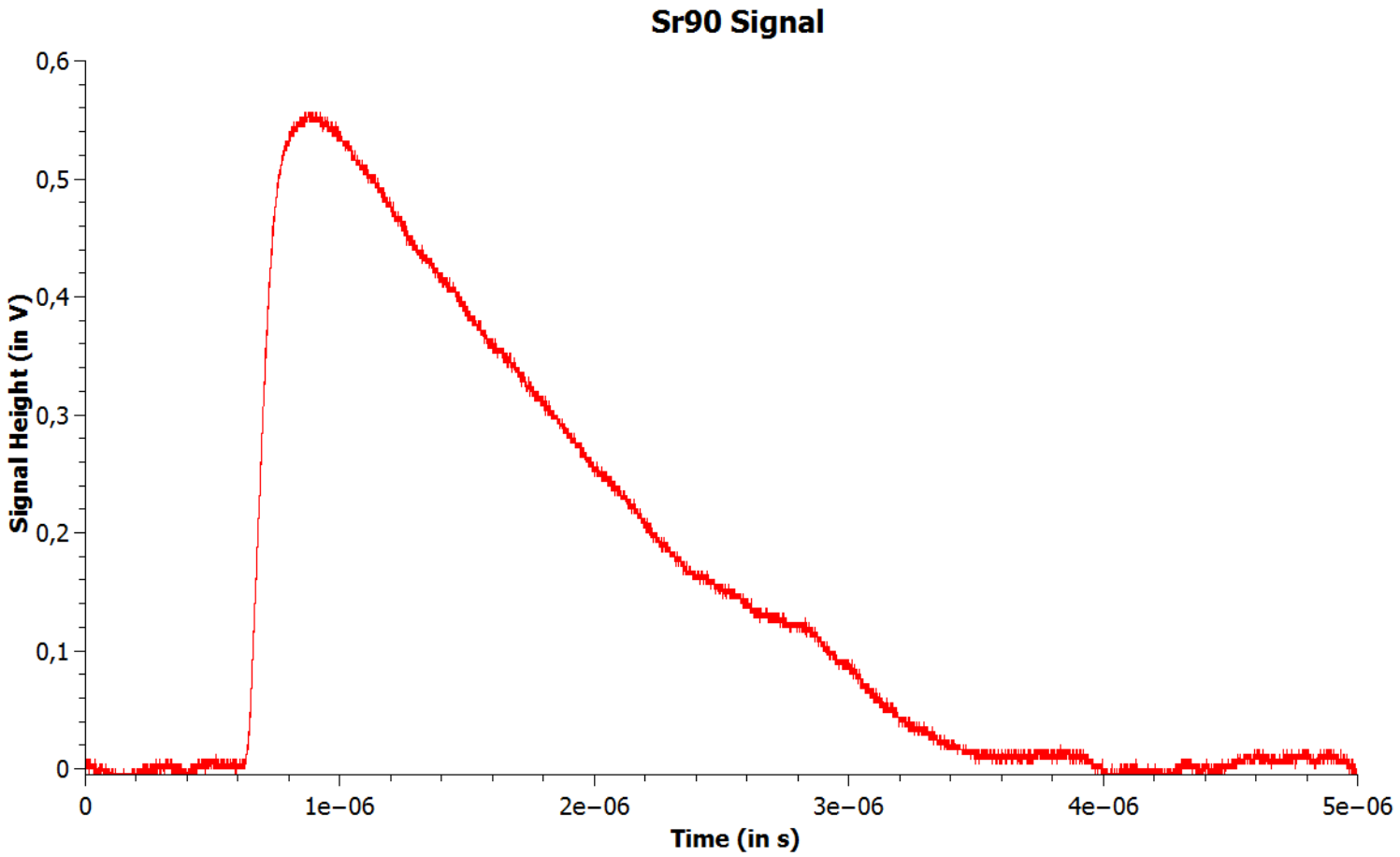


- Fe55 signal

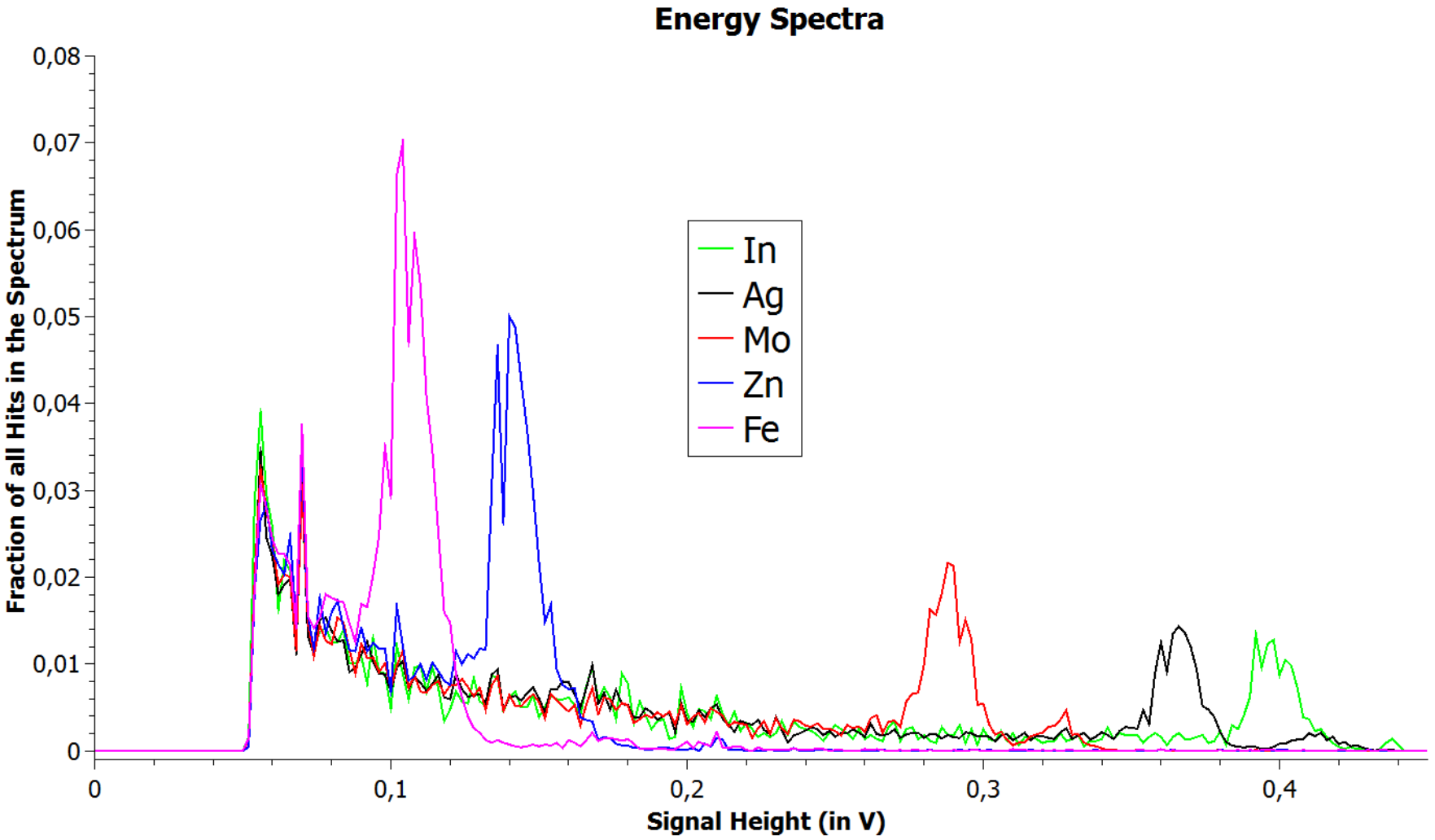

Fe55 Signal
Signal ~ 1660e
Noise ~100e (RMS)
125ns
Signal Height (in V)
Time (in s)
0,12
0,1
0,08
0,06
0,04
0,02
0
−0,02
0
1e−06
2e−06
3e−06
4e−06



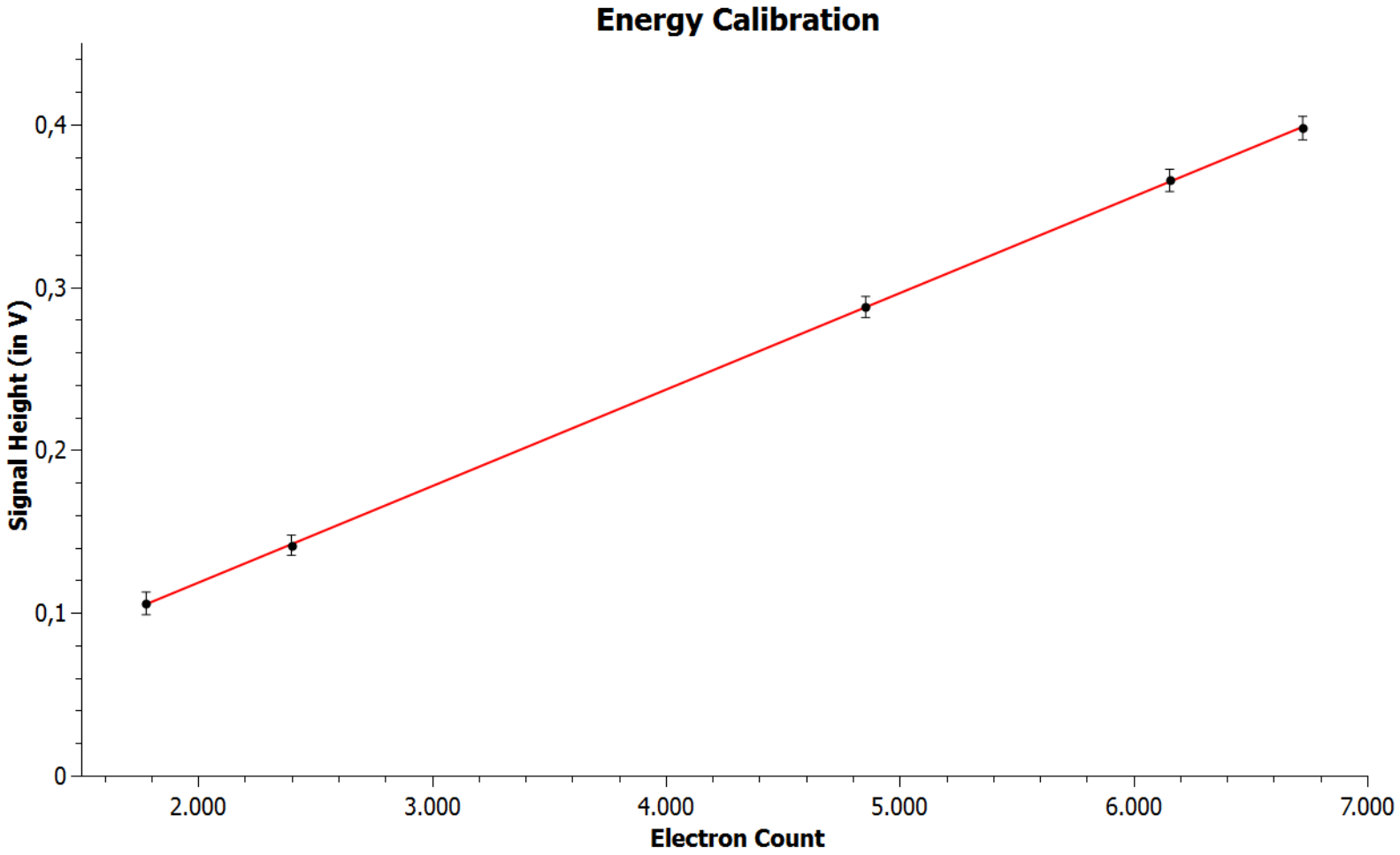
- Sr90 signal


Sr90 Signal
Signal Height (in V)
0,6
0,5
0,4
0,3
0,2
0,1
0
0
1e−06
2e−06
3e−06
4e−06
5e−06
Time (in s)

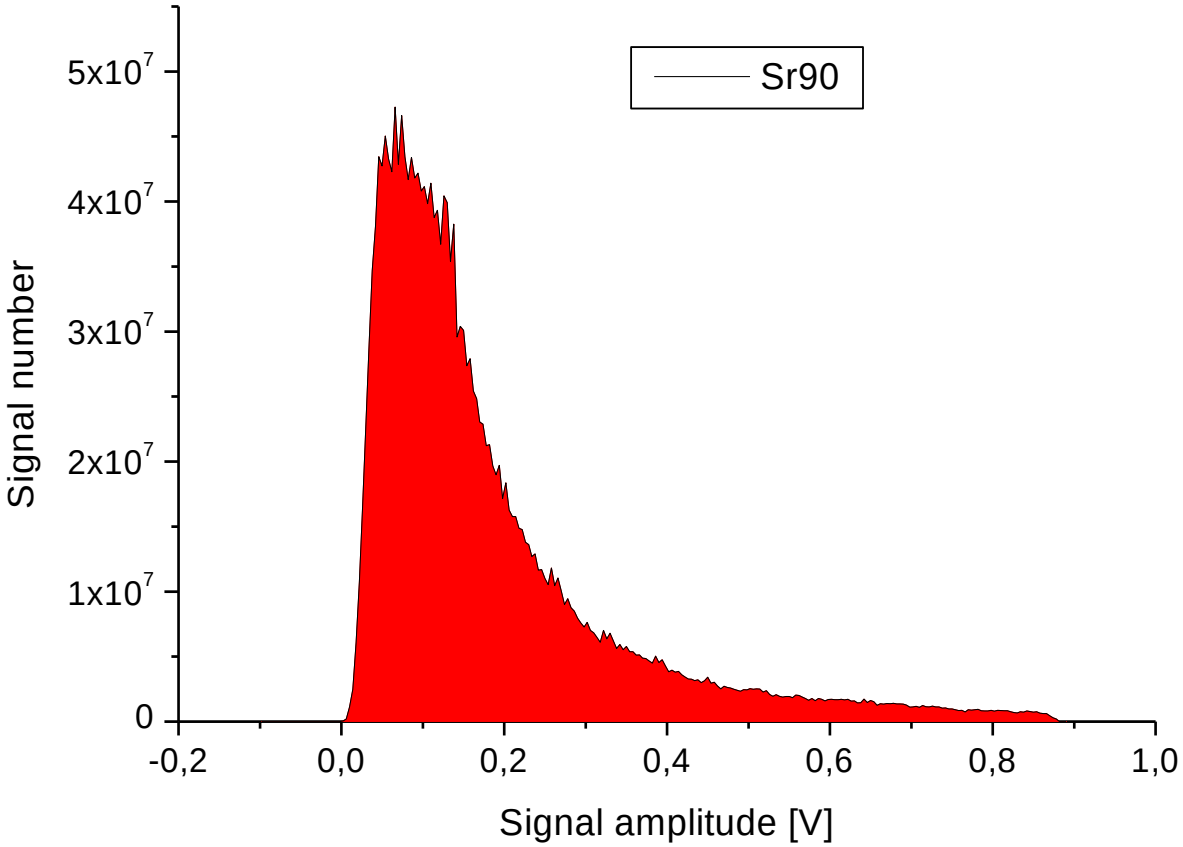
- Spectra of different elements (targets irradiated with x-ray tube)



- Energy calibration



- Sr90 spectrum, HV bias ~ 50V (possible up to 160V)



Conclusion

- The reticle size HVCMOS demonstrator for ATLAS in AMS H35 technology has been designed and fabricated
- The sensors have been produced on four different substrate resistivities: 20, 80, 200 and 1000 Ωcm
- The chips contain four pixel matrices
- The pixels can be readout by FEI4 capacitively or through bumps
- Several active pixel structures with and without comparator have been implemented
- Readout using a digital block at the periphery is also possible. There is 1-1 connection of every pixel to its digital cell at the periphery
- PCB has been designed, HV sensor can be wire bonded alone or with flipped FEI4
- PCB can be attached to GPAC/MultiIO system or readout using evaluation board Nexys/Video
- First results obtained with a sensor on standard substrate are very good