Monolithic CMOS ASIC Developments

11th "Trento" Workshop on Advanced Silicon Radiation Detector

Talk: HVCMOS 1 / 153

SLAC National Accelerator Laboratory

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U.S. DEPARTMENT OF ENERGY
Office of Science

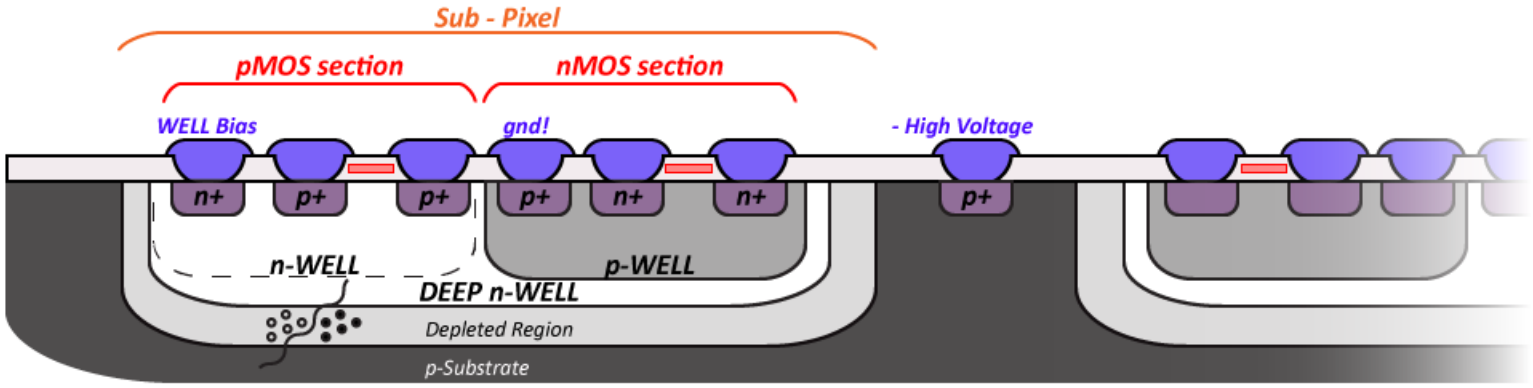
SLAC NATIONAL ACCELERATOR LABORATORY

Outline

- **Monolithic CMOS ASIC**
- **Motivations**
- **CHESS-2 : CMOS HV Evaluation for Strip Sensors**
- **COOL-1: CMOS fOr Outer Layers ASIC**
- **KPiXM: ECal read-out of Silicon Detector for ILC**

Monolithic CMOS ASIC

AMS 0.35µm HV



Sensor and read-out on the same substrate.

Motivations from a Science perspective

Monolithic technologies have the potential for providing higher granularity, thinner, intelligent detectors at lower overall cost:

- Significantly lower material budget
  - eliminate the need for bump bonding or other challenging interconnect methods
  - can be thinned to less than 100um
- Smaller pixel size
  - not limited by bump bonding
- Lower costs
  - can be implemented in standard commercial technologies

	Hybrid	Depleted MAPS	
		HVCMOS	HRCMOS
collection speed	fast (drift)	fast (partial/drift)	fast (drift)
cost	high	low	low
material	high	low	low
pixel size	medium	small	small
signal	high	low	high
In pix processing	high	Medium/high	high

Monolithic technologies for Particle Physics Application

SLAC

We have an interest in monolithic technologies for applications in Particle Physics:

- ATLAS Strips (**CHESS2** in collaboration with UCSC)
- ATLAS Outer Pixels (**COOL**)
- ILC SiD Tracker and Ecal (**KPiXM**)

CHESS2 - Objectives

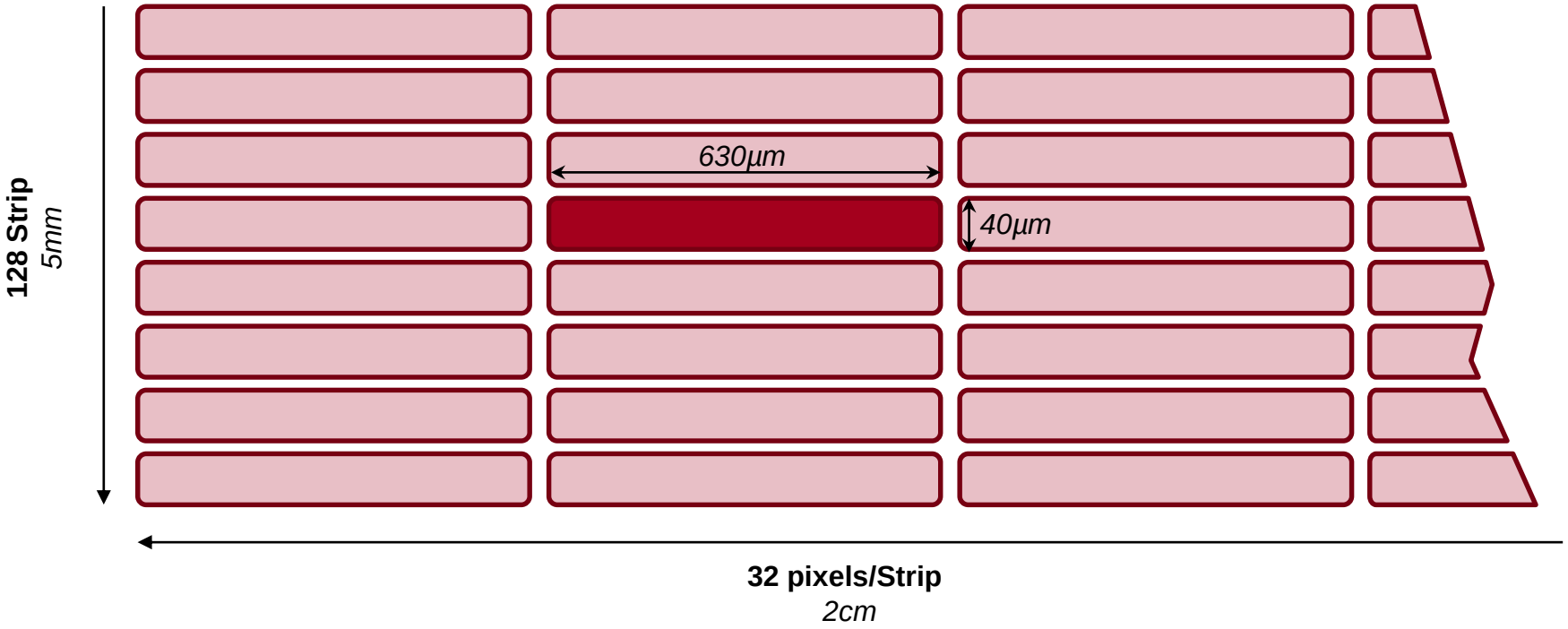
- **Demonstrate HVCMOS as a viable solution for ATLAS strip detector.**
  - *Record hits on full reticle sensor 128 strips – 32 sub-pixels*
  - *Amplify, filter and discriminate signal*
  - *Encode hit position in sensor and send to external readout electronics*

- **Further investigate performances of HVCMOS MAPS sensors**
  - *Size close to final sensor : test beams, module assembly, etc..*
  - *Evaluate sensors with different substrate resistivity 20, 50-100, 200-300, 600-2000 Ohm-cm.*
  - *Study radiation hardness using test structures.*
  - *Characterize the pixel arrays with different methods, include edge-TCT and beam tests*
  - *Large scale effects: common noise, cross-talk, power drops etc..*

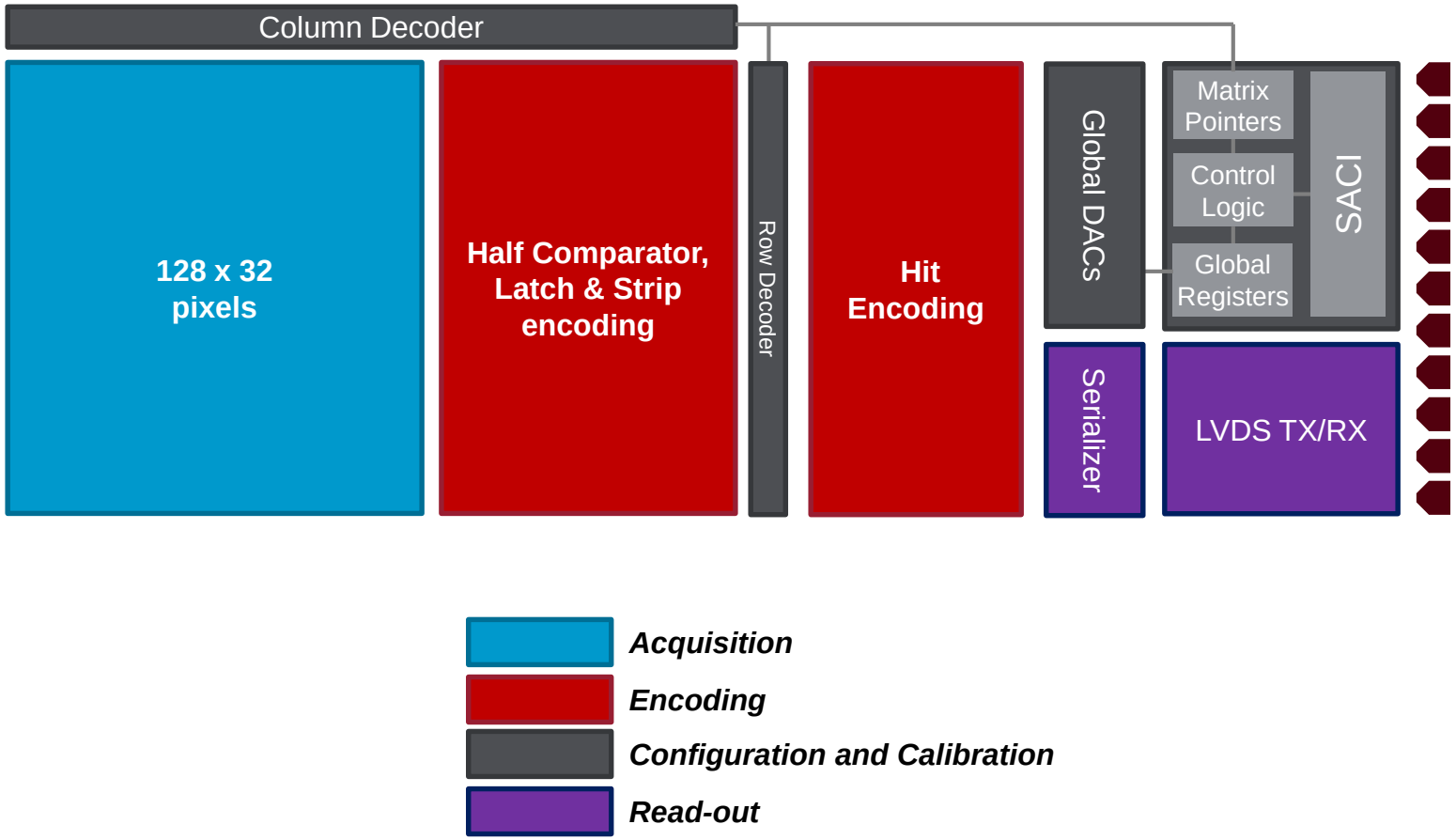
CHESS2 - Specifications

	Specs	*Comments*
Substrate resistivity	20Ohms to 1000Ohms	*Minimal MIP from from 1500e to 4000e*
Substrate high voltage bias	120V	*40% more charge vs 60V*
Pixel size	40µm x 630µm	*400fF det. capacitance*
Number of pixel per strip	32	
Number of strips	128	*Factor ~2 improvement in r-phi resol.*
Timing resolution	25ns	
Maximum number of hits per strip	1 + flag	
Maximum number of hits per 128 strips	8	
Readout speed	320MHz	
Number of wire bonds	28/128strips (data only)	*x5 reduction*
Additional constraint	Rad-hard design	*Periphery: dead area 4mm - shorter strips*

CHESS2: Strip sensor size

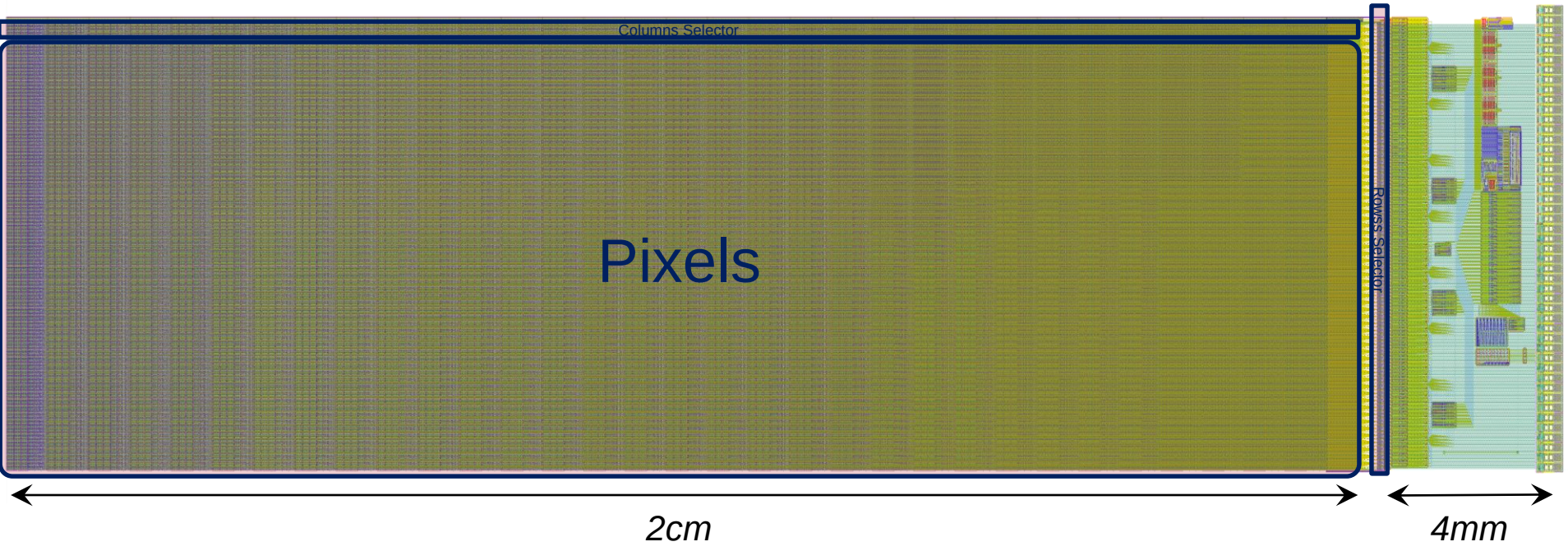


CHESS2: ASIC Architecture



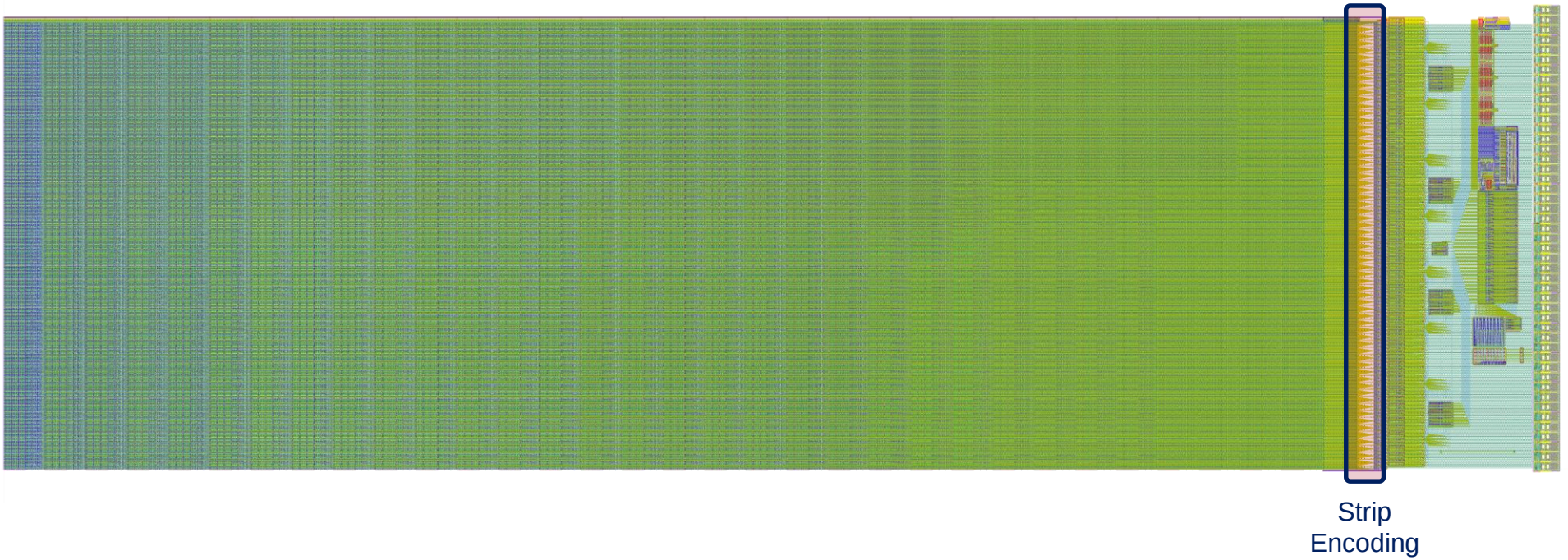
CHESS2 Floor Plan

Pixels – Row, Column selectors



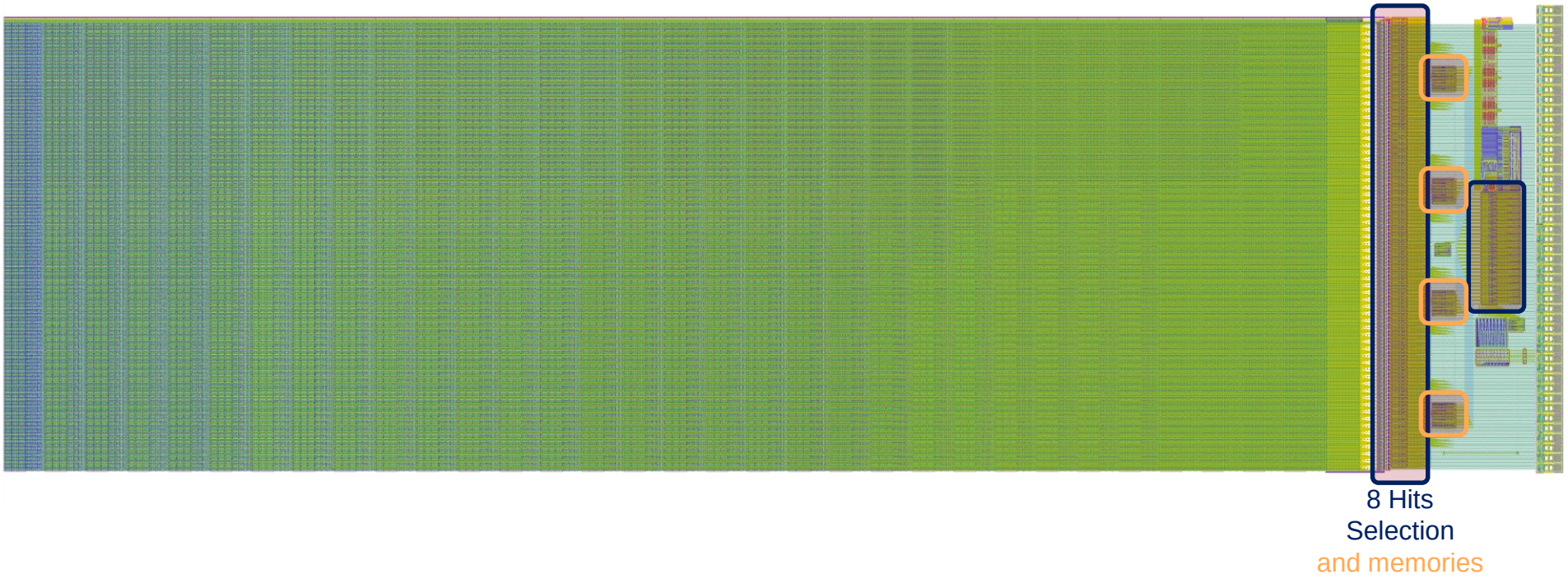
CHESS2 Floor Plan

Strip Encoding



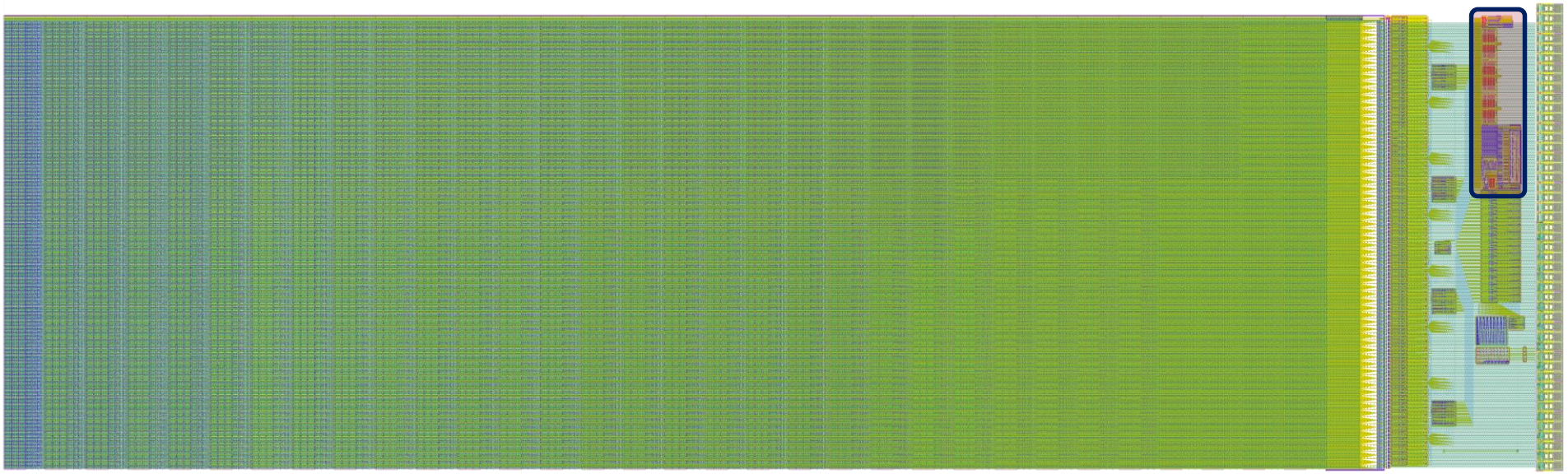
CHESS2 Floor Plan

8 Hit Encoding Logic & Memories



CHESS2 Floor Plan

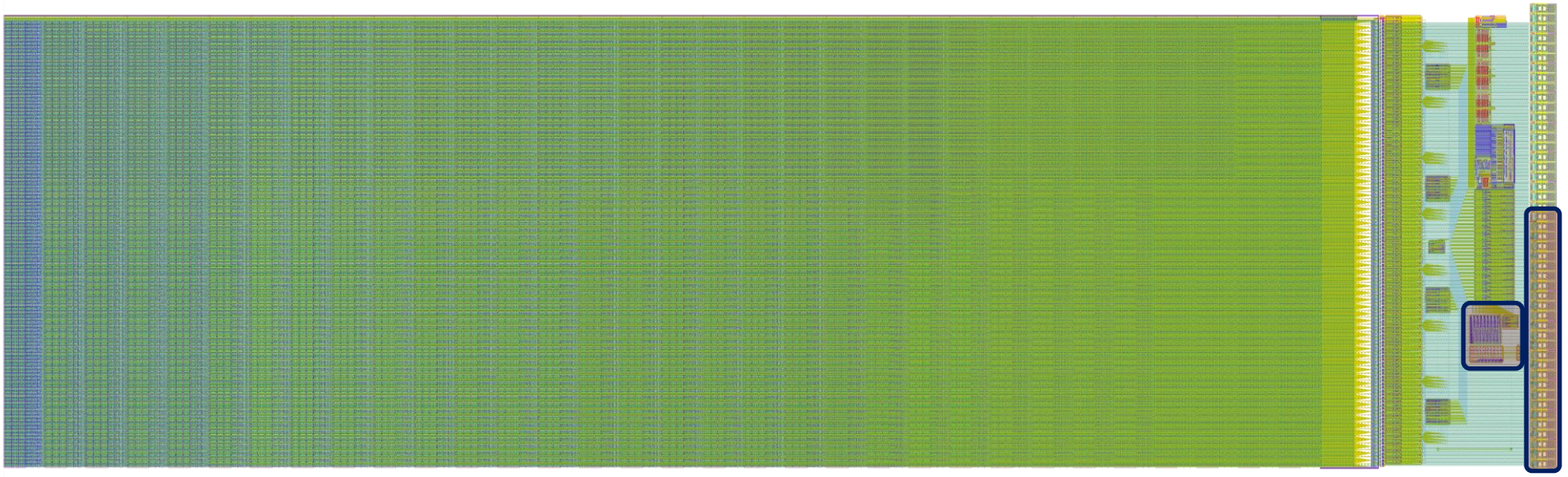
SACI – Registers – Current sources



SACI &
Current sources

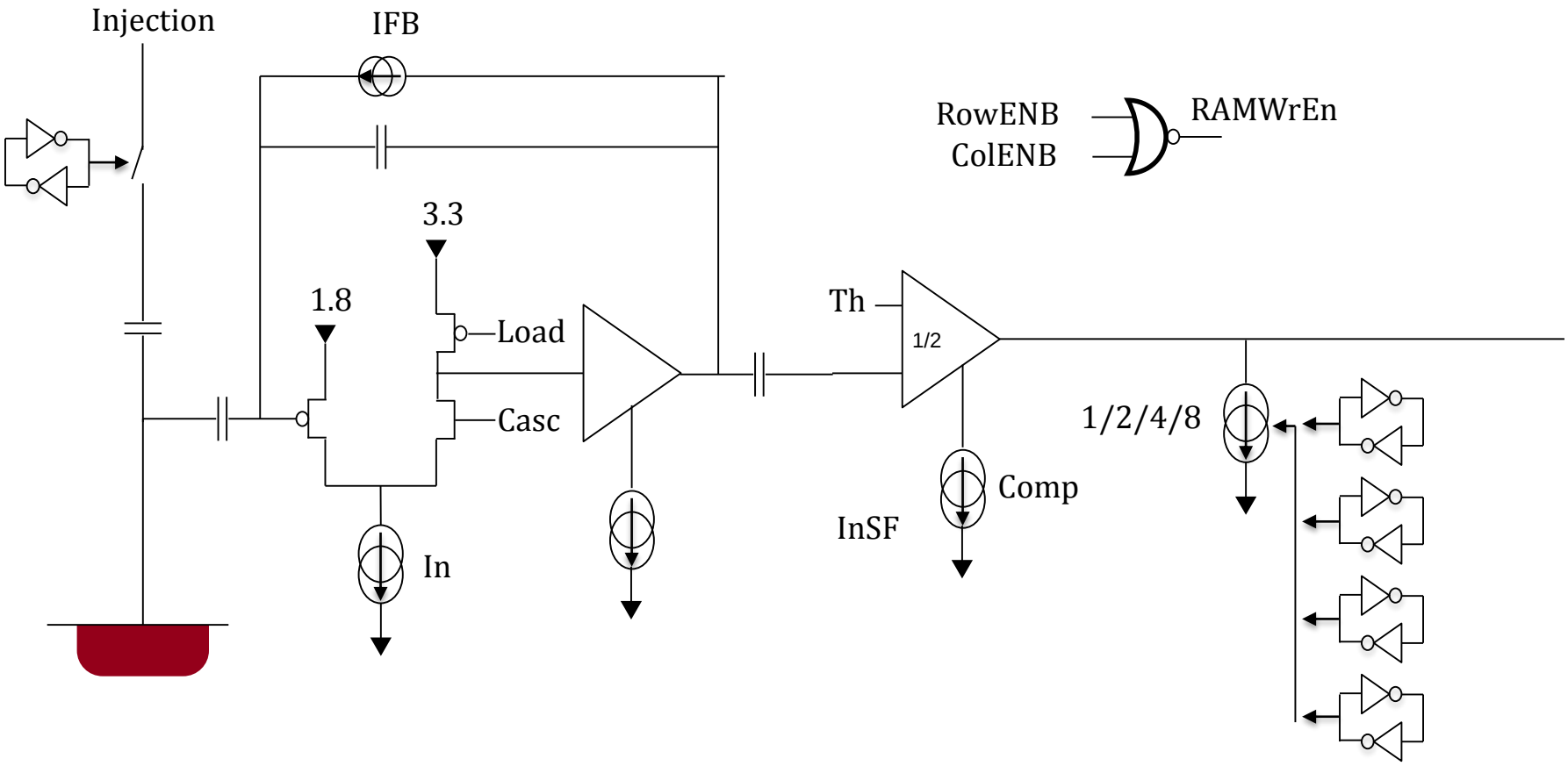
CHESS2 Floor Plan

Serializer – LVDS TX/RX

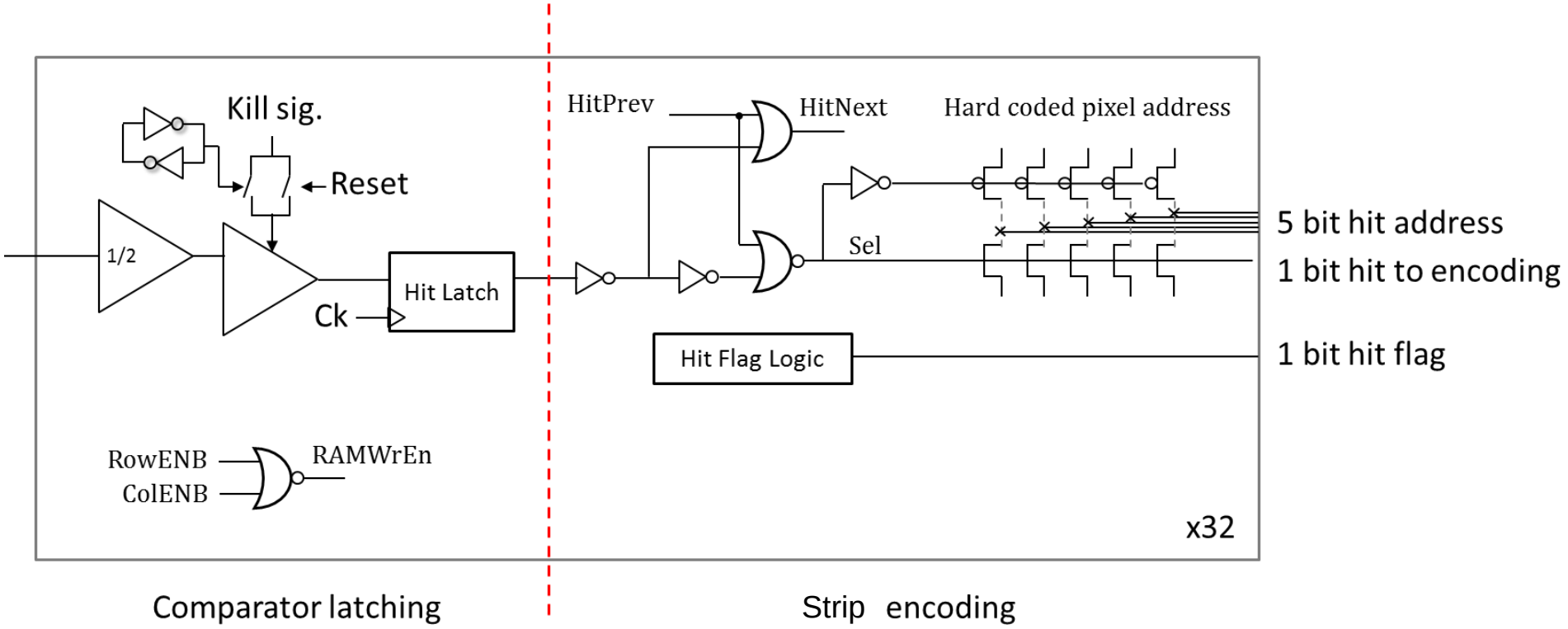


Serializer & LVDS TX/RX

CHESS2: Pixel



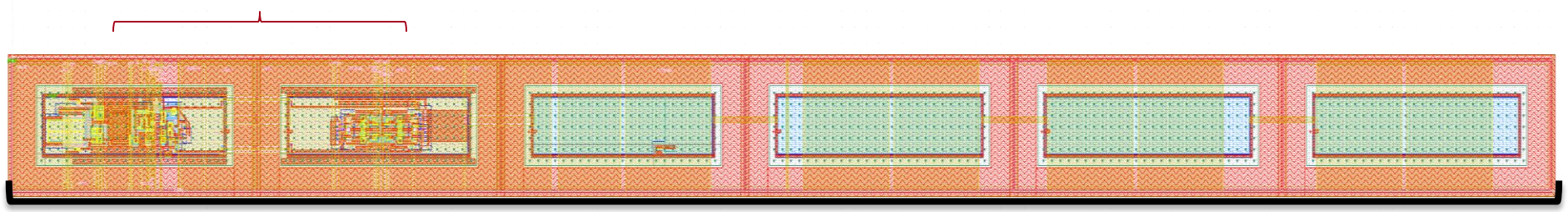
CHESS2: Pixel periphery schematic



- Encode the column address of the first hit and raise a flag if a double hit has occurred on the same strip

CHESS2: Pixel Layout – 630µm x 40µm

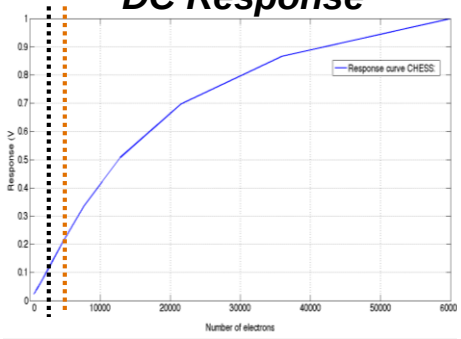
- Amplifier
- Half comparator
- Charge injection
- Pixel Selection
- Comparator Trimming Memory



- 6 connected NWELLs
- 50% diode fraction
- P-contact around each NWELL
- 120V rules

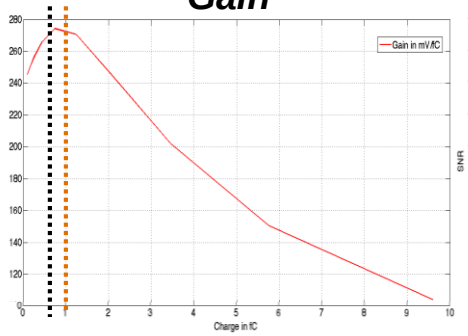
CHESS2: Simulated Pixel Behavior

DC Response



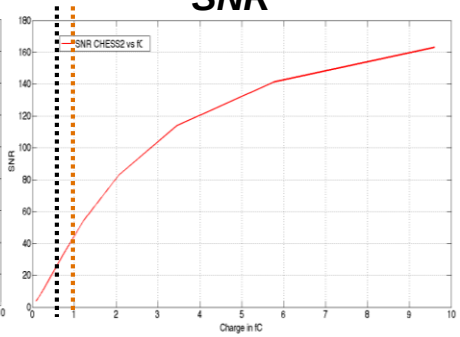
75mV @ 20Ω
200mV @ 600Ω

Gain



~270mV/fC

SNR

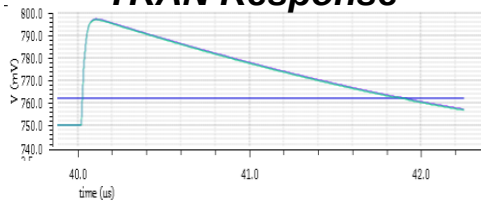


10 @ 20Ω
40 @ 600Ω

1MIP@ 20Ω
1MIP@ 600Ω

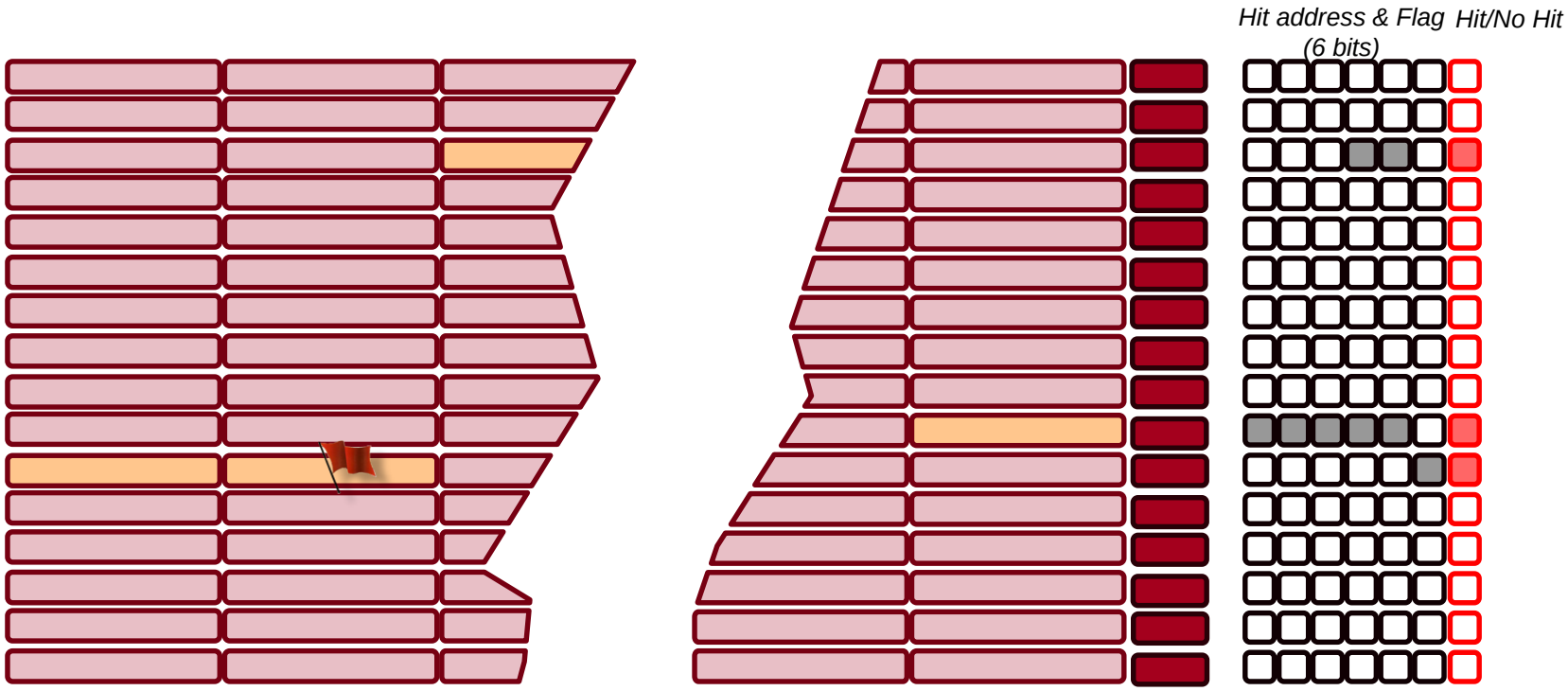
Equivalent charge at different substrate resistivity

TRAN Response



Less than 10ns walk time
~10ns peak time

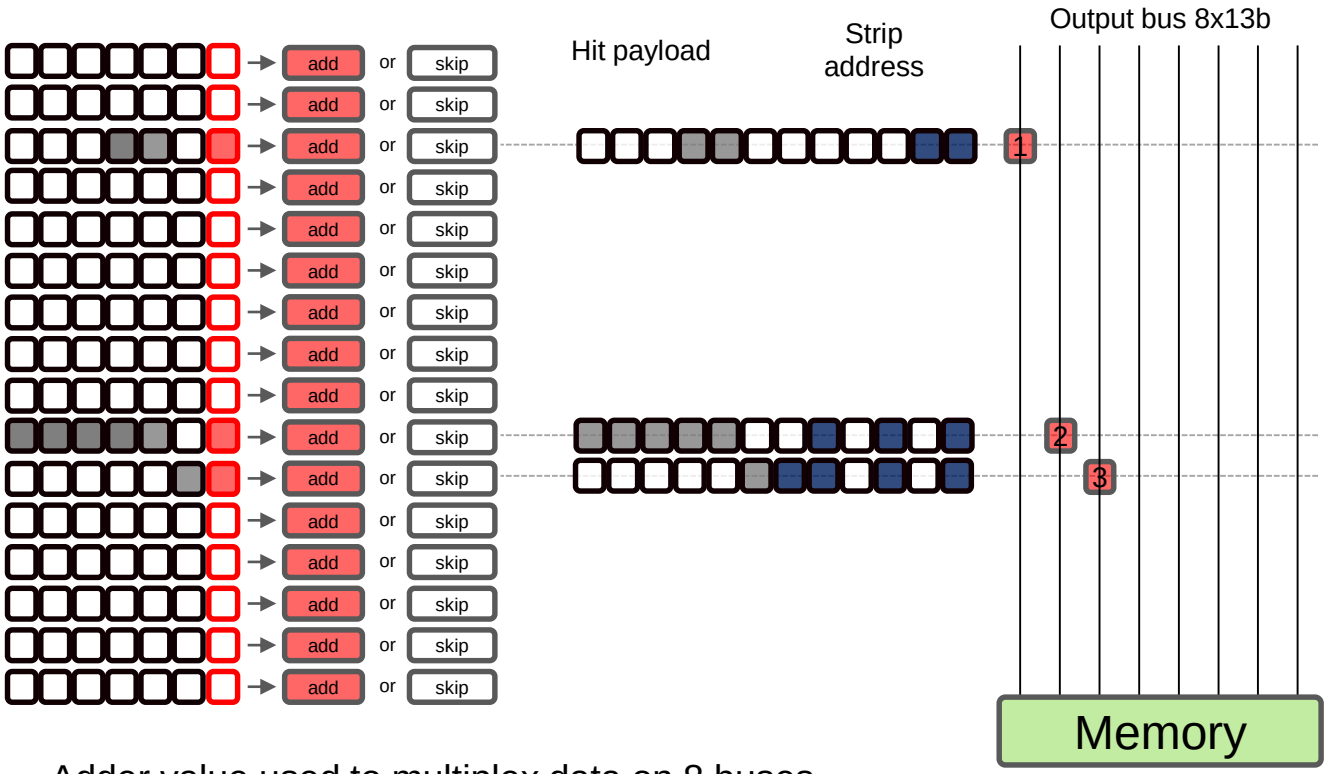
CHESS2: Strip Encoding



1 hit per strip + flag in case of multiple hits. 5 + 1 bit

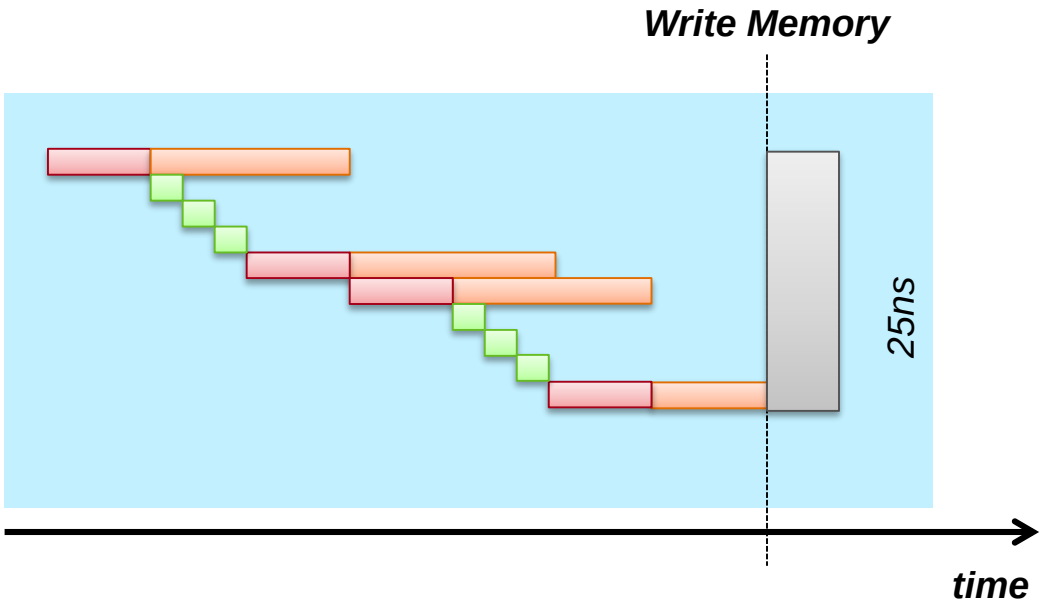
8 hits maximum per 128 strips. 7 bit

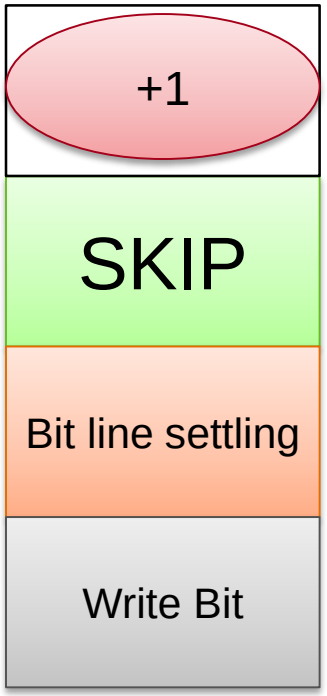
CHESS2: Hit Encoding – Fast Skip Concepts



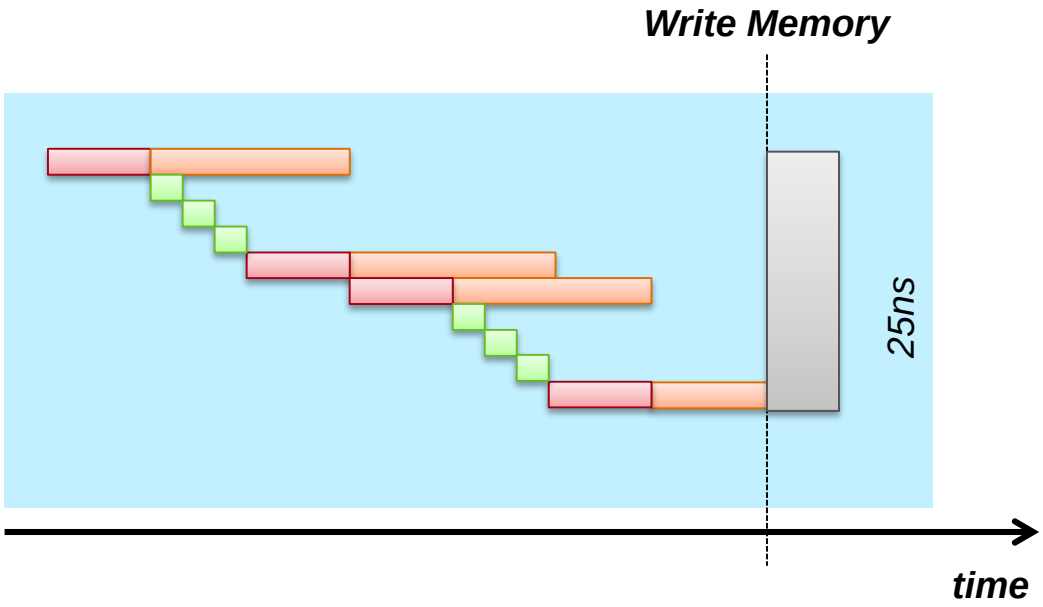
- Adder value used to multiplex data on 8 buses
- Overflow protection in 3b adder: 8 hits maximum
- Adder are slow *(up to 1ns in worst case speed)*
- *Huge load on the bit lines (127 switch off-capacitance + 5mm line capacitance)*

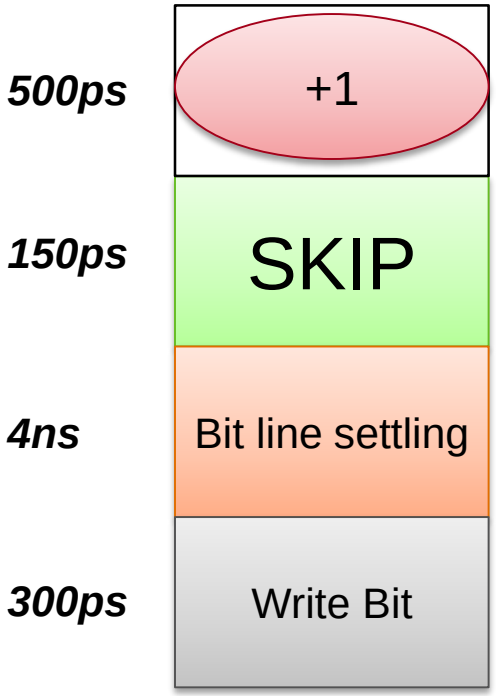
CHESS2: Hit Encoding – Fast Skip Concepts





CHESS2: Hit Encoding – Fast Skip Concepts

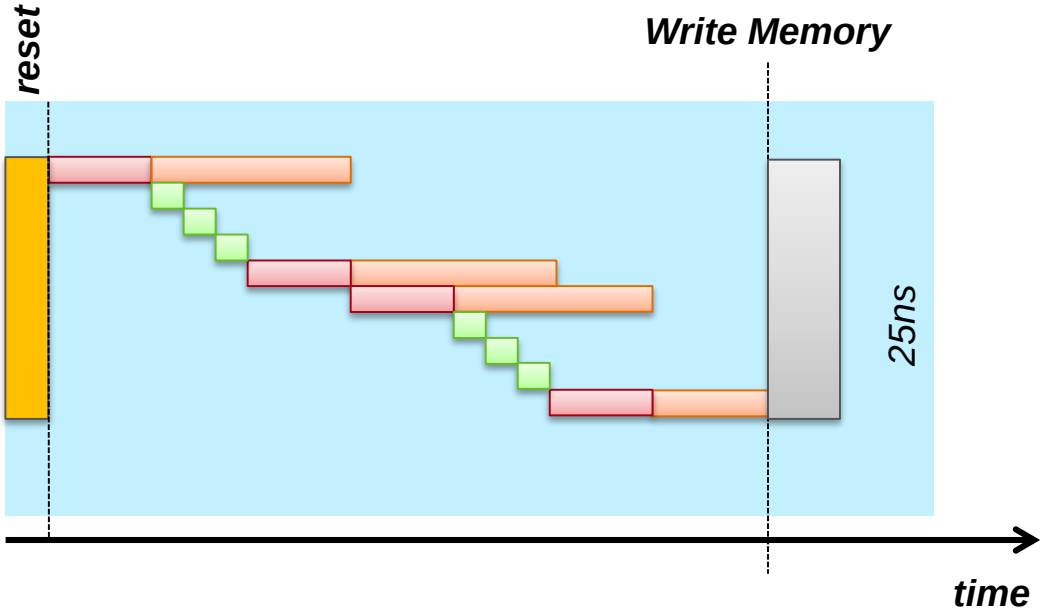


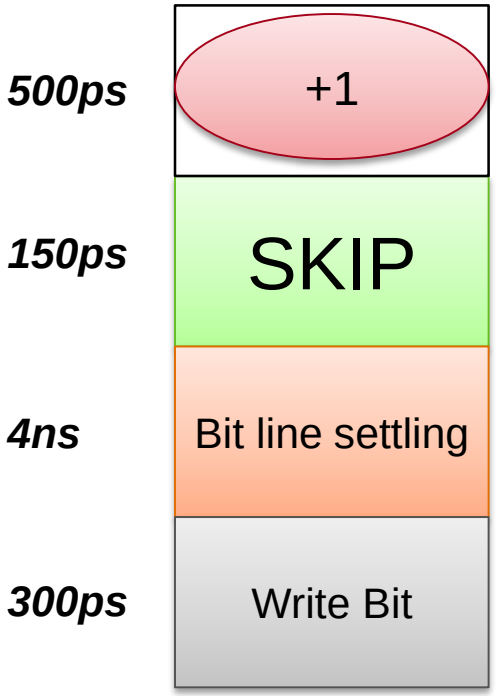


- Time to get the bit lines ready is based on number of hits
- Can be as high as 64ns if are all hits.

We are interested in the first 8 hits so the worst case using this architecture is when we have no hit on the first 120 rows and hit on the last 8 rows -> 22ns

CHESS2: Hit Encoding – Fast Skip Concepts





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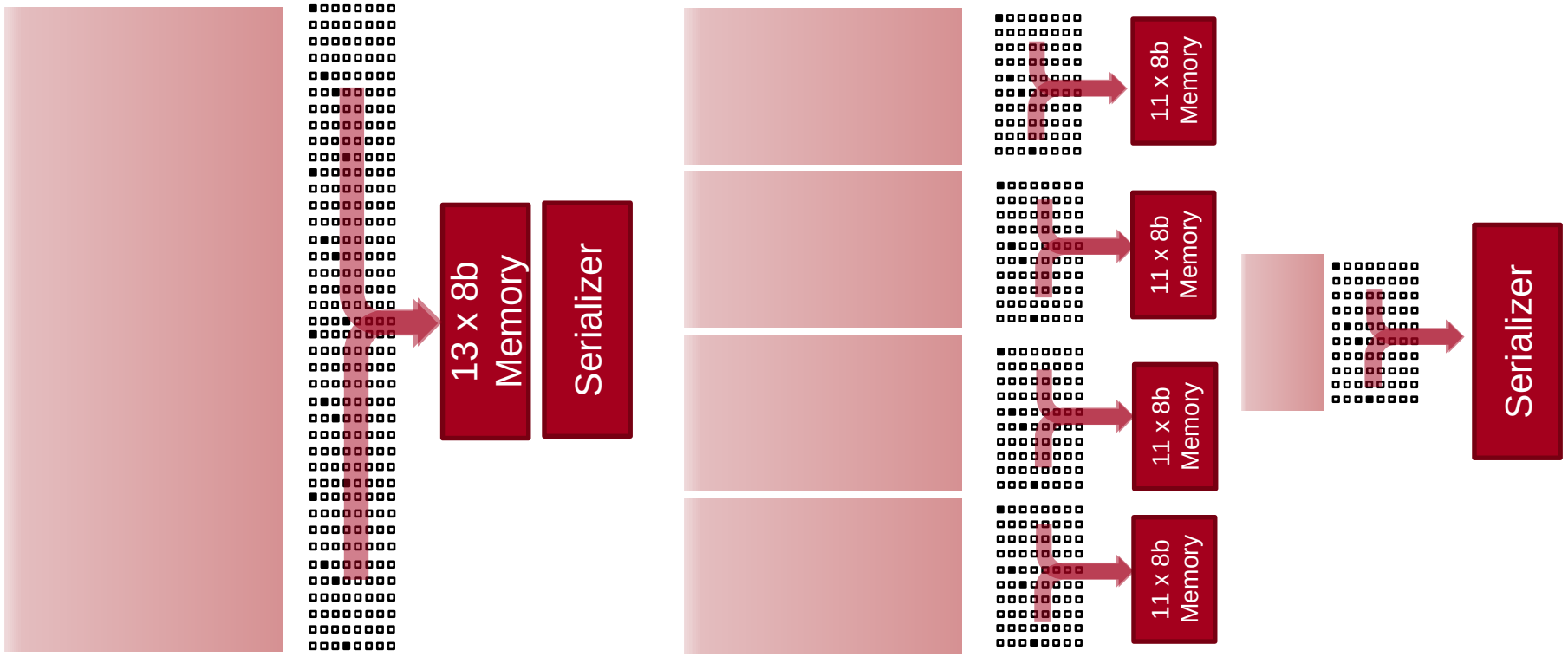
We are interested in the first 8 hits so the worst case using this architecture is when we have no hit on the first 120 rows and hit on the last 8 rows -> **22ns**

→ Avoid ghost from previous cycle introducing a **reset phase**

CHESS2: Hit Encoding – Fast Skip Concepts

Find first 8 hits in 128 rows

2x Find first 8 hits in 32 rows *(2 stage in a pipeline-like behavior)*



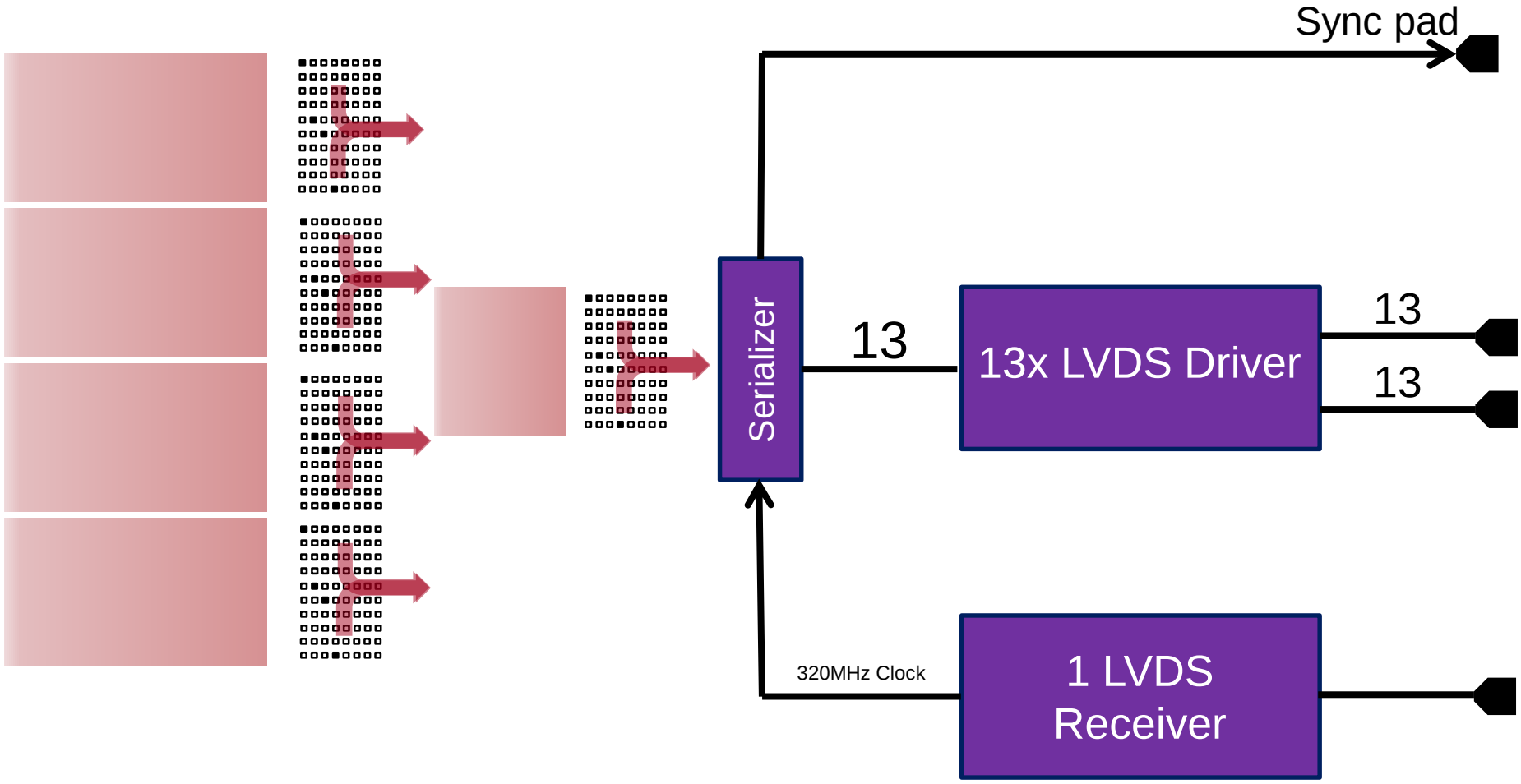
Worst case scenario:

22ns

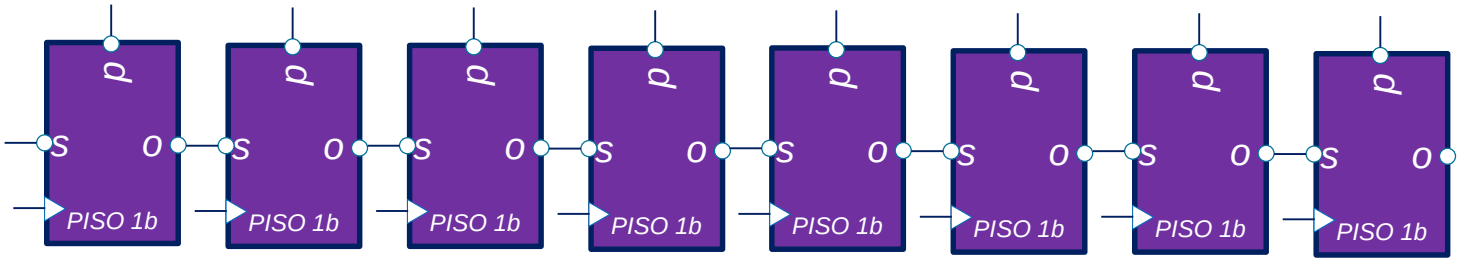
7.6ns

CHESS2: Fast Adder x32 (Layout)

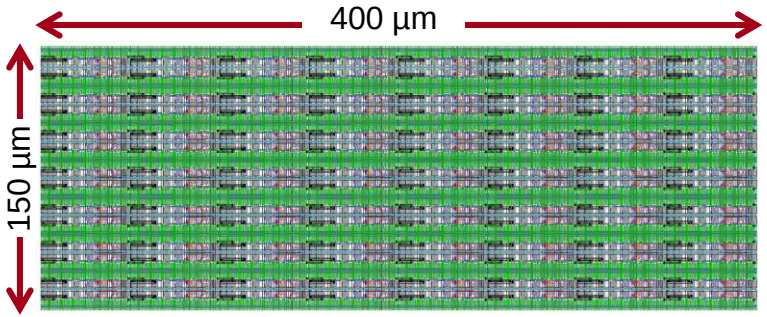
CHESS2: LVDS TX/RX and Sync



CHESS2: Serializer



- 8 x 13 1bit PISO Cell.
- Parallel input with 25ns period (synchronized to the 40MHz external clock).
- Serial Output has 3.125ns period (synchronized to the 320MHz external clock).



SLAC ASIC Control Interface (SACI)

Serial Interface with handshake protocol

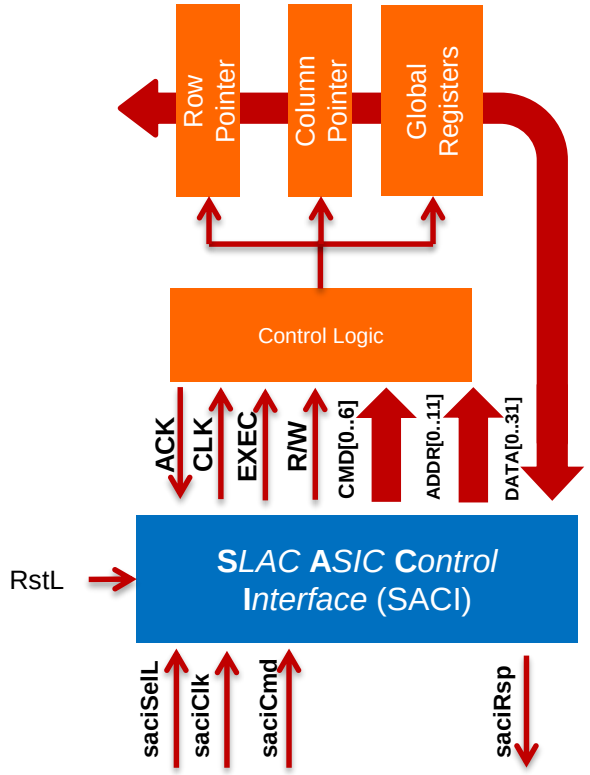
5 Signals

- 3 shared: *saciClk*, *saciCmd*, *saciRsp*.
- 1 dedicated select line per slave: *saciSelL.*
- 1 Reset Line (*RstL*) can be shared with the ASIC Global Reset.

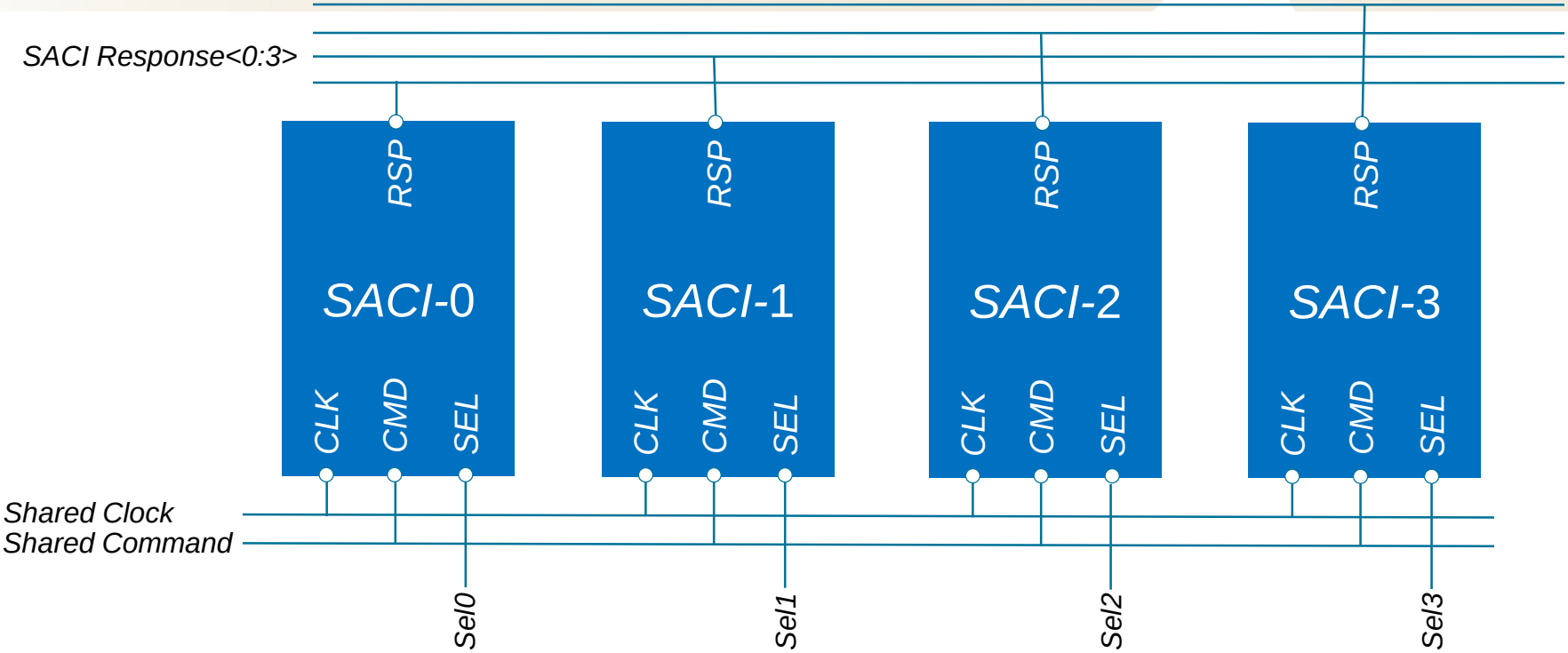
- Operated between 0V and 3.3V
- Allows multiple SACI on same bus (parallel mode).

SACIcmd (serial signal):

–

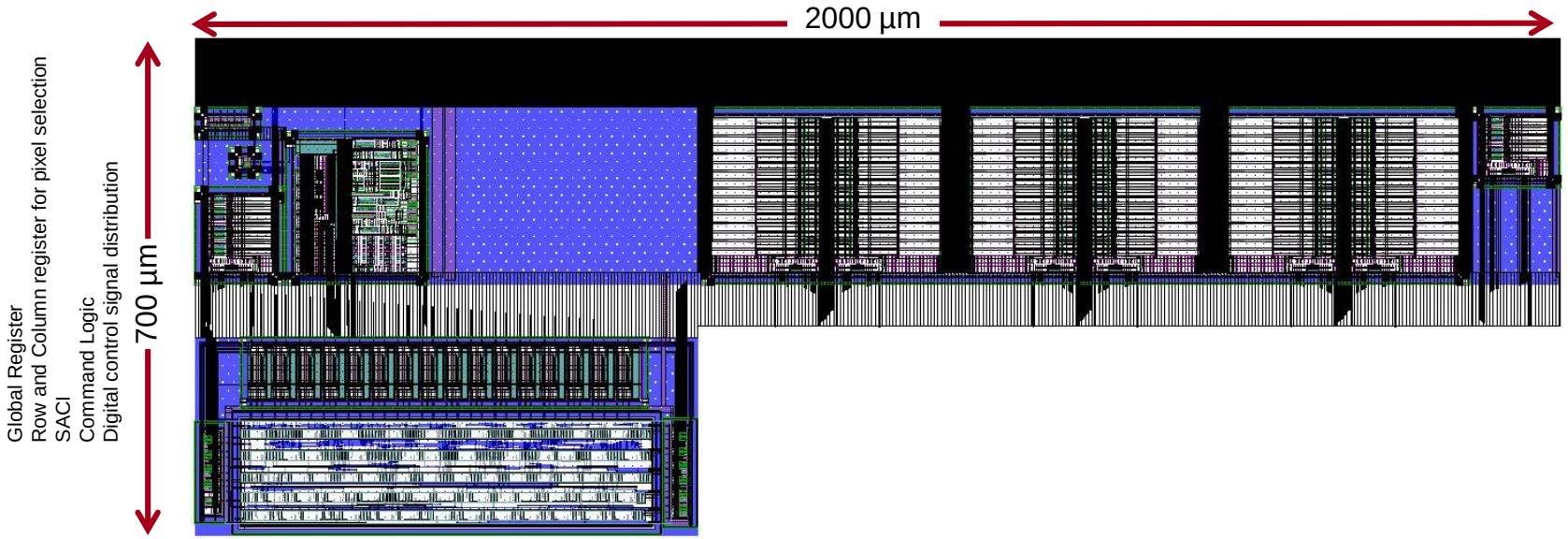


SACI – Multiple ASIC connection



Response line can be shared if only 1 SACI is selected when the command arrives.

Control Unit



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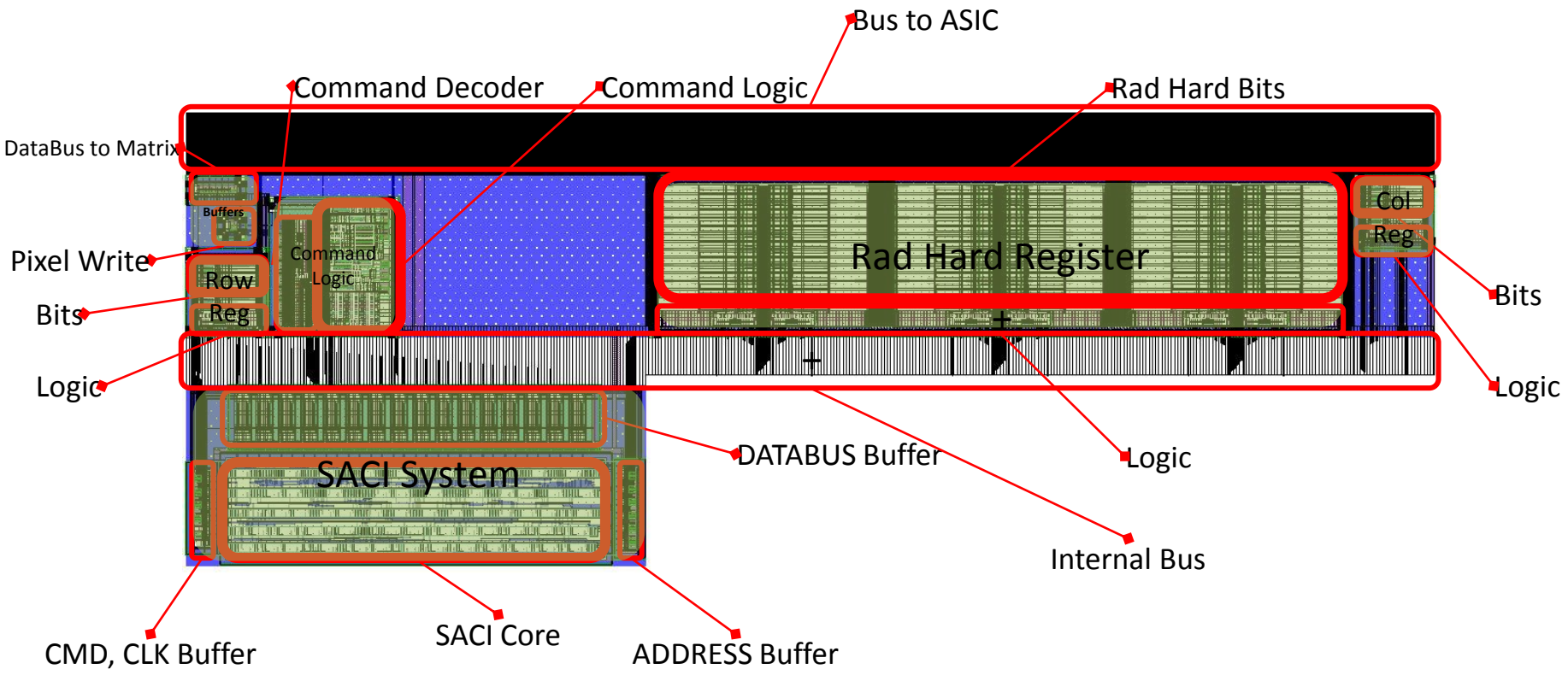
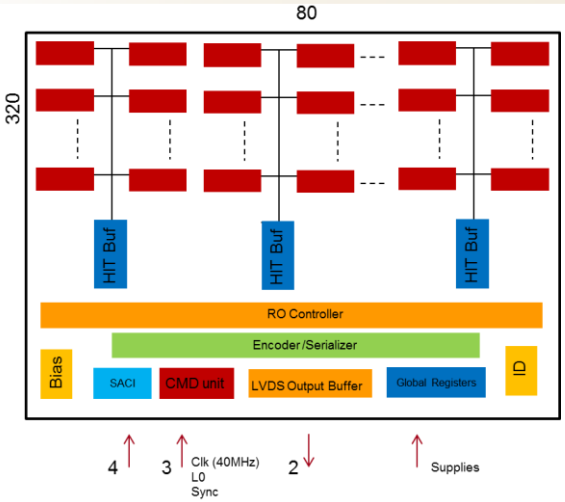


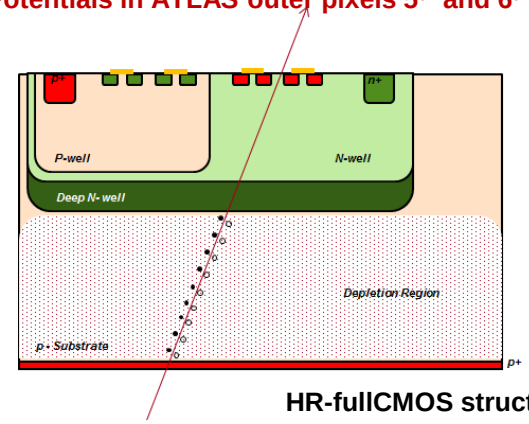
COOL-1: CMOS fOr Outer Layers ASIC

Can we build a full read-out system that meets the ATLAS pixels requirements (at least for the outer layers)?



Tentative goals	COOL-1
Pixel size	250x50 μm^2
Array	320x80
Full Size	reticles
Max. Signal	~10ke$^-$
Effective ENC	<120e$^-$
DC Current cons.	~ 20μA/pix

Large Potentials in ATLAS outer pixels 5th and 6th layers!



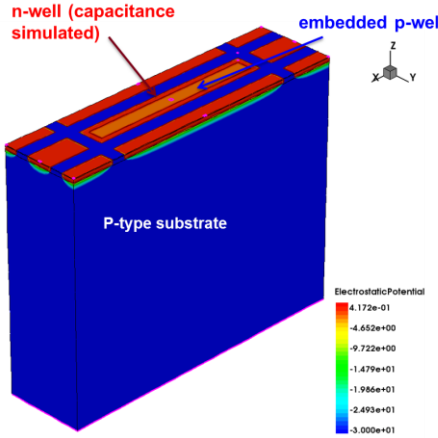
HR-fullCMOS structure

General characteristics

- Bunch timing and amplitude (ToT) extraction
- Column digital readout
- End-of Column hit buffers controlled by the L0 trigger (1MHz, 6μm latency)
- System-on-chip approach (limited IO required
- Serial LVDS readout
- SACI configuration protocol
- Calibration per pixel
- Auxiliary Monitoring

Objectives:

- Demonstrate HR-CMOS as a viable solution for complex circuit architectures (FEI3-like)
  - In-time efficient (95%) within 25ns
  - has a sufficient S/N ratio
  - has 50x250 μm^2 pixel
  - can cope with the expected hit rate
  - is low power ~20μA/pixel
  - can sustain 50 Mrads TID and 10^15 neq/cm2 NIEL



Baseline Pixel 250x50, nwell 230x30	n-well to internal p-well capacitance	330fF
Baseline Pixel 250x50, nwell 230x30	total n-well capacitance with internal p-well	400fF
Baseline Pixel 250x50, nwell 230x30	total n-well capacitance without internal p-well	70fF
Narrow diffusion: 250x50, nwell 220x20	total n-well capacitance without internal p-well	51fF

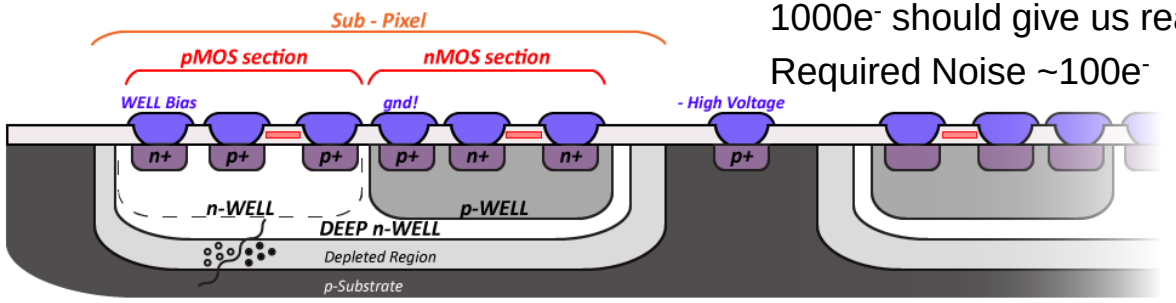
HR CMOS in LFoundry 0.15µm technology

LF15A is a modular 0.15 µm RF CMOS process, offering up to 6 levels of Al plus thick metal (2 - 6 µm), optionally a MIM capacitor, a polyimide passivation and I/O voltages of 1.8 V, 3.3V and 5.0 V.

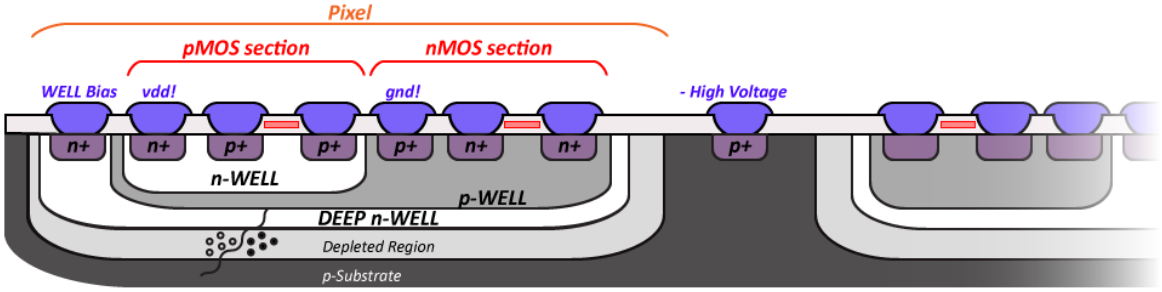
- Substrate resistivity 1-2kΩcm
- Allow isolated NWELL within a DNWELL (Full CMOS)
- Large fill factor ~85% for 50x250 µm^2 pixel
- Break down voltage ~120V

Thinned to 125um:

- full depletion from the back side should be feasible (80V at 2kΩcm)
- Q_{MIP} ~ 10000e$^-$
- Cin ~ 400fF (70fF DNW to SUB, 330fF DNW to PW) for 50x250 µm^2 pixel (worst case)
- Considering sharing a threshold around 1000e$^-$ should give us reasonable efficiency. Required Noise ~100e$^-$

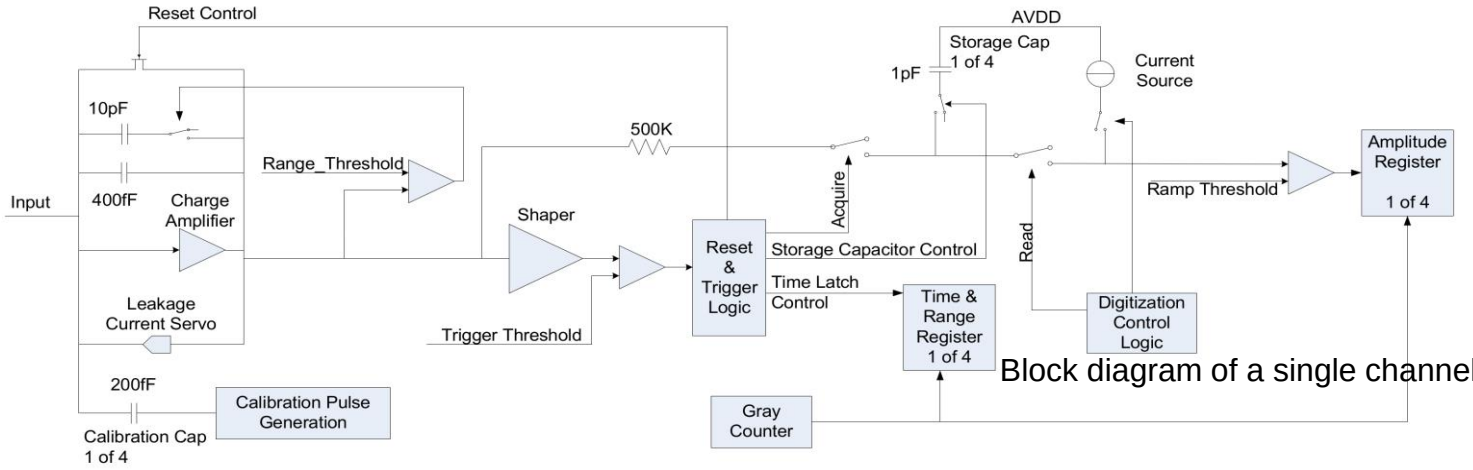


AMS 0.35µm HV

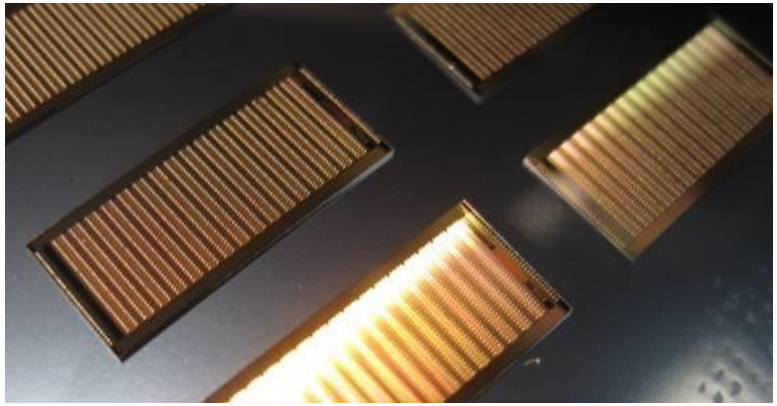


LF 0.15µm HR

KPiX ASIC: ECal read-out of Silicon Detector (SiD) for ILC



Block diagram of a single channel

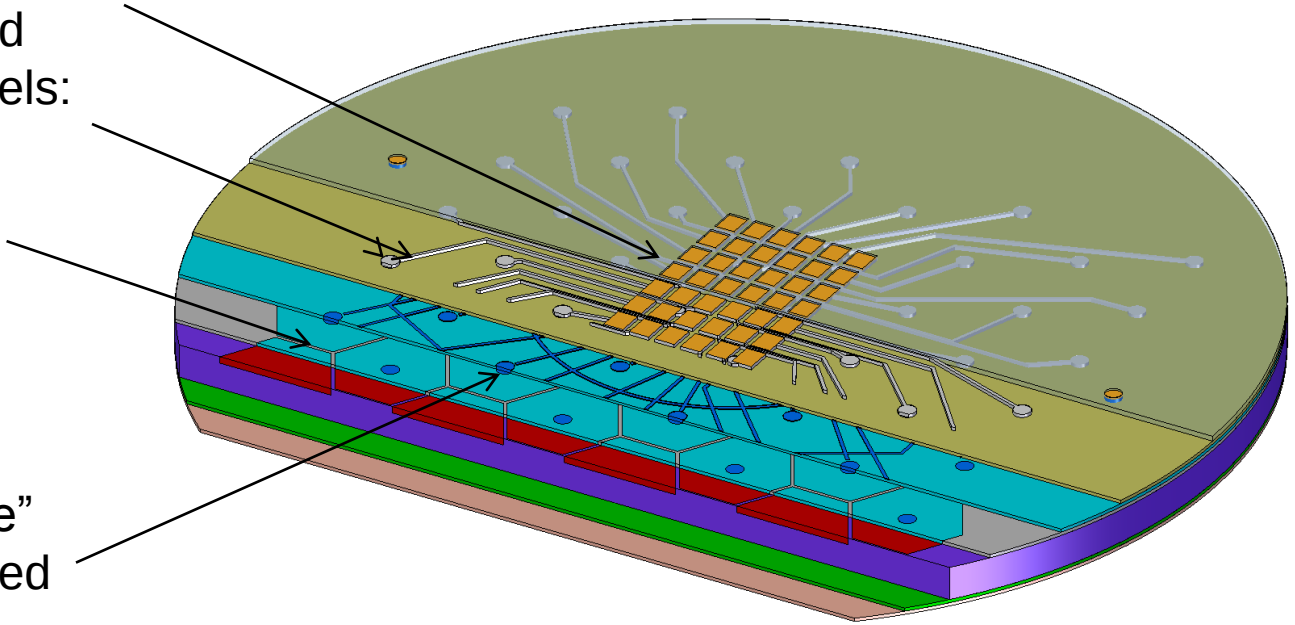


1024-channel KPiX

KPiX, An Array of Self Triggered Charge Sensitive Cells Generating Digital Time and Amplitude Information", D. Freytag. G. Haller, et al. SLAC-PUB-13462, 2008. 4pp (IEEE NSS Oct 2008)
KPiX, an 1,024 cell ASIC, Design and Performance, accepted for presentation at NSS 2012

Sensor Traces

In present design, metal 2 traces from pixels to pad array run over other pixels: parasitic capacitances cause crosstalk.



New scheme has “same” metal 2 traces, but a fixed potential metal 1 trace shields the signal traces from the pixels.

The Ecal sensors are large hexagonal silicon sensors with a diameter of about 10cm segmented in little hexagons of ~5mm. KPix is bump bonded in the center and traces running on top of pixels fan out across the entire sensor

Major Lessons Learned

- Bump bonding to sensors with Al pads can be very difficult…
  - Consider sensor foundry build final pad stack.
  - Don’t dice the sensors until bonding issues are fully controlled.
- EMCal can have huge number of pixels hit simultaneously, causing synchronous disturbances as pixels reset…Problem understood, small changes in KPiX design.
- Sensors plus ROC’s can have issues with parasitic couplings…

KPiXM

	KPiXM-Trk	KPiXM-Cal
Pixel size	50x500 µm²	1000x1000 µm²
Array	200x2400	100x94
Full Size	Stitched 5x5 reticles	Stitched 5x5 reticles
Max. Signal	1fC	1pC
Effective ENC	<200e⁻	<1000e⁻
Filtering	LP + CDS	LP + CDS
S/N	>20	>4
In pix mem. depth	1 bucket	16 buckets
ADC resolution	12 bits	12 bits
DC Power cons.	~ 20µW/pix	~ 20µW/pix
Power pulsing	Yes	Yes

General characteristics

- Amplitude and Timing extraction on N bunches per train in each pixel (N=1 for the tracker, N=16 for the calorimeter)
- Synchronous (time-variant operation)
- Ultra-large Area beyond reticle size (stitching)
- System-on-chip approach (limited IO required
- Platform based design
- Sparse readout
- Power Pulsing
- Calibration per pixel
- Temperature monitoring and tracking
- Auxiliary Monitoring

Large Potentials in SiD Trk and Ecal

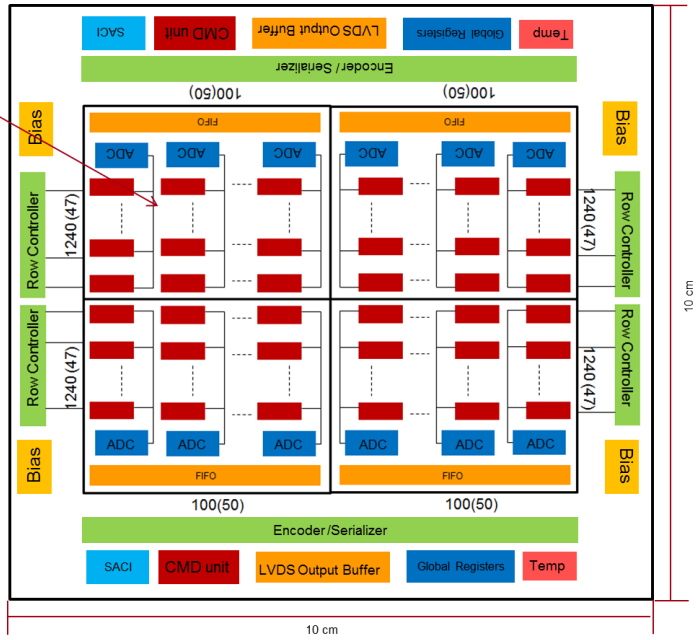
Pixel Matrix: fully analog. Different designs for each detector variants

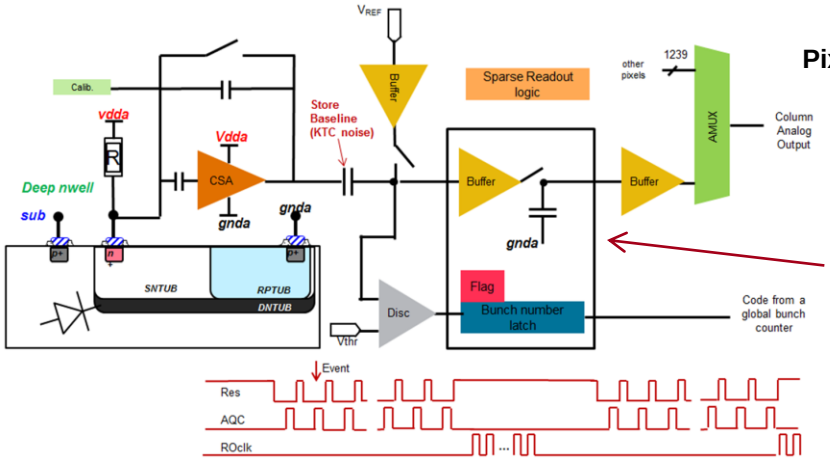
Balcony (kPixM platform):

Analog BE:
- Bias
- Provides Calibration and Monitoring support

Mixed Signal BE:
- Performs Analog to Digital Conversion

Digital BE:
- Controls Configuration
- Controls Acquisition and Readout
- Serialize digital data





Pixel architecture

x16 for Cal version

Conclusions

- CHESS2 is a full size demonstrator for the strip sensor in HVCMOS technology. In case of success it would significantly reduce strip sensor manufacturing cost, material budget, improve resolution, simplified readout chip.
- Fairly complicated chip with difficult layout and new process, design time took much longer than expected. In the top level layout stage and full chip simulations.
- Passive and Active pixel variants for COOL and KPiXM are under design.

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Strip CMOS Author list

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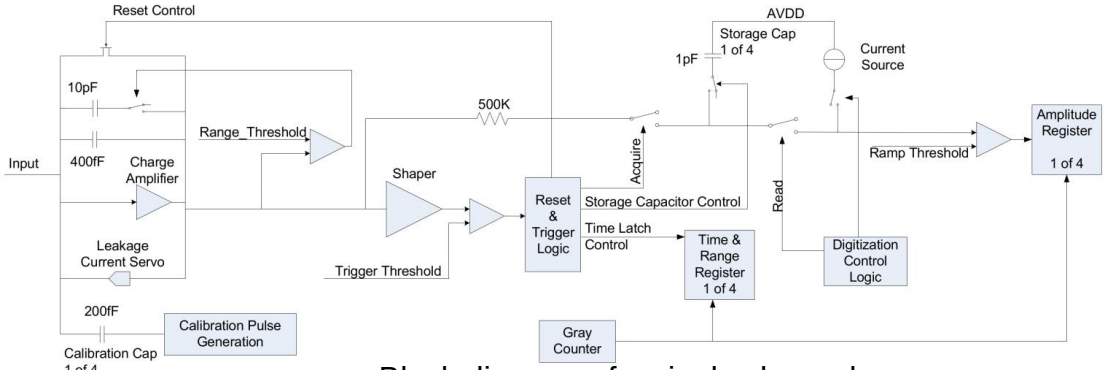
Backup Slides

KPiX ASIC: ECal read-out of Silicon Detector (SiD) for ILC

SLAC

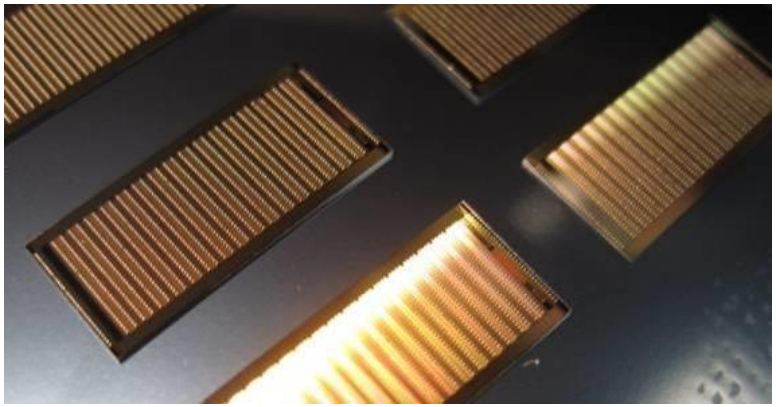
32×32 array = 1024 channels
Designed to be

- bump-bonded to a Si sensor, or
- bumped to a hybrid for large area detectors (RPC's, GEM's, etc)



Block diagram of a single channel

- For each channel of the system-on-chip
  - 4 samples per train with individual timestamps
  - auto-triggering
  - internal per-channel 13-bit ADC
  - automatic range switching for large charge depositions (10pC)
  - bias current servo for DC coupled sensors
  - power cycling: power down during inter-train gaps (20 uW avg for ILC time structure)
  - built-in calibration
  - nearest neighbor trigger ability
  - high-gain feedback capacitor for tracker application
  - dual polarity for GEM and RPC applications
  - external trigger for test beam
- Digital IP core with serial data IO (only 4 signals)
- 0.25µm TSMC



1024-channel KPiX

KPiX, An Array of Self Triggered Charge Sensitive Cells Generating Digital Time and Amplitude Information", D. Freytag. G. Haller, et al. SLAC-PUB-13462, 2008. 4pp (IEEE NSS Oct 2008)
KPiX, an 1,024 cell ASIC, Design and Performance, accepted for presentation at NSS 2012