TCT measurements of HV-CMOS test structures irradiated with neutrons

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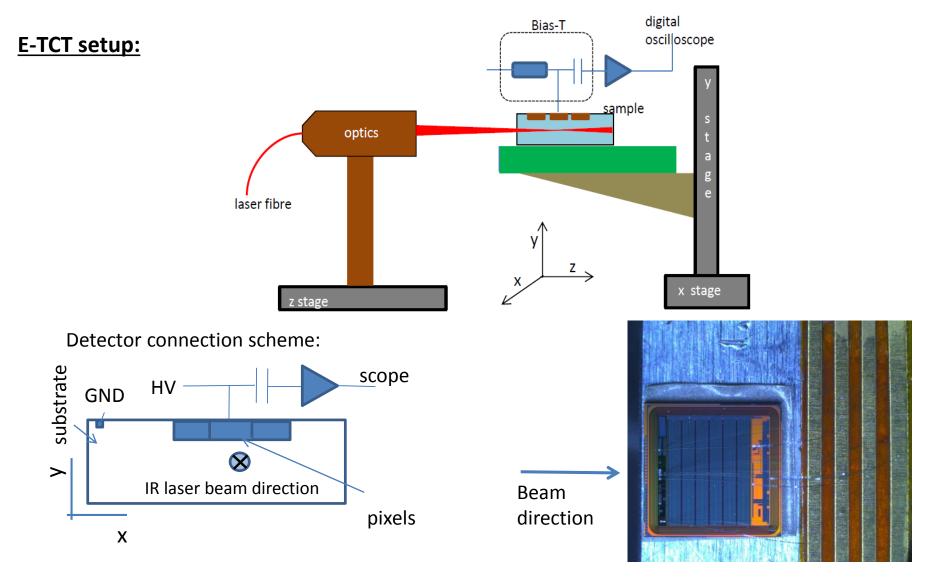
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E-TCT measurements with HVCMOS structures from 3 different foundries made on different substrate resistivities:

- **1. AMS**: 10 Ω cm and 20 Ω cm
- **2. X-FAB** :100 Ωcm
- **3.** LFoundry: 2000 Ω cm

All devices are made on **p-type** substrates

These structures are investigated as candidates for tracking detectors at HL-LHC



Passive devices (no amplifier in the pixel):

- ightarrow observe induced current pulses on collecting electrode on the scope
- \rightarrow collected charge: integral of the pulse in 25 ns

<u>AMS: 10 Ωcm, 20 Ωcm</u>

CCPDv2 (HV2FEI4) chip, AMS 0.18 µm process:

- → active device: output of the amp in the n-well observed on the scope
- substrate resistivity 10 Ω cm
- max bias 60 V

CHESS1 chip, AMS 0.35 μm process:

- \rightarrow passive device
- substrate resistivity 20 Ωcm
- max bias 120 V

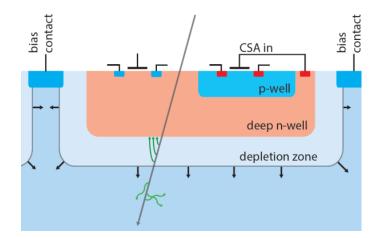
Back plane not processed

ightarrow bias connected from the top of the chip

More detail:

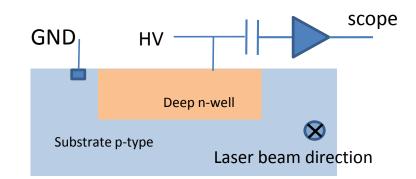
I. Perić et al., NIMA582 (2007) 876-885

- I. Perić et al., NIMA765 (2014) 172-176
- I. Peric et al., 2015 JINST 10 C05021.



From: S. Fenandez-Perez, TWEPP 2015

Passive pixel: no electronic in the n-well



LFoundry: 2000 Ωcm

- 150nm CMOS
- 2 k Ω cm p-type bulk
- HV process, max bias > 100 V
- Thinning and back side metallization possible

More detail:

 Piotr RYMASZEWSKI et al., Prototype active silicon sensor in LFoundry 150nm HV/HR-CMOS technology for ATLAS Inner Detector Upgrade (TWEPP 2015), 2016 JINST 11 C02045 <u>https://indico.cern.ch/event/357738/session/9/contribution/200</u>

CCPDLF VB chip scope two versions: HV GND PW PW PW (no BP) without back side (BP) metallization **PSUB** NISO NISO \rightarrow substrate bias from top DNW • with BP \rightarrow substrate bias from the back plane GND (BP) Measurements done with structures A and F on CCPDLF VB chip

PW

ightarrow see slides from F. Hügging from this morning

<u>X-FAB: 100 Ωcm</u>

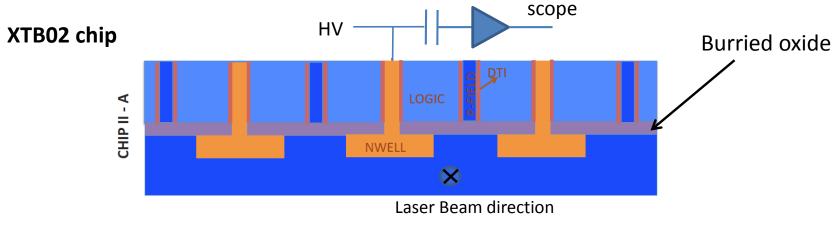
- X-FAB Trench SOI 0.18 um
- p-type bulk, 100 Ωcm
- max bias 300 V
- no back side processing (bias from TOP)

More detail:

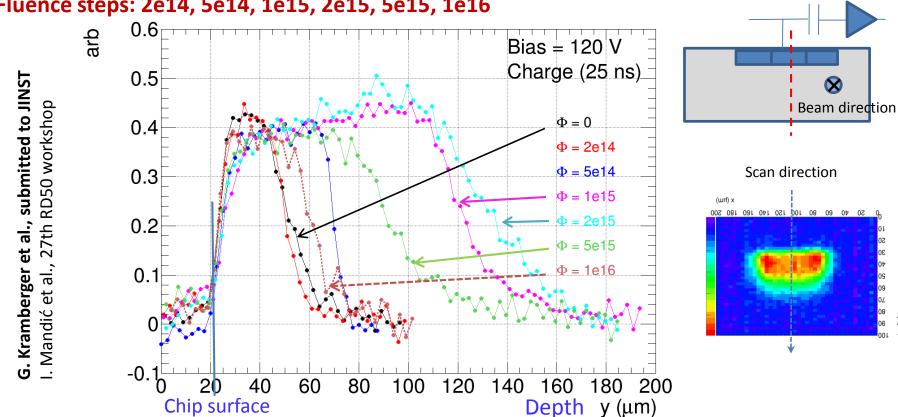
• S. Fernandez et al.,

Charge Collection Properties of a Depleted Monolithic Active Pixel Sensor using a HV-SOI process (TWEPP 2015), **2016 JINST 11 C0106** <u>https://indico.cern.ch/event/357738/session/9/contribution/3</u>

- S. Fernandez-Perez et al., *Radiation hardness of a 180nm SOI monolithic active pixel sensor*, NIMA 796 (2015) 13.
- T. Hemperek et al., A Monolithic Active Pixel Sensor for ionizing radiation using a 180 nm HV-SOI process, NIMA 796(2015)8-12
- slides of M. Backhaus from this morning session



E-TCT, charge collection profile, AMS (20 Ω cm)



Fluence steps: 2e14, 5e14, 1e15, 2e15, 5e15, 1e16

- charge collection width increases with fluence up to \sim 2e15 n/cm²
 - → concentration of initial acceptors falls with irradiation faster than new acceptors are introduced \rightarrow space charge concentration falls
- charge collection width falls with fluences above ~ 2e15 n/cm²
 - → initial acceptor removal finished, space charge concentration increases with irradiation

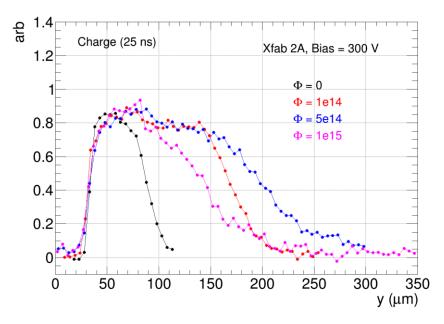
• at 1e16 charge collection region still larger than before irradiation

 \rightarrow similar behaviour also in CCPDv2 chip (10 Ohm-cm)

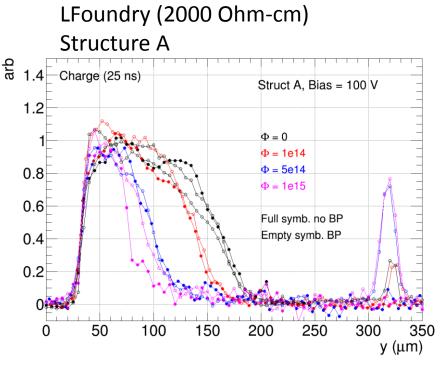
E-TCT, charge collection profiles, Lfoundry, X-FAB

Irradiated up to 1e15 n/cm²

X-FAB (100 Ohm-cm)



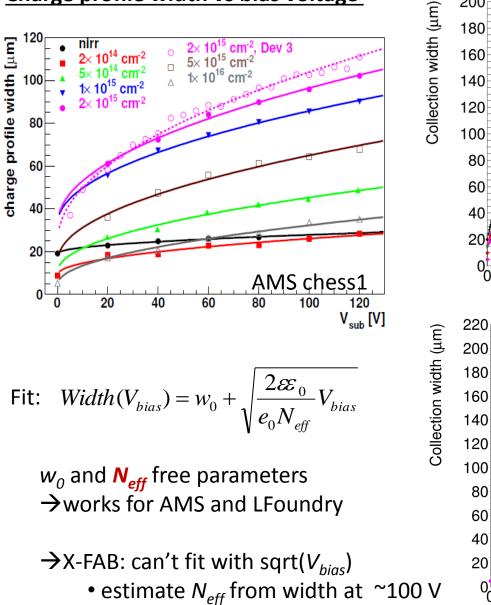
Large increase of charge collection width after 1e14 and 5e14 → effective acceptor removal in X-FAB

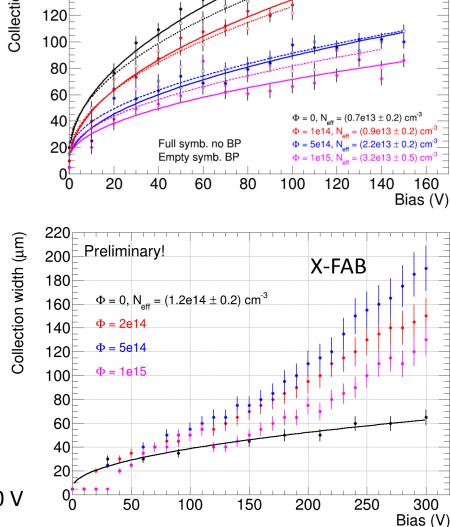


Charge collection width doesn't increase with irradiation

- →these measurements show no effective acceptor removal effect in LFoundry
- → some difference between Back Plane and no Back Plane samples at highest fluence

Charge profile width vs bias voltage





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Preliminary!

LFoundry

<u>*N_{ef}* vs fluence</u>

acceptor removal AMS and X-FAB: Fit: $N_{eff} = N_{eff0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g \cdot \Phi_{eq}$

Radiation introduced deep acceptors: $q \sim 0.02 \text{ cm}^{-1}$

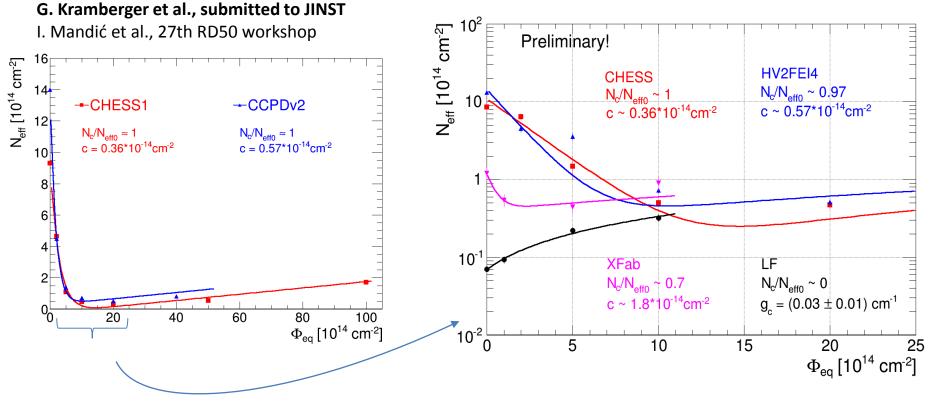
q fixed to 0.02

 $N_{c'}N_{eff0}$ and *c* free parameters,

LFoundry: no removal ($N_c \simeq 0$), fit:

 $N_{eff} = N_{eff\,0} + g \cdot \Phi_{eq}$

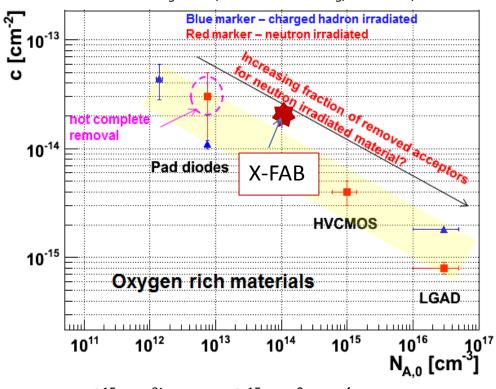
N_{eff0} and g free



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Effective acceptor removal



G. Kramberger et al, 10th Trento Meeting, Feb. 17-19, 2015

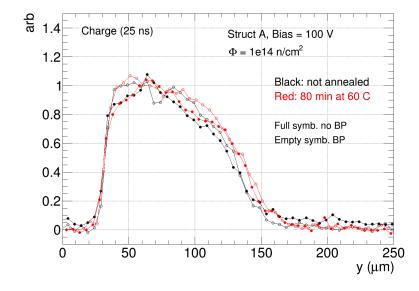
• AMS (20 Ω cm, N_{A0} ~ 10¹⁵ cm⁻³): c ~ 4·10⁻¹⁵ cm⁻², N_c/N_{eff0} ~ 1

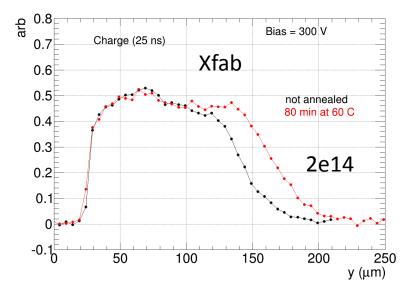
- X-FAB (100 Ω cm, N_{A0} ~ 10¹⁴ cm⁻³): c ~ 2·10⁻¹⁴ cm⁻², N_c/N_{eff0} < 1
- LFoundry (2000 Ω cm, N_{A0} ~ 6·10¹² cm⁻³), no effective acceptor removal observed in this study \rightarrow probably because $N_c/N_{eff0} \ll 1$

Charge collection profile - annealing

Measurement before and after 80 minutes at 60 C

ightarrow 10% to 20 % increase of charge collection width after annealing

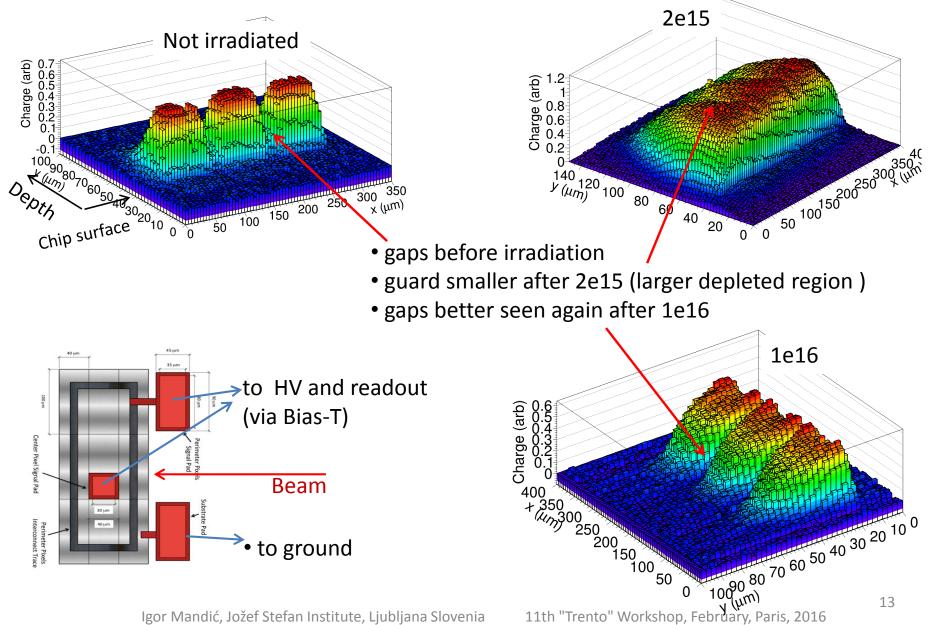




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<u>Measurements with pixel array: AMS (20 Ω cm)</u>

Bias = 120 V, all 9 pixels connected to readout, charge (25 ns)

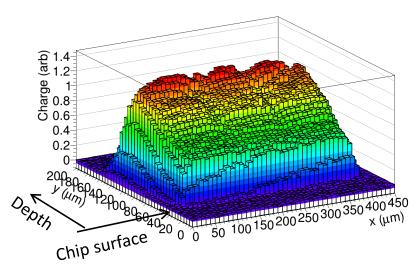


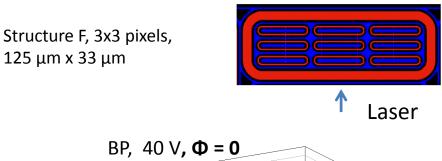
LFoundry, Structure F, all pixels read out

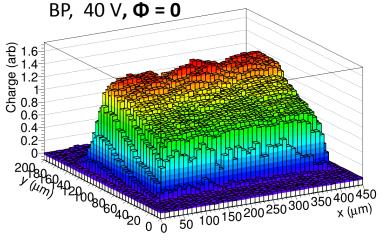
 \rightarrow no efficiency gaps between pixels

No BP, 40 V, **Φ** = **0**

No BP, 50 V, **Φ** = 1e15

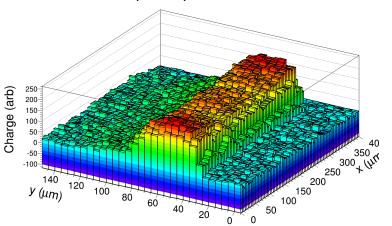


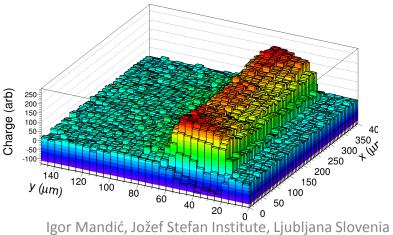




125 μm x 33 μm

BP, 50 V, **Φ** = 1e15

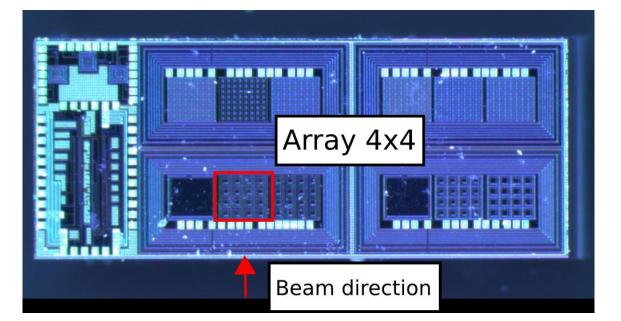


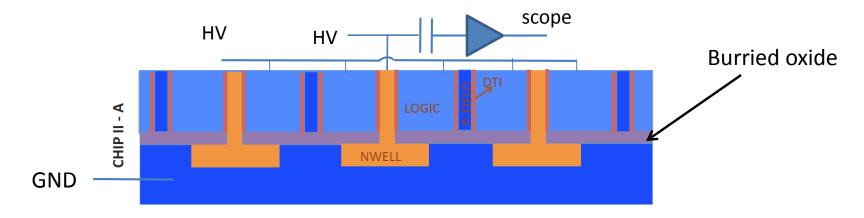


<u>X-FAB: 100 Ωcm</u>

XTB02 chip

pitch 100 μm
n-well: 40 μm x 50 μm

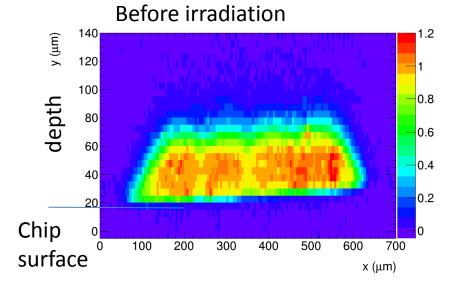


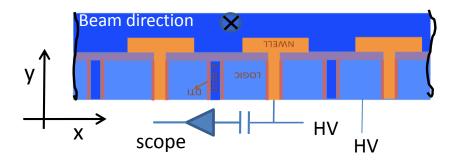


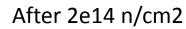
→ "logic" (space for CMOS circuits for active device) and n-well should be at same potential

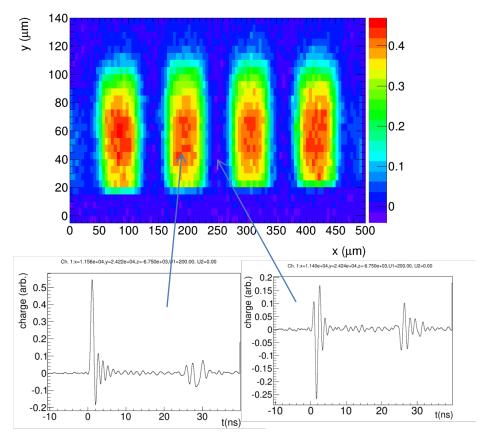
<u>X-FAB: 100 Ωcm</u>

• 4x4 pixel array, all n-wells connected to readout







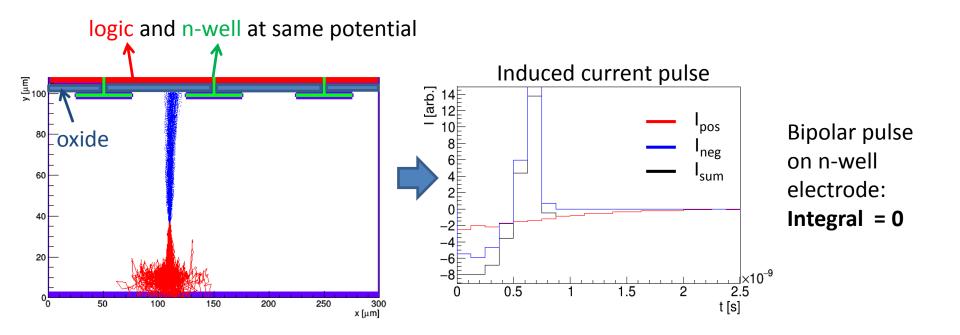


- high collection under n-wells
- Iow charge between → but E-field not zero
 - ➔ large pulses with small integral
 - looks like "logic" acts as collecting electrode (AC coupled)

11th "Trento" Workshop, February, Paris, 2016

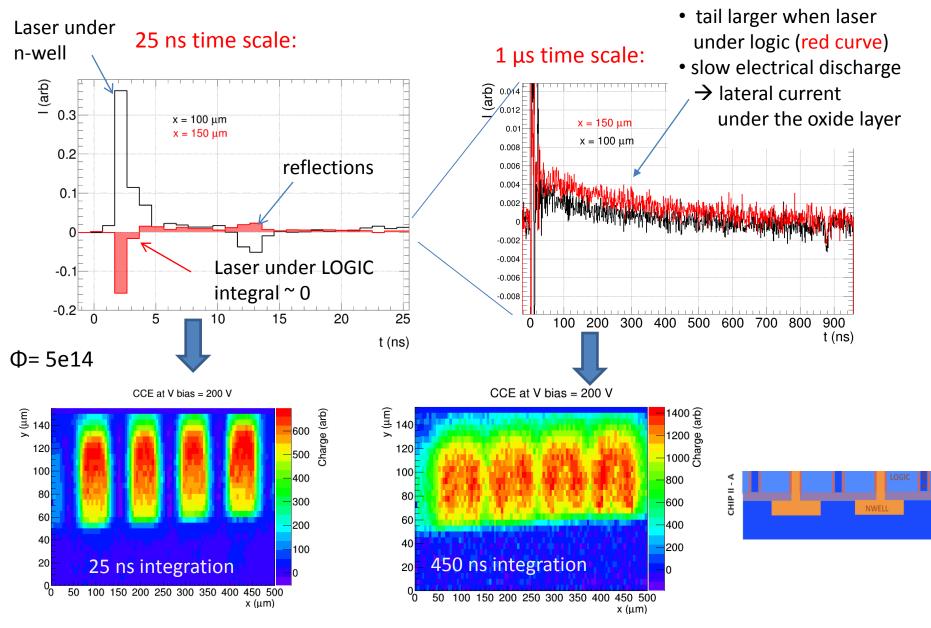
KDetSim simulation

- KDetSim a ROOT based detector simulation package by G. Kramberger (<u>link</u>) (presented at 27th RD 50 Workshop)
- link to the software: <u>http://www-f9.ijs.si/~gregor/KDetSim/</u>



- drift of electrons stops on the oxide surface
- bipolar pulse induced on the readout electrode \rightarrow integral in 25 ns = 0

Efficiency gaps smaller at longer integration times



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11th "Trento" Workshop, February, Paris, 2016

Summary

- Edge-TCT measurements with test structures made on 3 different substrate resistivities:
 - AMS : 10 and 20 Ωcm
 - X-FAB: 100 Ω cm
 - LFoundry: 2000 Ωcm
- large increase of charge collection width after irradiation with neutrons observed in AMS and X-FAB
 - dependence of charge collection width with fluence consistent with effective acceptor removal
 - indication that acceptor removal in X-FAB less complete than in AMS
- X-FAB:
 - increase of charge collection width with bias voltage after irradiation faster than sqrt(V)
 - efficiency gaps between pixels after irradiation (at short (25 ns) integration times)
 - ightarrow parasitic (temporary) charge collection by the "logic" electrode
- LFoundry: charge collection width decreases with increasing fluence
 - ightarrow effective acceptor removal not observed
 - $\rightarrow N_{eff}$ introduction rate on high side
 - no significant charge collection gaps between pixels in the array
 - indication of effect of back plane contact at highest fluence (1e15 n/cm²)