VERTEX 2016

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La Biodola, Isola d'Elba, Italy

Book of Abstracts

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Welcome

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Highlights of the Pixel 2016 workshop

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The Pixel 2016 workshop was held in Sestri Levante (not far from Elba) in early September.

It is the 8th of a series that initiated in the year 2000 in Genoa and moved to US, Europe and Asia. It is the only workshop entirely dedicated to the technology of the pixel detectors and all the applications in particle and x-ray physics. In this report I'll illustrate the most significant advances which have been presented and discussed at the workshop.

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ALICE ITS Operational Experience

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ALICE, A Large Ion Collider Experiment, is conceived to study the physics of strongly interacting matter and the properties of the Quark-Gluon-Plasma produced in ultra-relativistic heavy-ions collisions at the CERN LHC. The innermost detector of ALICE is the Inner Tracking System (ITS) which plays the essential role of primary and secondary vertex reconstruction, it is used for particle tracking and identification and contributes to the first trigger level. The ITS covers the pseudo-rapidity range $|\eta|<0.9$ and consists of six cylindrical layers of silicon detectors placed coaxially around the beam pipe. Three different technologies have been selected to equip the ITS: pixel detectors for the two inner layers, drift detectors for the two central layers and strip detectors for the outer layers. In this report the three detectors constituting the ITS are briefly described, the operational experience during Run2 is summarised with a focus on the performance of the detector compared to Run1 and on the interventions done during the long technical stop at the end of 2015.

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LHCb silicon detectors: Run 2 operational experience

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LHCb is a dedicated experiment to study New Physics in the decays of heavy hadrons at the Large Hadron Collider (LHC) at CERN. The detector includes a high precision tracking system consisting of a silicon-strip vertex detector (VELO) surrounding the pp interaction region, a large area silicon-strip detector located upstream of a dipole magnet (TT), three stations of silicon-strip detectors (IT), and straw drift tubes placed downstream (OT). The operational experience of the silicon detectors VELO, TT and IT from LHC Run 2, the maintenance work during year end shut down, and the upgrade of operation and monitoring software will be presented. Possible operational challenges for the silicon detectors in LHC Run 2 will also be discussed, with particular emphasis on studies of the effects of radiation damage.

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ATLAS IBL operational experience

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The Insertable B-Layer (IBL) is the inner most pixel layer in the ATLAS experiment, which was installed at 3.3 cm radius from the beam axis in 2014 to improve the tracking performance. To cope with the high radiation and hit occupancy due to proximity to the interaction point, a new read-out chip and two different silicon sensor technologies (planar and 3D) have been developed for the IBL.

After the long shut-down period over 2013 and 2014, the ATLAS experiment started data-taking in May 2015 for Run-2 of the Large Hadron Collider (LHC). The IBL has been operated successfully since the beginning of Run-2 and shows excellent performance with the low dead module fraction, high data-taking efficiency and improved tracking capability. The experience and challenges in the operation of the IBL will be presented as well as its performance.

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ATLAS Tracker and Pixel Operational Experience

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The tracking performance of the ATLAS detector relies critically on the silicon and gaseous tracking subsystems that form the ATLAS Inner Detector. Those subsystems have undergone significant hardware and software upgrades to meet the challenges imposed by the higher collision energy, pileup and luminosity that are being delivered by the LHC during Run2. The key status and performance metrics of the Pixel Detector, the Semi Conductor Tracker, and the Transition Radiation Tracker are summarised, and the operational experience and requirements to ensure optimum data quality and data taking efficiency are described.

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CMS Tracker operational experience

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The CMS Tracker was repaired, recalibrated and commissioned successfully for the second run of Large Hadron Collider. In 2015 the Tracker performed well with improved hit efficiency and spatial resolution compared to Run I. Operations successfully transitioned to lower temperatures after commissioning environmental control and monitoring. This year the detector is expected to withstand luminosities that are beyond its design limits and will need a combined effort of both online and offline team to yield the high quality data that is required to reach our physics goals. We present the experience gained during the second run of the LHC and show the latest performance results of the CMS Tracker.

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STAR MAPS Vertex Detector operational experience

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The Heavy Flavor Tracker at the STAR experiment is a set of silicon tracking detectors at the STAR experiment at the Relativistic Heavy Ion Collider at Brookhaven National Laboratory that is designed to extend the STAR measurement capabilities in the heavy flavor domain. This system took data in Au+Au collisions, p+p and p+Au collisions at $\sqrt{s_{NN}}$ =200 GeV at RHIC, during the period 2014-2016. The innermost high resolution PiXeL detector (PXL) is the first application of the state-of-the-art thin Monolithic Active Pixel Sensors (MAPS) technology in a collider environment.
The PXL detector is based on 50 μm-thin MAPS sensors with a pitch of 20.7 μm. Each sensor includes an array of nearly 1 million pixels, read out in a column parallel rolling shutter mode with an integration time 185.6 μs. The 170 mW/cm2 power dissipation allows for air cooling and contributes to reduce the global material budget to 0.4% radiation length on the innermost layer.
The experience and lessons learned from construction and operations of this novel detector will be presented in this talk. Detector performance and results from 2014 Au+Au data analysis, demonstrating the STAR capabilities of charm reconstruction, will be shown.

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The CLAS12 Silicon Strip Detector at CEBAF

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The Silicon Vertex Tracker is a central tracker built for the CLAS12 experiment aiming at measuring the momentum and reconstructing the vertices of charged particles emerging from the target. The system is designed to operate at a luminosity of 1035 cm-2s-1 and to have a momentum resolution of 5% for 1 GeV tracks. The tracker is centered inside 5T solenoid magnet and has 33792 channels of Hamamatsu silicon microstrip sensors. To lower the amount of material in the tracking volume to 0.06X0 modules are assembled on the barrel using unique cantilevered geometry. The sensors have

graded angle design to minimize dead areas and a readout pitch of 156 μm. Double sided module hosts three daisy-chained sensors on each side with total strip length of 33 cm. There are 512 channels per module read out by four Fermilab Silicon Strip Readout (FSSR2) chips featuring data driven architecture, mounted on a rigid-flex hybrid. We describe the detector and present performance results from tracker commissioning with cosmic muons.

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Operational experience with the NA62 Gigatracker

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The Gigatracker is a hybrid silicon pixel detector developed for the NA62 experiment at CERN, which aims at measuring the branching fraction of the ultra-rare kaon decay $K^+ \to \pi^+ \nu\overline{\nu}$ at the CERN SPS. The detector has to track particles in a 75 GeV/c hadron beam with a flux reaching 1.3 MHz/mm^2 and provide single-hit timing with better than 200 ps r.m.s. resolution for a total material budget of less than 0.5% X_0 per station. The tracker comprises three 61mm×27mm stations installed in vacuum (~10^{-6}mbar) and cooled with liquid C_6F_{14} circulating through micro-channels etched inside few hundred of microns thick silicon plates. Each station is composed of a 200μm thick planar silicon sensor bump-bonded to 2×5 custom 100μm thick ASIC, called TDCPix. Each chip contains 40×45 asynchronous pixels, each 300μm×300μm and is instrumented with 720 time-to-digital converter channels with 100 ps bin. In order to cope with the high rate, the TDCPix is equipped with four 3.2 Gb/s serializers sending out the data. Detector description, operational experience and results from the NA62 experimental runs will be presented.

B04-Detectors in design and construction / 18

The DAMPE silicon tungsten tracker

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The DAMPE (DArk Matter Particle Explore) satellite has been successfully launched on the 17^{th} December 2015. It is a powerful space detector made of the following sub systems: a double layer plastic scintillator strip detector (PSD), a silicon-tungsten tracker converter (STK), a bismuth germanium oxide imaging calorimeter (BGO) and a neutron detector (NUD). The DAMPE satellite has been designed for the identification of possible Dark Matter signatures thanks to its capability to detect electrons and photons with an unprecedented energy resolution in an energy range going from few GeV up to 10 TeV. Moreover, thanks to the measurement of the nuclei flux up to 100 TeV, the DAMPE satellite will contribute to a better understanding of the propagation mechanisms of high energy cosmic rays. Currently, the DAMPE satellite is showing excellent performances in orbit and soon the first results will be published.

In this document, a detailed description of the silicon-tungsten tracker-converter STK and its performance in orbit are reported. The tracker has been designed and developed by an international collaboration composed of groups from University of Geneva, INFN Perugia, INFN Bari, INFN Lecce and the Institute of High Energy Physics, Beijing. The STK is made of 768 single-sided AC-coupled silicon micro-strip detectors arranged in 192 ladders for a total silicon area of about 7 m^2, comparable to the silicon area of the AMS-02 tracker. Moreover, the STK is also used as converter thanks to the insertion of tungsten foils which allow the conversions of incoming photons in electron-positron

pairs. The STK is showing a very stable behavior in orbit with excellent performances in terms of charge reconstruction and space resolution.

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Development and construction of the Belle II DEPFET pixel detector

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The construction of the new accelerator at the Japanese Flavour Factory (KEKB) has been finalized and the commissioning of its detector (Belle II) is planned by early 2017. This new e+e- machine ("SuperKEKB") will deliver an instantaneous luminosity of 8·10^35 cm−2s−1, which is 40 times higher than the world record set by KEKB.
In order to be able to fully exploit the increased number of events and provide high precision measurements of the decay vertex of the B meson systems in such a harsh environment, the Belle II detector will include a new silicon vertex detector, based on the DEPFET technology. The new pixel detector, close to the interaction point, consists of two layers of active pixel sensors. The DEPFET technology combines the detection together with the in-pixel amplification by the integration, on every pixel, of a field effect transistor into a fully depleted silicon bulk. In Belle II, DEPFET sensors thinned down to 75 µm with low power consumption and low intrinsic noise will be used.
In the talk, a general overview of latest results and the construction status will be presented.

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The Belle II SVD detector

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The Silicon Vertex Detector (SVD) is one of the main detectors in the Belle II experiment (KEK, Japan). The SVD takes essential roles of precise decay-vertex determination and low-energy-track reconstruction in combination with the PiXel Detector (PXD). SVD consists of four-layers Double-sided Silicon Strip Detectors (DSSD) located in a cylindrical shape around the Belle II interaction point. Each layer is composed of several DSSD ladders. Considering high beam-background circumstance in Belle II, we employ the APV25 readout ASIC chip with performances of small shaping time (~50nsec) and high irradiation tolerance (over 1MGy). The most notable feature of the SVD DSSD is a "chip-on-sensor" concept, which minimizes lengths of the signal propagation from DSSD strips to APV25 and reduces noises from strip capacitance into an acceptable level.
Under the international cooperation among several institutes, the SVD is being developed toward the installation in 2018. Currently, the mass production of the SVD ladders has been started. Also we have performed an electron-beam test combined with the PXD in order to develop tracking algorithm and estimate the performance. This talk will give an overview of the SVD development status, the performance, and the prospect of the SVD assembly and commissioning until the installation.

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The LCHb VELO for Phase 1 Upgrade

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The LHCb experiment will undergo a complete upgrade during the second long shutdown of the LHC. The detector closest to the interaction region, the Vertex Locator (VELO), will be removed and replaced with a new design. The new VELO will sit closer to the interaction point and be capable of a full 40 MHz hardware readout which will drastically increase the physics reach of LHCb, leading us from the discovery towards the precision era. This presentation will discuss the aim, design, testing and current status of the VELO Upgrade.

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The LHCb UT for Phase 1 upgrade

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The planned upgrade of the LHCb detector is designed to achieve 40 MHz readout (the maximum bunch crossing rate), allowing the experiment to collect 5fb^-1 of data per year. As part of this upgrade the tracking subsystem in front of the dipole magnet will be replaced by the Upstream Tracker (UT). Data from the UT will be critical to the LHCb software trigger, allowing more rapid and reliable extrapolation of tracks from the Vertex Locator to the Downstream Tracker. In addition to rapid readout, the UT will feature improved granularity to accommodate increased occupancy.
The detector consists of 4 planes with a total area of approximately 8.5 m^2, composed of single sided silicon strip sensors. The sensors are integrated with the dedicated front-end electronics into modules assembled in a double-sided fashion on vertical structures called staves, providing mechanical support and cooling. The innermost sensors have a circular cut-out at one edge to increase the acceptance near the beam pipe, and most of the sensors feature embedded pitch-adapters to match the sensor output pitch and the front-end electronics input pitch. The dedicated front-end ASIC (SALT) provides digitization with a built-in 6-bit ADC, common mode subtraction, and zero suppression and data processing and formatting. All components of the detector are designed to maintain performance through an integrated luminosity of 50 fb^-1.
The detector will commence operation together with the rest of the upgraded LHCb experiment after the LHC LS2 shutdown, currently scheduled to end in 2020. An overview of the UT design will be given and details of the performance of prototype sensors, electronics, and mechanical components, as well as the envisaged electronics system design and readout architecture, will be presented.

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The upgrade of the ALICE ITS

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ALICE (A Large Ion Collider Experiment) is studying the physics of strongly interacting matter and in particular the properties of the Quark-Gluon Plasma (QGP), using proton–proton, proton–nucleus

and nucleus–nucleus collisions at the CERN LHC (Large Hadron Collider). To fulfil the requirements of the ALICE physics program for run 3 of the LHC, a major upgrade of the experimental apparatus is planned for installation in the second long LHC shutdown. A key element of the ALICE upgrade is the construction of a new, ultra-light, high-resolution Inner Tracking System (ITS). The new ITS will significantly enhance the determination of the distance of closest approach to the primary vertex, the tracking efficiency at low transverse momenta, and the read-out rate capabilities, with respect to what achieved with the current detector. It will consist of seven detector layers based on a Si Monolithic Active Pixel Sensors with a pixel size of about 30x30 μm^2. This contribution presents the design goals and layout of the new ALICE ITS, focusing on the performance of the sensor prototypes and on the technical implementation of the main detector components.

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The upgrade of the CMS pixel detector for phase 1

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The innermost layers of the CMS tracker are built out of pixel detectors arranged in three barrel layers (BPIX) and two forward disks in each endcap (FPIX). The original CMS detector was designed for the nominal instantaneous LHC luminosity of 1 x 10^34 cm^-2 s^-1. Under the conditions expected in the coming years, which will see an increase of a factor two of the instantaneous luminosity, the CMS pixel detector will see a dynamic inefficiency caused by data losses due to buffer overflows. For this reason the CMS Collaboration has been building a replacement pixel detector which is scheduled for installation in an extended end of year shutdown during Winter 2016/2017.

The Phase I upgrade of the CMS pixel detector will operate at full efficiency at an instantaneous luminosity of 2 x 10^34 cm^-2 s^-1 with increased detector acceptance and additional redundancy for the tracking, while at the same time reducing the material budget. These goals are achieved using a new readout chip and modified powering and readout schemes, one additional tracking layer both in the barrel and in the disks, and new detector supports including a CO2 based evaporative cooling system, that contribute to the reduction of the material in the tracking volume.

This contribution will review the design and technological choices of the Phase I detector, and discuss the status of the construction of the detector and the performance of its components as measured in test beam and system tests. The challenges and difficulties encountered during the construction will also be discussed, as well as the lessons learned for future upgrades.

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The CMS Silicon Pixel detector for HL-LHC

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The LHC is planning an upgrade program which will bring the luminosity to about $5 \cdot 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in 2028, with the goal of an integrated luminosity of 3000 fb^{-1} by the end of 2037. This High Luminosity scenario, HL-LHC, will present new challenges of higher data rates and increased radiation. In order to maintain its physics reach in the HL-LHC era, the CMS Collaboration is preparing an upgrade program of the detector known as the Phase-2 upgrade. The CMS Phase-2 Pixel upgrade will require a high bandwidth readout system and highly radiation tolerant sensors and on-detector

ASICs. Several technologies for the upgrade sensors are being studied. Serial powering schemes are under consideration to accommodate significant constraints on the system. These prospective designs, as well as new layout geometries that include very forward pixel discs with acceptance extended from |eta|<2.4 to |eta|<4, will be presented together with performance estimates.

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The CMS Outer Tracker detector for HL-LHC

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The LHC is planning an upgrade program that foresees to increase the luminosity to about 5*10^34cm-2s-1 by 2028, and which will allow to reach an integrated luminosity of 3000fb-1 by 2037. In line with the preparations for the High Luminosity LHC (HL-LHC), the LHC experiments are preparing substantial upgrades of their detectors in order to cope with the new requirements. For the HL-LHC era CMS will replace its current outer tracker by a completely new system that will withstand the harsh operation condition and fully exploit the provided luminosity. In contrast to the existing tracker, the new system will also provide trigger information that will allow track reconstruction in the Level-1 trigger decision. The presentation will discuss the design of the future CMS outer tracker and show highlights from the ongoing R&D activities.

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The Mu3e Pixel-Tracker

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The Mu3e experiment at PSI will search for the Lepton Flavor Violating Decay mu^+ -> e^+e^+e^- with an unprecedented sensitivity of 1 out of 10^16 decays. The Mu3e tracking detector has four layers of High Voltage-Monolithic Active Pixel Sensors (HV-MAPS) and exploits He-gas cooling and an ultra-light mass design with a thickness of 1 per mill of a radiation length per layer to fulfill the very stringent requirements from multiple Coulomb scattering. All registered hits are readout and reconstructed using an online event reconstruction.

The design of the MUPIX chip implementing a trigger-less readout architecture is presented together with recent results from test beam measurements obtained with the MUPIX7 chip, which represents a fully functional small scale HV-MAPS prototype of the final sensor. The layout of the ultra-light tracker modules is described and data transmission tests using thin aluminium-kapton flex-prints are presented.

Finally an outlook is given. Possible applications of the HV-MAPS technology, in particular of the MUPIX design, for upgraded LHC experiments and track trigger applications will be discussed.

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The ATLAS tracker pixel detector for HL-LHC

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The high luminosity upgrade of the LHC (HL-LHC) in 2026 will provide new challenges to the ATLAS tracker. The current inner detector will be replaced with an entirely-silicon tracker which will consist of a five barrel layer Pixel detector surrounded by a four barrel layer Strip detector. The expected high radiation levels are requiring the development of upgraded silicon sensors as well as new a front-end chip. The dense tracking environment will require finer granularity detectors. The data rates will require new technologies for high bandwidth data transmission and handling. The current status of the HL-LHC ATLAS Pixel detector developments as well as the various layout options will be reviewed.

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The ATLAS tracker strip detector for HL-LHC

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As part of the ATLAS upgrades for the High Luminsotiy LHC (HL-LHC) the current ATLAS Inner Detector (ID) will be replaced by a new Inner Tracker (ITk). The ITk will consist of two main components: semi-conductor pixels at the innermost radii, and silicon strips covering larger radii out as far as the ATLAS solenoid magnet including the volume currently occupied by the ATLAS Transition Radiation Tracker (TRT). The primary challenges faced by the ITk are the higher planned read out rate of ATLAS, the high density of charged particles in HL-LHC conditions for which tracks need to be resolved, and the corresponding high radiation doses that the detector and electronics will receive. The ITk strips community is currently working on designing and testing all aspects of the sensors, readout, mechanics, cooling and integration to meet these goals and a Technical Design Report is being prepared. This talk is an overview of the strip detector component of the ITk, highlighting the current status and the road ahead.

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CMOS pixel development for HL-LHC

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CMOS pixel detectors with charge collection in an epitaxial layer (10-20 μm thick) have been developed since 2001 and have become realized in the STAR pixel detector at RICH and are also proposed for the ALICE ITS Upgrade. For the rate and radiation environment expected at the HL-LHC new approaches have been developed based on the following enabling technology features: HV add-ons that allow to use high depletion voltages (HV-MAPS); high resistivity wafers for large depletion depths (HR-MAPS); radiation hard processed with multiple nested wells to allow CMOS electronics

embedded with sufficient shielding into the sensor substrate and backside processing and thinning for material minimization and backside voltage application.

R&D within for HL-LHC has started about 2010. Currently members of more than 20 groups in ATLAS are actively pursuing CMOS pixel R&D in an ATLAS Demonstrator program (sensor design and characterizations) started in 2014. The program's first goal was to demonstrate that depleted (monolithic) CMOS pixels (DMAPS) are suited for high rate, fast timing and high radiation operation at LHC. For this a number of technologies have been explored and characterized. In this presentation the challenges for the usage of CMOS pixel detectors at HL-LHC are discussed such as fast readout and low power consumption designs as well as fine pitch and large pixel matrices. Different designs of CMOS prototypes are presented with particular emphasis on timing (rate) performance and radiation tolerance.

B08-Poster and industry session / 6

Wire-bonding and Assembly Studies for the Outermost Layer of Silicon Vertex Detector in the Belle-II experiment

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The vertex detector (VXD) for the Belle-II experiment, at the Super-KEKB in Japan, measures precisely information of vertexing and tracking. The VXD consists of a pixel detector (PXD) and a silicon vertex detector (SVD) with two and four layers, respectively, so that operates under a high luminosity environment of the Belle-II experiment. For the SVD, a novel chip-on-sensor concept, called "Origami", is developed to reduce the multiple Coulomb scattering and capacitive noise. A wire-bonding and assembly procedures for the outermost layer of the SVD have been studied. A wire-bonding study especially for the Origami module has been performed. As changing the bonding parameters, we measure pull-forces to break the wires by pulling them and observe shape types of broken wires and bond foot prints. In addition, an issue on position precision of a tilted DSSD is found, and a shim method has been employed and studied to improve mechanical precision of the DSSD. In this paper, we present the results of wire-bonding study and introduce the shim method to solve the problem of the tilted sensor during the assembly procedures.

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2.5 Gb/s Simple Optical Wireless Communication System for Particle Detectors in High Energy Physics

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We successfully demonstrated simple and low cost 2.5 Gb/s optical wireless transmission at 10 cm distance, aiming to be employed in high-energy physics experiments using off-the-shelf VCSEL and PIN photodiode with proper ball lens. The measured tolerance to misalignment is around ±1mm at Bit Error Rate of 10-12.
Summary:
Particle physics experiments generate large amounts of data, whose transmission requires huge infrastructure of optical fibers. This increases the material budget, limits space and also introduces excessive labor cost for cables installation and management. High-speed Optical Wireless Communication (OWC) can be a viable solution to reduce the complexity of optical fiber networks for future upgrades. We are designing an OWC system for particle detectors, having as a reference application the inner tracker of Compact Muon Solenoid (CMS) operating in Large Hadron Collider (LHC) at CERN. The proposed OWC solution is not intended to completely substitute the optical fiber links, but it will be rather used to introduce the radial connectivity between silicon strip sensors.
We have designed a 2.5 Gb/s OWC link, which comprises a VCSEL (1550nm) transmitter and a PIN photodiode with ball lens at 10 cm of transmission distance. In future, this simple and low cost design may be integrated on silicon strip sensors inside CMS or other short distance links in particle detectors.
After careful design of the receiver, we achieved a tolerance to misalignment in the range of ±1mm, which is important because, only passive alignment in range of ≥±0.25 mm is acceptable in particle detector systems. In this paper, we report the design of the OWC link and detailed tolerance to misalignment study, based on different diameter lenses at the receiver. By this analysis, we designed the custom packaging for the photodiode and a 4mm ball lens. The results of this activity will also be presented in the paper.
We are aiming to deploy the OWC link in high energy physics environment therefore, we have selected VCSEL and InGaAs PIN photodiode because of their radiation tolerance [J. Troska et al, IEEE Trans on Nuclear Sci, 58, 6, Dec 2011]. Moreover, we selected fused silica and quartz glass type lenses, since they only can provide proper irradiation properties, i.e. much better than BK7 glass at 1550nm [S.M. Javed Akhtar., et al, Optical Materials, Vol 29, 12, Aug 2007].Since these glass types are still tested for lower dose in future we will plan irradiation test in order to qualify the optical components and especially the lens in environments with high radiation level.

B08-Poster and industry session / **70**

Fast pattern recognition of ATLAS L1 track trigger for HL-LHC

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A fast hardware based track trigger for high luminosity upgrade of the Large Hadron Collider (HL-LHC) is being developed in ATLAS. The goal is to achieve trigger levels in high pileup collisions that are similar or even better than those achieved at low pile-up running of LHC by adding tracking information to the ATLAS hardware trigger which is currently based on information from calorimeters and muon trigger chambers only.
Two methods for fast pattern recognition are investigated. The first is based on matching tracker hits to pattern banks of simulated high momentum tracks which are stored in a custom made Associative Memory (AM) ASIC. The second is based on the Hough transform where detector hits are transformed into 2D Hough space with one variable related to track pt and one to track direction.
Hits found by pattern recognition will be sent to a track fitting step which calculates the track parameters . The speed and precision of the track fitting depends on the quality of the hits selected by the pattern recognition step. The figure of merit of the pattern recognition is measured by the efficiency for finding hits from high pT tracks and the power of rejecting hits from low pT tracks and fakes.
We will describe the implementation of the two methods for Silicon Tracker (SIT) for ATLAS HL-LHC upgrad and compare the performance using full event simulation with 200 event pile-up .

B08-Poster and industry session / 49

A silicon posititon sensitive detector for the AEGIS experiment

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The AEGIS experiment at CERN aim to measure the gravitational constant of anti-Hydrogen and in the future perform long-term anti-matter mass spectroscopy. To achieve the gravitational measurement, the AEGIS collaboration will produce a pulsed anti-Hydrogen beam for the first time and measure the deflection of the path of the antihydrogen from a straight line, after it has passed through a Moire reflectometer. A gravitational module, consisting of a silicon detector, an emulsion detector and a scintillating fibre time-of-flight detector will measure the annihilation of the anti-Hydrogen and is being developed to provide a position resolution better than 10 μm. Here we present the status of the AEGIS experiment as well as the latest results on the gravitation module, in particular new results on the silicon detector where the annihilations will take place.

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Qualification of Barrel Pixel Detector Modules for the Phase 1 Upgrade of the CMS Vertex Detector

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To withstand the higher rates of LHC Runs 2 and 3, with expected luminosities of up to 2 x 10^34 cm^{-2} s^{-1}, the current CMS pixel detector at the LHC will be replaced as part of the CMS Phase I Upgrade during the extended winter shutdown in 2016/17. The new pixel detector features a new geometry with one additional detector layer in the barrel region (BPIX) and one additional disk in the forward region (FPIX), new digital readout chips and improved front-end electronics as well as a new CO2-based cooling system for both the barrel and forward region. An overview of the BPIX detector module production will be given, with special focus on the different stages of quality assurance. A review of the quality tests as well as the calibrations which all produced modules undergo in a temperature and humidity controlled environment will be given, together with a description of the testing setups. Exemplary, the KIT/Aachen production line and its subprocesses will be presented together with their quality and yield.

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Tracking Machine Learning Challenge

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The instantaneous luminosity of the LHC is expected to increase at HL-LHC so that the amount of pile-up can reach a level of 200 interaction per bunch crossing, almost a factor of 10 w.r.t the luminosity reached at the end of run 1. In addition, the experiments plan a 10-fold increase of the readout rate. This will be a challenge for the ATLAS and CMS experiments, in particular for the tracking, which will be performed with a new all Silicon tracker in both experiments. In terms of software, the increased combinatorial complexity will have to be dealt with within flat budget at best.

Preliminary studies show that the CPU time to reconstruct the events explodes with the increased pileup level. The increase is dominated by the increase of the CPU time of the tracking, itself dominated by the increase of the CPU time of the pattern recognition stage. In addition to traditional CPU optimisation and better use of parallelism, exploration of completely new approaches to pattern recognition has been started.
To reach out to Computer Science specialists, a Tracking Machine Learning challenge (trackML) has been set up, building on the experience of the successful Higgs Machine Learning challenge in 2014 (see talk by Glen Cowan at CHEP 2015). It associates ATLAS and CMS physicists with Computer Scientists. A few relevant points:

- A dataset consisting of a simulation of a typical full Silicon LHC experiments has been created, listing for each event the measured 3D points, and the list of 3D points associated to a true track. The data set is large to allow the training of data hungry Machine Learning methods : the orders of magnitude are : one million event, 10 billion tracks, 1 terabyte.
- The participants to the challenge should find the tracks in an additional test dataset, meaning building the list of 3D points belonging to each track (deriving the track parameters is not the topic of the challenge)
- A figure of merit has been defined which combines the CPU time, the efficiency and the fake rate (with an emphasis on CPU time)
- The challenge platforms allow measuring the figure of merit and to rate the different algorithms submitted.

The emphasis is to expose innovative approaches, rather than hyper-optimising known approaches. Machine Learning specialists have showed a deep interest to participate to the challenge, with new approaches like Convolutional Neural Network, Deep Neural Net, Monte Carlo Tree Search and others.

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4D fast tracking for experiments at the High Luminosity LHC

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Several efforts have been recently devoted to develop high-resolution timing detectors for tracking at the High Luminosity LHC (HL-LHC) experiments while track triggers, implemented with dedicated hardware, have been used at hadron colliders to select heavy-flavour decays. We propose a R&D project to combine the two methods and develop an innovative detector, based on accurate time and position particle hit measurements, for 4D tracking and fast track trigger. The precise measurement of the hits' time is the key feature to operate an effective pattern recognition that guarantees a high tracking efficiency while enhancing the ghost track rejection, and to perform selective track triggering. We ultimately aim to exploit this detector in flavour physics experiments, in conditions of a high event pile-up, where sensors and front-end electronics are required to provide a hit time resolution of the order of 20 ps and a hit position resolution better than 40 μm, and are able to continuously operate in a harsh radiation environment (up to a total flux of 10^{17} 1-MeV neutrons equivalent per cm^2).
State of the art tracking pixel detectors with precise time-tagging show a time resolution of about 200 ps, and we aim to reduce this by one order of magnitude. Crucial aspects to achieve this ultimate time resolution are the optimization of pixel sensor geometries (in both 3D and planar technologies) to achieve the most uniform electric field, and the design of fast and low noise dedicated front-end ASIC. This front-end will incorporate a fast current amplifier followed by a discriminator and a time-to-digital converter, and will be developed in 65 nm CMOS technology with fault tolerant architecture which matches the radiation hardness requirements.
Feasibility studies of a 4D fast track finding system, using hits' space and time information, has been recently presented as a possible solution for the low level track trigger of the HL-LHC experiments. The system is based on a massively parallel algorithm implemented in commercial FPGAs using a pipelined architecture and allows a precise real-time determination of the track parameters (including time) while maintaining a low fraction of reconstructed fake tracks.
The proposed detector will allow to perform flavour physics at the LHC operating at instantaneous luminosities more than one order of magnitude larger than the current ones, while guaranteeing large tracking efficiencies and a negligible ghost tracks rate.

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Readout architecture for the Pixel-Strip module of the CMS Outer Tracker Phase-2 upgrade

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The Outer Tracker upgrade of CMS introduces new challenges for the front-end readout electronics. In particular, the capability of identifying particles with high transverse momentum requires high speed real time communication among readout ASICs. The Pixel-Strip module needs two different readout ASICs, namely the SSA for the strip sensor and the MPA for the pixelated sensor. At each Bunch Crossing, the strip data are transmitted to the MPA which is responsible for the particle discrimination. The proposed architecture allows for a total data flow between readout ASICs of ~100 Gbps and reduces the output data flow from 1.28 Tbps to 60 Gbps per module with a total power density < 100 mW/cm^2.

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PixFEL: development of an X-ray diffraction imager for future FEL applications

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A readout channel for applications to X-ray diffraction imaging at free electron lasers has been developed in a 65 nm CMOS technology. The analog front-end circuit can achieve an input dynamic range of 100 dB by leveraging a novel signal compression technique based on the non-linear features of MOS capacitors. Trapezoidal shaping is accomplished through a transconductor and a switched capacitor circuit, performing gated integration and correlated double sampling. A small area, low power 10 bit successive approximation register (SAR) ADC, operated in a time-interleaved fashion, is used for numerical conversion of the amplitude measurement. A prototype chip has already been fabricated and characterized. A new readout chip, consisting of 32x32 square cells, has been designed to be bump bonded to a slim/active edge pixel sensor and form the first demonstrator for the PixFEL X-ray imager. The pixel pitch is 110 μm, for a total area of about 16 mm^2. In particular, a couple of different versions for the time variant processor have been implemented and, as compared to the prototype version, the charge preamplifier is provided with a larger range of gain settings, therefore improving the system capability to comply with photon energies in the 1 keV to 10 keV interval. This work, besides discussing in detail the readout channel and array architecture, will present the results from the chip characterization.

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Double-sided strip sensors for Limadou-CSES project

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Production of 60 AC-coupled double-sided silicon microstrip sensors, designed to equip the two layers of the HERD detector in the Limadou-CSES project, has been recently completed at FBK. The sensors, fabricated on 150 mm silicon wafers, have an overall size of 10.96 cm x 7.76 cm = 85.05 cm2. Sensor testing and quality control has been performed at INFN Trieste and TIFPA. After presenting an overview of the test procedures and results, the contribution will focus on the analysis of some characteristic defects, which were severely limiting the production yield. As a result of this study, a modification of the fabrication process has been proposed, leading to an increased yield.

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Characterization of HV-CMOS detectors in BCD8 technology and of a controlled hybridization technique

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Radiation detectors built in high-voltage and high-resistivity CMOS technology are an interesting option for the large area pixel-trackers sought for the upgrade of the Large Hadron Collider experiments. A possible architecture is a hybrid design, where CMOS sensors are readout by front-electronics coupled through a thin dielectric layer. A critical requirement is the radiation hardness of both the sensor and interconnection technology up to a dose of 0.1-1 Grad, depending on the distance from the interaction region.

In this paper we present the characterization of detctors built in BCD8 technology by STMicrolectronics. The BCD8 is a 160 nm process integrating bipolar, CMOS and DMOS devices and it is mostly used for automotive application. A version with 70 V voltage capability has been tested to evaluate its suitability for the realization of CMOS sensors with a depleted region of several tens of micrometer. Sensors featuring 50×250 μm2 pixels on a 125 Ωcm resistivity substrate have been characterized showing a uniform breakdown at 70 V before irradiation, as expected by design in this technology, and a capacitance of about 80 fF at 50 V reverse bias voltage.

The response to ionizing radiation is tested using radioactive sources and an X-ray tune, reading out the detector with an external spectroscopy chain. At the nominal 50 V bias, the device can detect soft X-rays, whose ionization yield is comparable to a minimum ionizing particle in the depletion region, demonstrating the detector is suitable also for charged particle detection and tracking application.

Irradiation tests were performed up to proton fluences exceeding 5×10¹⁵ p/cm2 and they show the depletion and breakdown voltages increases with irradiation

A hybridization process for capacitive coupling has been developed. It consists of gluing the CMOS sensor to the readout electronics using a dielectric epoxy, whose thickness is controlled by SU8 pillars deposited on the readout chip surface. Uniformity of better than 100 nm on the pillar surface has been obtained. Assemblies have been performed using the ATLAS FE-I4 readout ASIC and prototype CMOS sensors. Measurements show a planarity better than 1.5 μm peak-to-peak on the 5 mm length of the HV-CMOS chip. To evaluate more precisely the achievable uniformity dummy chips of FE-I4 sizes have been made on 6-inch wafers. The measurement of the 24 capacitors on each chip is expected to achieve a precise estimation of the real thickness uniformity. The goal is to achieve less then 10% variation on the glue thickness (~0.5 μm).

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Testbeam results for the first real-time tracking system based on artificial retina algorithm

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The INFN-Retina project aims at developing a fast track finding system prototype capable to operate at 40 MHz event rate with hundreds of track per event, for the high-luminosity LHC experiments. A tracking system prototype to be tested on beam has been built as practical demonstrator. In this work, we present the testbeam results of an embedded tracking system prototype based on artificial retina algorithm, capable to reconstruct tracks in real time with a latency <1 μs and with track parameter resolutions that are comparable with the offline results. The maximal event rate that the telescope can accept is 1.1 MHz and it is determined by the Beetle readout chip. The test was carried out using a 180 GeV/c proton beam at the CERN SPS. The tracking system prototype consists of 8 planes of single-sided silicon sensors with 512 strips each and 183 μm pitch; the active area of the sensor is about 100 cm2 with 500 μm thickness.

A custom data acquisition (DAQ) board based on Xilinx Kintex 7 FPGA has been developed. It manages the readout of the ASICs, the sampling of the analog channels, and the retina algorithm implementation. The FPGA resources have been divided among the different modules of the retina architecture: approximately 10% for the switch module that routes the data to appropriate cellular units for the processing stage, 50% for the pool of engines that evaluate how well a set of hits matches with a specific track hypothesis, and 10% for the track parameter determination, keeping the rest for backup. This configuration allows to realise more than 1000 cellular units working in parallel at a clock frequency of the system greater than 200 MHz. Testbeam results will be presented and compared with simulations, in particular for the tracking performance. Perspective for the future will be also discussed.

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The CMS Pixel Luminosity Telescope

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The Pixel Luminosity Telescope is one of the newest additions to a number of sub-detectors dedicated to measuring the luminosity provided to the CMS experiment by the LHC. The PLT, as an independent luminometer, consists of eight 3-layer telescopes based on silicon pixel detectors placed at a high eta around the beam pipe on each end of CMS. All 16 telescopes view the interaction point under a small angle. A fast cluster counting signal from the front-end chips is used to form 3-fold coincidences in the telescopes when a particle passes all three planes. By applying the zero-counting method a bunch-by-bunch online measurement of the delivered luminosity is produced. Tracking information is used in offline analysis methods to derive corrections to the measured data by distinguishing collision products from beam halo and other accidental events caused by albedo, multiple scattered and other stray particles. The tracking information also provides an alignment of the installed telescopes. Using the CMSSW simulation framework and the experience gained during the 2015 running period, the PLT operating configuration was prepared for the high luminosity running period in 2016. The performance of the detector will be presented.

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A Decay Tree Fitter for the Belle II Analysis Framework

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The Belle II experiment at SuperKEKB is rapidly approaching its data taking phase, where it will be used to perform precision measurements of SM and new physics processes with unprecedented accuracy. At the same time, the Belle dataset (~1ab^{-1}) still presents rich possibilities for physics analyses, which can now also be performed within the Belle II Analysis Software Framework (basf2). In both of these cases, high precision reconstruction of particle observables is paramount.

Decay chains in particle physics experiments are typically reconstructed vertex by vertex, starting with final state particles and ending with the head of the decay tree. However, this means each vertex fit is blind to upstream information which could potentially improve the fit resolution.

An alternate approach, which was used with success in BaBar, involves using a least square approach, based on a Kalman filter, to extract all parameters of the decay chain simultaneously. This method is especially useful in the reconstruction of neutral or missing particles and provides access to the full covariance matrix of the decay. It is being implemented in basf2 and will be presented along with the outlook for future physics analyses.

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THE SOFTWARE FRAMEWORK OF THE BELLE II SILICON VERTEX DETECTOR AND ITS DEVELOPMENT FOR THE 2016 TEST-BEAM AT DESY

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(on behalf of the Belle II SVD group)

In this poster, I shall give an overview of the reconstruction software for the Belle II Silicon Vertex Detector (SVD). The Belle II detector at the SuperKEKB e+e- collider in Tsukuba, Japan, aims to probe the flavour frontier, looking for new sources of CP violation. Construction will be completed in late 2018 to be ready for physics data taking. The SVD is a key component of the Belle II inner detector (Vertex Detector), comprised of four layers of double-sided silicon strip sensors. It is responsible for reconstructing trajectories of slow pions, for providing energy loss information for particle identification, and for an accurate determination of decay vertices such as those from K-short mesons. The SVD must therefore provide highly reliable, and precise charged particle hit information at an unprecedented luminosity (designed value 8 x 10^35 cm^-2 s^-1).During April 2016 the SVD and the Pixel detector systems were tested at a DESY test-beam facility in Hamburg, Germany. In this exercise the performance of hardware design, data acquisition and software framework were studied, providing much needed insight for the completion of the detector modules and for their operation in Belle II. I shall discuss SVD software framework, focusing on the aspects that have been developed for the DESY test-beam as well as some aspects of full Belle II operation: such as the treatment of data quality issues in silicon strips, calibration of the charge read-out system, and hit clustering algorithms.

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An Associative Memory Chip for the Trigger System of the ATLAS Experiment

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The AM06 is the 6th version of a large Associative Memory chip designed in 65 nm CMOS technology. The AM06 operates as a highly parallel ASIC processor for pattern recognition in ATLAS experiment at CERN. It is the core of the Fast TracKer electronic system which is tailored for online track finding in trigger system of ATLAS experiment at the LHC. The Fast TracKer system is able to process events up to 100 MHz in real time.

AM06 is a complex chip, designed combining full-custom memory arrays, standard logic cells and IP blocks. It contains memory banks that store data organized in 18 bit words; a group of 8 words is called a “pattern”. AM06 silicon area is 168 mm2 and contains 421 millions transistors and stores 217 patterns.

Moreover AM is suitable also for interdisciplinary applications (i.e., general purpose image filtering and analysis). In future we plan to design a more powerful and flexible chip at 28 nm CMOS.

In this poster the architecture of design and the characterization results of AM06 will be presented.

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Measurement of the hit resolution and reconstruction efficiency of the Belle-II Silicon Vertex Detector in the 2016 beam test at DESY

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The Belle-II experiment is a multipurpose particle detector which will take data at the asymmetric electron positron collider SuperKEKB operated at a design luminosity of $8 \times 10^{35} cm^{-2} s^{-1}$.
Track reconstruction close to the interaction point in the Belle-II experiment is provided by the Silicon Vertex Detector (SVD), consisting of 4 layers of double sided silicon strip detectors, and two layers of pixel detectors (PXD). The SVD was designed to provide a high hit finding efficiency and position resolution when operated in the high-luminosity environment provided by the SuperKEKB collider.

In April 2016 a combined beam test of the SVD and the PXD has been performed at DESY Hamburg to test the full data acquisition chain which will be used in the Belle-II experiment.
For this beam test a section of the SVD and the PXD have been placed in a beam of high energy electrons.
Several runs of data taking have been recorded with varying beam energies, ranging from 2 GeV up to 5 GeV, within a magnetic field which strength was varied between 0 Tesla and 1 Tesla.

We use the data recorded at the beam test at DESY to perform a measurement of the hit reconstruction efficiency and the resolution of the reconstruction of hit positions of the SVD-sensors. For this measurement we use reconstructed tracks to predict the position of a hit on the SVD-sensor under test

and try to find reconstructed hits in the proximity of
the predicted position. Efficiencies are estimated by
counting how often a hit could be associated to
the reconstructed track. The spatial resolution of reconstructed
hits is estimated by analyzing the residuals of the
reconstructed hit positions with respect to the positions predicted by the
extrapolated track.
To avoid biases the SVD-sensor under test is not included
in the track finding and fitting procedure. The efficiency
is measured as a function of the position on the sensor.

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Large Area Thinned Planar Sensors for Future High-Luminosity-LHC Upgrades

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Planar hybrid silicon sensors are a well proven technology for past and current particle tracking detectors in HEP experiments. However, the future high-luminosity upgrades of the inner trackers at the LHC experiments pose big challenges to the detectors. A first challenge is an expected radiation damage level of $2 \cdot 10^{16}$ n_{eq}/cm^2. For planar sensors, one way to counteract the charge loss and thus increase the radiation hardness is to decrease the thickness of their active area. A second challenge is the large detector area which has to be built as cost efficient as possible, i.e. it is aimed for low-cost and large-sized sensors.

The CiS research institute has accomplished a proof-of-principle run with n-in-p ATLAS-Pixel sensors where cavities are etched to the sensors back side to reduce its thickness. One advantage of this technology is that thick frames remain at the sensor edges and guarantee mechanical stability on wafer level while the sensor is left on the resulting thin membrane. During the dicing step, the frames can be removed in order to obtain completely thin sensors. For this cavity-etching technique, no handling wafers are required which represent a benefit in terms of process effort and cost savings.

The membranes with areas of up to ~ $4 \times 4\,cm^2$ and target thicknesses of 100 and 150µm feature a sufficiently good homogeneity across the whole wafer area. The processed pixel sensors show good electrical behaviour with an excellent yield for such a prototype run. First sensors with electroless Ni- and Pt-UBM are already successfully assembled with read-out chips. The technology is currently transferred to 6" wafer size. First results of etching trials with dummy wafers with larger thinned areas will be shown as well.

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A monolithic pixel sensor with fine space-time resolution based on silicon-on-insulator technology for the ILC vertex detector

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We have been developing a silicon-on-insulator (SOI) pixel sensor optimized for vertexing at the International Linear Collider (ILC) experiment. The SOI monolithic pixel detector is realized using standard CMOS circuits fabricated on a fully depleted sensor layer. We are currently designing and evaluating the prototype sensor named SOFIST. The SOFIST can store both position and timing information of the charged particles in each 20×20 μm pixel. The pixel circuit contains a comparator for hit-signal discrimination. If the charge signal is over the threshold voltage level, this analog signal and hit-timing information are captured to analog memory and embedded time-stamp circuits, respectively. The position resolution of the sensor is further improved by the position weighted with the charges shared among multiple pixels. The target performance of the position resolution is better than 3 μm. The sensor also has column-parallel analog-to-digital conversion (ADC) circuits and zero-suppression logic for high-speed data readout. In this presentation, we report the status of the development and evaluation of the prototype sensor.

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Graphene and 2D Materials for Radiation Detection Devices

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Pixels detectors are widely used detection devices in high-energy physics experiments. For more precise and accurate measurements one would like to have faster, less noisy and smaller pixels, but current technology imposes several limits on these characteristics.

The aim of this study is to explore the applications of bi-dimensional materials such as graphene or transition metal dichalcogenide monolayers (TMDs) to address these problems. In particular, one wants to determine whether nanoelectronic devices based on 2D materials could be used to obtain built-in amplification of the pixel signal. In this work some prototype pixel sensors (50x50$\mu\mathrm{m}^2$) based on graphene and MoS_2 transistors are investigated by means of numerical simulations, to evaluate the expected performance. The working principle is the field-effect modulation of the channel conductivity of a 2D material-based transistor, due to the presence of ionization charges in a silicon absorber placed beneath. Several architectures were tested, and a final device of choice is presented, with a sketch of a realistic readout system and its noise figure. The conductance modulation due to incoming particles is found to be more than 30% (on a baseline of $\sim 10\mu$A), resulting in a strong current signal.

According to simulation results, 2D materials-based pixels show promising built-in pre-amplification and good signal quality, with $\mathrm{SNR} \sim 290$ for a MIP crossing the device. Moreover, their fabrication would be in principle simple, if 2D materials fabrication technology continues to improve. More specifically, these devices would be less complex than other proposed systems such as SOI or DEPFET pixels. These aspects allow to conclude that it would be highly desirable to further study the subject, to perfect the device design, as well as to build some prototype devices to be tested with a radiation source.

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The Monitoring System of the Belle-II Vertex Detector

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The Belle-II VerteX Detector (VXD) is a 6 layers silicon tracker device that will cope with an unprecedented luminosity of 8 × 10^35 cm−2s−1 achievable by the new SuperKEKB e+e− collider, now under commissioning at the KEK laboratory (Tsukuba, Japan).
All environment parameters such as temperature, humidity and radiation levels, must be constanly monitored and under certain conditions action must be promptly taken, such us interlocking the power supply or deliver an abort signal to the SuperKEKB collider.

The VXD electronics is cooled with a complex biphase CO2 system at -30° and constantly fluxed with N2 to keep the humidity as low as possible.
The temperature system is based on two different sensors, NTC thermistors and FOS (Fiber Optical Sensors) with partial overlap.
The humidity is monitored by sniffing system and precise dew-point sensors.

A radiation monitoring and beam abort system has been developed based on single-crystal diamond sensors.
The sensors will be placed in 20 key positions in the vicinity of the interaction region.
The severe space limitations require a remote readout of the sensors.
The system design will be described, along with the sensor characterization procedure and the prototype of the readout electronics.

In this contribution we present the first results of the temperature and humidity system commissioned in a Beam Test at DESY in April 2016 and the preliminary results of the radiation monitoring achieved with a prototype system during the first SuperKEKB commissiong phase in February-June 2016.

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A Prototype of a New Generation Readout ASIC in 65nm CMOS for Pixel Detectors at HL-LHC

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The HL-LHC accelerator will constitute a new frontier for particle physics after year 2024. Major experimental challenge resides in inner tracking detectors: here the dimension of sensitive area (pixel) has to be scaled down with respect to LHC detectors.

This paper describes a readout ASIC in 65nm CMOS with a matrix of 64x64 pixels each of dimension 50x50 μm2, designed by CHIPIX65 project, part of RD53 Collaboration. It is a demonstrator of a Pixel Phase 2 chip, with compact design, low power and in-time threshold below 1000e−. All IP-blocks and analog front ends are designed by CHIPIX65 project in the framework of RD53 Collaboration: they have been produced, tested and several have already proven to be radiation hard up to 5-800 Mrad. The chip implements two different analog front end designs, one with asynchronous the other with synchronous comparator designs, but with main common characteristics: compact design; ENC below 100 e- for 50 fF input capacitance; below 5 μW/pixel power consumption; fast rise time, allowing correct time-stamp; signal digitisation using Time Over Threshold; leakage current compensation up to 50nA per pixel.

All global biases and voltages are programmed in the chip periphery, for each value a 10-bits current steering global DAC is used; a band gap circuit provides a stable reference voltage. The adopted strategy is very robust, easily scalable and mismatch effects are kept to a negligible level. Bias voltages and current are monitored by a 12-bit ADC.

A novel digital architecture has been designed in order to maintain a high efficiency (above 99%) at pixel hit rate of 3 GHz/cm2 , trigger of 1 MHz rate and latency of 12.5µsec. The digital architecture is organized into pixel regions: in order to have a very compact and low power architecture, a large pixel region consisting of 4x4 pixels has been used. A 5-bit ToT charge is stored in a centralised latency buffer: at the arrival of a trigger, a matching logic selects eventually the right memory location and sends the data to the End of Column logic. The particle inefficiency due to this architecture is about 0,1% for an area occupation of of 65% and a low power consumption. The readout is obtained using a column drain protocol with a FIFO for each pixel region column, connected to a global dispatcher FIFO that after a 8b10b encoding splits the data into 20-bit trunks and sends them to a serialiser. Data are sent out from the chip using a differential transceiver converting the CMOS into SLVS JEDEC 400mV standard. Given the small size of the chip, an output rate of 320 MHz for the serialised data can be used, but higher output rates are possible., since SER and sLVDS-TX are designed to sustain up to 1.2 Gb/s. Chip configuration is performed through fully-duplex synchronous SPI-master/slave transaction. CHIPIX65 demonstrator will be submitted in June 2016.

B09-Applications to medical and other fields / 21

R&D networks and opportunities

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Future Radiation Detectors and Imaging Technologies have common requirements in different fields of application. The “ERDIT” network was formed in 2014 to explore the European research and development trends and to promote exchanges from different scientific fields and different countries. The talk will present the “ERDIT” network and related collaborative activities and review the current funding opportunities dedicated to Radiation Detectors and Imaging Technologies like ATTRACT.

B09-Applications to medical and other fields / 35

Applications of vertexing detectors

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Detector concepts originally developed for vertex applications have been further developed to address the needs of different applications outside high-energy physics. A typical example is the MEDIPIX series of detectors. The original concept was based on the Omega3 readout chip. Over the years the technology has been further developed into the MEDIPXI2 chip with energy windowing and its successor MEDIPIX3 adding charge summing to avoid spectral distortion due to charge sharing. The TIMEPIX chip introduced time-over-threshold (TOT) and time-of-arrival (TOA) concepts to identify incoming photons or particles. With its successor TIMEPIX3 TOT and TOA can be recorded simultaneously. TIMEPIX3 also uses event driven readout to increase the maximum event rate.

The different MEDIPIX/TIMEPIX chips have found applications as materials research, medical imaging, dosimetry and astronomy. This presentation will cover the characteristics of the devices and their use in different applications.

B09-Applications to medical and other fields / 50

Vertexing and tracking in hadrontherapy

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Hadrontherapy represents a remarkable example of the interdisciplinary collaboration between nuclear physics and medicine. Proton and carbon ion beams are used in the clinical practice for external radiotherapy treatments achieving, for selected indications, promising and superior clinical results with respect to X-ray based radiotherapy. At the same time, the accurate dose delivery is more sensitive to the patient positioning and to anatomical variations with respect to photon therapy. In order to fully exploit the advantages of ion beams in the clinical practice, the development of novel techniques to monitor the beam range and the dose release during the patient treatment is highly demanded. Several non-invasive monitoring strategies based on tracking and vertexing of secondary radiation exiting the patient have been proposed, \textit{e.g.}, prompt gamma, charged secondaries and beta+ emitters, and will be reviewed together with future directions.

B10-Applications to medical and other fields / 65

DepFET Direct Electron Detectors for time-resolved imaging applications

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Carrying out ultrafast electron diffraction (UED) experiments capturing the motion of molecules or the dynamics of biological systems at very short time scale require the availability of ultrafast, ultrabright electron sources and high performance imaging detectors. There has been tremendous progress in the field of semiconductor based X-ray detectors driven by the needs and demands of existing and upcoming fee-electron laser sources or related experiments.
While direct hit detectors are the standard choice for any application involving the detection of photons, there use is only marginally when it comes to the detection of electrons, as required in any ultrafast electron diffraction (UED) experiment or the wide field of electron microscopy applications (e.g. Transmission Electron Microscopy).
Most camera systems employed in such experiments are rather slow in terms of frame rate and use an indirect process by means of a scintillator to retrieve the electron intensity distribution by detecting the optical photons created in the scintillator.
This work reports on the development of novel ultrafast direct-electron-hit silicon detectors using DEPFET technology. These systems allow for a high signal-to-noise ratio and the capability to discriminate single electrons with high statistical probability. For UED experiments we are developing systems providing 1kHz frame rates and therefore single shot capabilities. A second (related) detector system will run at frame rates up to 80 kHz, and is mainly intended for recording the dynamics of non-periodic (biological) samples in real space and real time by use of dynamic electron microscopy.

B10-Applications to medical and other fields / **75**

XFEL Detector Developments

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In the last years a large development effort has taken place in the photon science community around the world to develop detectors for existing and upcoming X-ray free electron laser (XFEL) facilities. XFELs have very short X-ray pulses (~100 fs) with a very high intensity (10^12) and, depending on the facility a high repetition rate of up to 4.5 MHz. The detectors usually aim to achieve single photon sensitivity (i.e. require a very low noise) and a dynamic range of 10^4-10^5 photons. To achieve this conflicting requirements different concepts have been developed by the different groups. In this presentation I will give an overview over the different developments.

B10-Applications to medical and other fields / **73**

Diamond detector technology; status and perspectives

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At present most experiments at the CERN Large Hadron Collider (LHC) are planning upgrades in the next 5-10 years for their innermost tracking layers as well as luminosity monitors to be able to take data as the luminosity increases and CERN moves toward the High Luminosity-LHC (HL-LHC). These upgrades will most likely require more radiation tolerant technologies than exist today. As a result this is one area of intense research. Chemical Vapor Deposition (CVD) diamond has been used extensively and successfully in beam conditions/beam loss monitors as the innermost detectors in the highest radiation areas of essentially all LHC experiments. The startup of the LHC in 2015 brought a new milestone where the first diamond pixel modules were installed in an LHC experiment (ATLAS) and successfully began taking data. As a result, this material is now being discussed as a possible sensor material for tracking very close to the interaction region and for pixelated beam conditions/beam loss monitors of the LHC/HL-LHC upgrades where the most extreme radiation conditions will exist.

The RD42 collaboration at CERN is leading the effort to use CVD diamond as a material for tracking detectors operating in extreme radiation environments. During the last three years the RD42 group has succeeded in producing and measuring a number of devices to address specfic issues related to use at the HL-LHC. We will present status of the RD42 project with emphasis on recent beam test results. In particular we present the latest results on material development, the most recent results on the independence of signal size on incident particle rate in poly-crystalline CVD diamond pad and pixel detectors over a range of particle fluxes up to 20 MHz/cm^2 measured, and results from first 3D diamond detectors which produce an extremely radiation tolerant device and collect nearly all of

the charge deposited in the material. In addition we will present plans for future use of the most recent devices.

B11-New developments and detector R&D / 38

Small pitch 3D devices

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The ATLAS IBL project led to an impressive progress in 3D radiation sensors, with experimental confirmation of their remarkable radiation tolerance with relatively low power dissipation, and the demonstration of medium volume productions with an acceptable yield. These accomplishments paved the way for using 3D sensors in other pixel detector systems in Phase 1 upgrades at the LHC (e.g., AFP and CT-PPS), and made them a very appealing option also for the innermost tracking layers at the HL-LHC. The latter application involves very high hit-rate capabilities, increased pixel granularity, extreme radiation hardness, and reduced material budget. Compared to existing 3D sensors, the future ones will have to be geometrically "downscaled", involving smaller pitch (e.g., 50×50 or 25×100 μm2), shorter inter-electrode spacing (~30 μm), narrower electrodes (~5 μm), and reduced active thickness (~100 μm). The development of a new generation of 3D pixel sensors with these challenging features is under way by different groups in Europe, in collaboration with processing facilities like FBK, CNM, and SINTEF.
This talk will first review the lessons learned from existing 3D detectors. Then it will address the main design and technological issues for small pitch 3D devices. Preliminary results from the electrical and functional characterization of the first prototypes will be reported and compared to TCAD simulations.

B11-New developments and detector R&D / 57

SOI Monolithic pixel detector technology

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Silicon-On-Insulator (SOI) is very fascinating technology which can be used to fabricate monolithic radiation detectors. Although there were several difficult issues to solve such as back-gate effect, sensor-circuit coupling, and radiation hardness etc., we could solve these issues by introducing buried wells, double-SOI wafer and higher dose LDD region.
We also introduced active merge technique in which NMOS and PMOS transistors are merged and share active layer and contacts. This reduced layout size less than 50% of previous design.
I will present newly developed technologies and recent developments of integration-type and counting-type detectors.

B11-New developments and detector R&D / 58

Micro channel cooling solutions for silicon detectors

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With the advent of thinner and more precise silicon detectors for vertexing and tracking in collider experiments, the design of sufficiently thin and stable supports and services is increasingly challenging. In this contribution an overview is given of the adoption of micro-channel cooling in high energy physics. The emphasis is on a recently proposed approach to integrate the cooling channels in the silicon sensor and the connectivity of the micro-channel circuit to the overall system. Measurements are presented of the cooling performance, that can exceed the performance of more traditional systems by a large factor. The measurements are extrapolated to more realistic systems. We also discuss the impact on the mechanical stability.

B12-New developments and detector R&D / 56

Low gain avalanche devices

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The objective of the work presented in this talk is the development of new position sensitive detectors with low signal amplification useful also for timing applications and called Low Gain Avalanche Detector (LGAD). These new devices are based on the standard Avalanche Photo Diodes (APD) normally used for optical and X-ray detection applications.
We will present the last experimental results on 50um thin LGAD fabricated for the High Granularity Time Detector of the ATLAS experiment. We have performed a beam test at CERN with LGAD of different gain and report the measured timing resolution, comparing it with laser injection and simulations. For the 50 μm LGAD, the timing resolution measured is 30 ps.
In order to optimize the electrical characteristics of thin LGAD we performed two dimensional numerical simulations based on Sentaurus and Silvaco simulation tools and the technological steps needed for the fabrication.
In this talk we will discuss also the radiation hardness of LGAD and the methods implemented to withstand the high fluences expected in the HGTD.

B12-New developments and detector R&D / 13

High fluence effects on silicon detectors: damage and defects characterization

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The CERN RD50 collaboration has the aim to investigate radiation hard semiconductor devices for very high luminosity colliders. This is done by looking into four key aspects: Defect/material characterization, detector characterization, new structures and full detector systems.

After the Phase II upgrade of the Large Hadron Collider (LHC) the luminosity will increase and therefore the radiation level for the silicon detectors. They have to be able to operate at fluences of up to 2E16 neq/cm^2. To cope with this, new semiconductor sensor technologies have been developed within the RD50 collaboration. This talk will give a brief overview of those, which include:

3D detectors, HV-CMOS pixel detectors, low gain avalanche detectors (LGAD) and sensors with slim/active edge.

B12-New developments and detector R&D / 77

Experimental techniques for defect characterization of highly irradiated materials and structures

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There are several applications where solid devices are exposed to irradiation. Depending on the operational conditions (type of the particles, temperature, fluence) the physical properties of the exposed device degrades differently, reaching the point of electrical failure in very harsh enviroments. The radiation damage, starting already under low irradiation fluences, get more complex with increasing the fluences due to the generation of various type of irradiation induced, electrically active, defects. Accordingly, the defect characterization becomes a more difficult and costly task, requiring several complementary techniques to understand the detailed relation between the "microscopic" reasons as based on defect analysis and their "macroscopic" consequences for device performance. In this respect, the talk will focus on the defect characterization techniques suitable for investigating highly irradiated materials/structures, employed and developed within CERN RD50 Collaboration: I-DLTS, TSC and TDRC for electrical characterization of bulk and interface defect states, HRTEM and EPR for structural and chemical identification of the radiation induced defects. Correlations with the results obtained by other techniques determining the „macroscopic" electrical properties of the devices (leakage current, effective doping, carriers trapping lifetime) will be presented as well.

B13-Radiation hardness and simulations / 60

Radiation damage models, comparison and perfomance of TCAD simulation

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The simulations of radiation damage effects in silicon detectors from the properties of the lattice defects has long been one of the important tasks of CERN-RD50 collaboration. As calculations often don't converge with full set of the indentified defects the simulations include either reduced number of defects or more often effective defects. Several different models were presented in the past, which gave reasonable agreement with the limited number of measured data, however often failing to describe a broader set of measurements of collected charge, leakage current and full depletion voltage. The models used within RD50 will be presented together with the comparisson of different simulation tools. A special empahasis will be given to practical aspects of simulations. Finaly the device model based on measurements whose parameters should be used as anchor points for simulations of heavly irradiated silicon detectors will be described.

B13-Radiation hardness and simulations / 72

Radiation Tolerance of 65nm CMOS

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The High Luminosity LHC (HL-LHC) is the proposed upgrade to the LHC to be made in a long machine shutdown which should take place in the years 2023 to 2025, according to current schedule and aims increasing the luminosity of the machine up to 5.1034 cm−2s−1. The upgrade will improve statistically marginal measurements and will allow a better chance to see rare processes.
The ATLAS and CMS experiments are planning major detector upgrades to cope with the increase in beam luminosity. Pixel detectors are placed in the innermost part of the experiments and are therefore exposed to the highest fluences and highest ionizing radiation doses. Simulations show that the innermost parts of the new pixel detector will integrate a fluence of about 1016 n/cm2 (1 MeV neutron equivalent) and a Total Ionizing Dose (TID) of 1000 Mrad.
The RD-53 collaboration was established to develop the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC. This development requires extreme rate and radiation tolerance. The 65 nm CMOS process seems to be promising for the future pixel readout chips in terms of high integration density and a first demonstrator chip containing 76 800 pixels of 50µm × 50 µm will be submitted in April 2017 .
The first part of this presentation is dedicated to the TID effects on the 65nm process. A lot of information about the 65 nm process tolerance were obtained by studying radiation effects on individual transistors and used as a way to understand the causes of failure in digital or analog designs. In fact, the radiation tolerance of 65 nm bulk CMOS devices was investigated using 10 keV X-rays up to a Total Ionizing Dose (TID) of 1 Grad and irradiation tests were performed at room temperature (25 ℃) as well as at low temperature (-15 ℃).
In principle, the gate oxides of advanced CMOS technologies are scaled to thinner dimensions, which should make devices highly tolerant to TID effects. However, irradiation tests showed a strong performance degradation for the small size devices. In fact, the Shallow Trench Isolation (STI) used as the field oxide for device isolation and represents the main issue when considering TID effects for scaled down technologies.
We will review the various degradations induced by the STI charge buildup. The first degradation is related to the leakage current in the irradiated NMOS devices and caused by the parasitic STI device. The second type of degradation concerns the threshold voltage shift of narrow channel devices. The effect, intitled “Radiation-Induced Narrow Channel Effect” (RINCE) was already reported for other commercial processes. Furthermore, For this 65 nm process, another effect was observed and designed as Radiation-Induced Short Channel Effect (RISCE). It is realated to the fact that degradation depends not only on the width of the channel but more degradation is observed for short channel than for long channel devices.
The effect of the bias and of the temperature during irradiation and during annealing will be discussed. In particular, high temperature annealing does not help recovering the current drive in irradiated devices. On the contrary, performance degradation is observed after high temperature annealing for PMOS devices. Very often, in irradiation qualification, the Low Dose Rate (LDR) dammage is estimated from the TID effects at a High Dose Rate (HDR) followed by high temperature annealing. For the 65 nm process, testing are carried out in order to estimate the dammage at LDR and to provide a methology for qualification and especially for the pixel detector which will function in a cooled area.
A methology for SPICE parameters extraction for radiation-induced degradation on pmos and nmos transistors is proposed. Comparison of radiation-induced leakage current, threshold shift and mobility degradation in test MOSFETs between total dose irradiation experiments and simulation results exhibits a good agreement.
The second part of this presentation is dedicated to the Single Event Upset (SEU) tolerance for the 65nm process. Indeed, for the future pixel readout chips, local and global memories are implemented to retain respectively the local pixel configuration and the global chip configuration. SEU tolerant memories are used to allow reliable operation at high beam intensities and to avoid reloading frequently the configuration data. A prototype chip has been designed where a different structures of the configuration memories based on Dual Interlocked CElls (DICE) or on Triple Redundancy Latches (TRL) were implemented.
SEU tolerance tests were carried out at CERN-PS facility with the 24 GeV protons beam. SEU measurements show that the DICE latch improves the SEU tolerance by a factor of 10 with only a small increase on the area compared to the standard latch, making the DICE suitable for pixel configuration whereas the TRL allows an improvement by a factor of 2500 but the structure consumes a higher area making it suitable only for global configuration.

B13-Radiation hardness and simulations / **2**

RD53 status and plans

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The RD53 collaboration is developing a large scale pixel front-end chip, which will be a tool to evaluate the performance of 65 nm CMOS technology in view of its application to the readout of the innermost detector layers of ATLAS and CMS at the HL-LHC. This paper will review recent results concerning radiation effects on devices and circuits in this technology, and will give a picture of the current understanding of damage mechanisms and of rad-hard design criteria. Experimental results of the characterization of two small scale readout chips will be discussed in the frame of the design work that is currently leading to the development of the large scale demonstrator chip RD53A to be submitted by the end of 2016.

B14-Electronics and system integration / **69**

Chip Development for High Time Resolution Silicon Detectors

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The NA62 GigaTracKer (GTK) is a hybrid pixel detector required to time MIPS to better than 200ps (RMS) with a material budget of less than 0.5% X_0. I will introduce the GigaTracker Readout ASIC (TDCPix) designed to respond to these requirements, giving some detail about the main challenges, the architectural choices made during the design, the measured performance of the ASIC and detector assembly, as well as what we believe limits the time resolution. If time permits, I will compare and contrast the GTK electronics with those required for the CMS HGCAL upgrade project front end electronics.

B14-Electronics and system integration / **53**

High Speed Optical and Electrical link developments

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The vast quantities of data being produced by modern particle physics detectors require the use of high-speed serial data transmission technologies in order to enable their successful design. This contribution will review the developments in this area that target the Phase II upgrades of the LHC experiments and may find application in other areas in the same way as their current counterparts have done. The technologies being pursued cover both optical and electrical data transmission links, with the target application typically driving choice based on balancing the pros and cons of the two approaches. The customized front-end components being developed will be described in the context

of their uses within complete link systems that are not only capable of reading-out detectors but also provides the means to control them.

B14-Electronics and system integration / 67

Development of wireless data and power transmission for tracking detectors

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A large contribution to the total material budget of trackers come from services for data communication and power. Optimizing the material budget without large scarification of reliability is important when designing trackers.
The WADAPT (Wireless Allowing Data And Power Transmission) project investigates the feasibility for wireless data and power transmission to trackers. The project benefit from the fast growing development of wireless technology for the consumer market. The components becoming available in consumer products uses millimeter waves and capable of Gbps data transfer over short distance at low power hence possibly well suited for use in trackers. The millimeter wave transceivers and antennas are med with technology widely used in trackers. The size of the components in wireless data link is compatible with tracking detectors.
We will present results from feasibility studies of wireless data transfer in tracker environment using commercial components that are not optimized for trackers. Results will be shown on data transfer between and trough tracker layers, Bit Error Rate for a Gbps wireless data link, measurement of crosstalk between closely placed links etc.
The WADAPT project is now developing a wireless data link optimized for trackers that can be easily integrated with components currently developed for HL-LHC. We will present the plan and status of this development.

B15-Online and offline tracking and vertexing / 28

FTK status and perspectives for track trigger in ATLAS at HL-LHC

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The expected instantaneous luminosities delivered by the Large Hadron Collider will place continually increasing burdens on the trigger systems of the ATLAS detector. The use of tracking information is key to maintaining a manageable trigger rate while keeping a high efficiency. At the same time, however, track finding is one of the more resource-intensive tasks in the software-based processing farms of the high level trigger system. To support the trigger, ATLAS is building and currently installing the Fast TracK Finder (FTK), a hardware-based system that uses massively parallel pattern recognition in Associative Memory to reconstruct tracks above transverse momenta of 1 GeV across the entire detector at 100 kHz with a latency of ~100 microseconds. In the first-stage of track finding, FTK compares hits in ATLAS silicon detectors against ~1 billion pre-computed track pattern candidates. Track parameters for these candidates, including goodness-of-fit tests, are calculated in FPGAs using a linear approximation, leading to nearly offline-quality efficiency and resolution with a low fake rate.
In order to prepare for the future high-luminosity environment, ATLAS is also studying upgrades to the hardware-based track trigger capabilities of the detector. The FTK++ upgrade will expand

on the power of the FTK system, with newer and faster FPGAs and a significantly larger number of patterns, allowing the upstream software-based trigger system access to full-scan tracking at 100 kHz, even with an average of up to 200 overlapping proton-proton interactions.
The L1Track upgrade will use shared hardware technologies with FTK++ and provide regional tracking for confirmation of the earliest stage muon and calorimeter trigger systems, particularly for single electron triggers, with a latency of only 6 microseconds. L1Track is expected to maintain high efficiency (>= 95%) and low fake rate for tracks with transverse momenta above 4 GeV at a rate of 1 MHz. In an alternative upgrade model in which the full 1 MHz rate is passed to a computing farm, FTK++ will continue to provide the full-scan tracking at 100 MHz, and L1Track will be replaced by the EFTrack system, which will similarly provide fast regional tracking to the computing farm.
This contribution will describe the parameters of the FTK system and the status of installation and commissioning of the hardware, as well as future, longer-term, plans for hardware-based track triggers at ATLAS.

B15-Online and offline tracking and vertexing / **63**

The CMS track trigger for the High Luminosity LHC

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The High Luminosity LHC is expected to deliver luminosities of 5 × 10ˆ34 cm-2s-1, with about 200 proton-proton interactions per bunch crossing, on average. For their physics program to take advantage of these high collision rates the LHC experiments need to redesign their trigger systems so that they identify charged particle tracks at the very first stage of triggering. The CMS track trigger upgrade will make use the silicon tracker detector upgrade to measure with precision, with a latency of about 5 microseconds, the transverse momenta of all charged particles, for particles with momentum above 2 GeV/c. We discuss the challenges that this project entails and different algorithmic and architectural solutions that can help overcome them. We also describe the current status and plans for these projects.

B15-Online and offline tracking and vertexing / **48**

Tracking in high-multiplicity events

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The ALICE experiment is preparing a major upgrade of its inner silicon tracker (the Inner Tracking System) and of its Online and Offline systems for the upcoming Run3 of the LHC starting in 2021.

During its Run3, LHC will deliver Pb-Pb collisions at $\sqrt{s_{NN}} = 5.5$ TeV with a peak luminosity $L = 6 \times 10^{27} cm^{-}2s^{-1}$ and an interaction rate of 50 kHz, to be compared to the 8 kHz interaction rate currently delivered by the LHC. The aim of ALICE is to cope with such a high interaction rate improving at the same time the resolution and the efficiency of its silicon tracker.
In this context, one of the requirements for a prompt calibration of external detectors and to speed up the offline data processing is to run online the reconstruction of tracks in the Upgraded Inner Tracking System.

A new algorithm based on Cellular Automata has been developed to tackle this issue. In this algorithm the tracking is split in multiple phases to profit from data locality. At first, hit points are organised in sectors of azimuthal angle and longitudinal coordinate; then the algorithm looks for track segments within these sectors of the detector, independently. Track segments with compatible track parameters are marked as neighbours. Neighbouring track segments are then merged at the final stage using a set of rules defined by the Cellular Automaton mechanism, somewhat similar to the set of rules used in the Conway's Game of Life.

The obtained computing and tracking performance are compliant with the requirements of ALICE being able to reconstruct tracks of transverse momentum down to 100 MeV/c in events with high track density ($dN/d\eta$ up to 2000). The tracking and computing performance of this algorithm will be shown in the case of central Pb-Pb events at $\sqrt{s_{NN}} = 5.5$ TeV.

B16-Online and offline tracking and vertexing / **76**

Using precision timing information in high rate and high pileup conditions

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High energy particle collider experiments are facing ever more challenging conditions, operating at todays accelerators capable of providing instantaneous luminosity of 10^34 cm-2s-1 and above. The high center of mass energy, the large number of simultaneous collision of beam particles in the experiments and the very high repetition rates of the collision events pose huge challenges. They result in extremely high particle fluxes, causing very high occupancy in the particle physics detectors operating at these machines. A precise timing information with a precision of around 10 ps and below is seen as a major aid in the reconstruction of the physics events under such challenging conditions. In this talk I will review the efforts of the LHC collaborations to augment the timing performance of their detectors during future upgrade campaigns. to utilize precision timing for the event reconstruction in a high rate and high pileup environment as expected at the high luminosity LHC and at future hadron colliders. Different detector technologies allowing precision timing measurements will be discussed and their potential benefit will be illustrated with a particular focus on tracking.

B16-Online and offline tracking and vertexing / **42**

Investigating the Micron Automata Processor for HEP Pattern Recognition Applications

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The Micron Automata Processor is a dedicated pattern matching engine that is based on a non-Von Neumann processor architecture, and was designed primarily to satisfy the growing needs of high-speed text-based pattern search applications. We investigate its suitability for HEP pattern recognition applications, using a sample track-confirmation trigger to demonstrate a proof-of-principle. We compare its performance, in this sample application, with that of other processor architectures, including general purpose CPUs, GPUs, and custom devices based on content-addressable memories.

B16-Online and offline tracking and vertexing / 71

Tracking, calibration&alignment, and data processing in the LHCb upgrade

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For Run III foreseen to start in 2020, the LHCb experiment will run at an instantaneous luminosity of 2x10^33 cm-2s-1 with a fully software based trigger. A major upgrade of the detector and of data acquisition system will allow having a full readout at the collision rate of 40 MHz. LHCb is planning to have the same Run II strategy with a real-time alignment and calibration procedure and an offline-like quality reconstruction in the latest stage of the software trigger. This strategy includes the alignment of the full tracking system (both for the vertex detector and all the tracking stations) evaluated in few minutes at the beginning of each fill and the complete calibration of the PID sub-detectors for each run that corresponds to a maximum of 1 hour of data taking. The reconstruction used in Run I was optimized to fit the time constrained required by the software trigger: 45 ms and 650 ms for the first and second trigger stage.
In Run III, a total time budget of 13 ms event to take the trigger decision is foreseen.
This implies a large gain in speed in the reconstruction to be achieved. Different approaches are under study to mach this challenging goal, e.g. using parallelism in the CPU and GPU, use of machine learning to veto bad events on an early stage, optimization on different architectures.
The Run II strategy ends to have as output of the second stage of the software trigger the same quality performance as in the "offline" processing. This results in the possibility to perform analyses directly on the output of the trigger without requiring an offline reconstruction. Saving only the interesting information of the selected events reduces significantly the event size down to a factor of 10. Thus an equivalent factor higher rate of signals can be exploited in physics analyses with the same resources. During Run II, the event format has been made more flexible, which has allowed to satisfy more physics analysis requirements. In Run III, LHCb plans to use this same strategy for all the analyses with abundant signals to record the events in a reduced format that can be fed directly to the physics analysis.
The importance and the challenging of this strategy is discussed. We illustrate the operational and physics performance of the real-time alignment and calibration, the overview of the reconstruction and the real-time analysis model in Run2. Plans and different approaches under study for Run III are also presented.

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The ILC Vertex Detector requirements

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After few decades of R&D, the International Linear Collider (ILC) project has reached a level of maturity proving the feasibility of the machine and of the detectors. The ILC physics goals cover a very wide and ambitious program including top-quark quark physics, electroweak precision measurements, direct and indirect searches beyond the Standard Model (BSM) like SUSY, dark matter manifestations, exotic particles and phenomena, etc., and an extensive Higgs physics program covering mass, couplings to fermions and bosons, quantum numbers and total width measurements. These measurements are expected to reach an unprecedented level of precision in most of the cases, which will allow probing physics BSM, since typical deviations from the Standard Model are expected to be in the order of magnitude of the ILC sensitivity.

To accomplish the ambitious physics program of the ILC, the vertex detector will be essential for providing the necessary physics performances in terms of flavor tagging, displaced vertex charge determination and low momentum tracking capabilities.
Taking advantage of the much less demanding running conditions at the ILC than at hadron colliders like LHC, the vertex detector is expected to reach particularly high performances as far as spatial resolution and material budget are concerned (typical impact parameter resolution of the order of 5 microns and material budget in the order of 0.15-0.2 % of radiation length per layer).

In addition, the particular time structure of the beams has major consequences on the specifications of the detectors and their read-out architecture. It allows to concentrate the read-out during 199 ms beamless periods separating 1 ms long bunch trains or to suppress the average power consumption by switching off (at least partially) the detectors in-between trains (the so called power pulsing).

Finally, the beam related background of the ILC, which translates into a high rate of low momentum-e-e+ pairs hitting the vertex detector, drives the expected occupancy (and the related necessary read-out speed) as well as the radiation load.

The talk will focus on the vertex detector requirements following from both the physics and the experimental constraints. Wherever different, the aspects to each detector concepts (SiD and ILD) will be discussed.

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Development of detector technologies for ILC vertexing.

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The physics programme at the ILC relies heavily on pure and efficient identification of heavy-flavour quarks, requiring pixel vertex detectors with 3-4 μm hit resolution and a material budget of 0.1-0.2% of a radiation length per layer.

Although technology choices are still several years in the future, a number of detector concepts are currently being actively studied. I will discuss these concepts and the associated ongoing R&D programmes, including potential sensor technologies (CMOS, CCD, DepFet etc) as well as mechanical and system issues.

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CLIC silicon pixel R&D

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The physics aims at the future CLIC high-energy linear e+e- collider set very high precision requirements on the performance of the vertex and tracking detectors. Moreover, these detectors have to be well adapted to the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The principal challenges are: a point resolution of a few μm,

ultra-low mass (~0.2% X0 per layer for the vertex region and ~1% X0 per layer for the outer tracker), very low power dissipation (compatible with air-flow cooling in the inner vertex region) and pulsed power operation, complemented with ~10 ns time stamping capabilities. A highly granular all-silicon vertex and tracking detector system is under development, following an integrated approach addressing simultaneously the physics requirements and engineering constraints. For the vertex-detector region, hybrid pixel detectors with small pitch (25 μm) and analog readout are explored. For the outer tracking region, both hybrid concepts and fully integrated CMOS sensors are under consideration. The feasibility of ultra-thin sensor layers is validated with Timepix3 readout ASICs bump bonded to active edge planar sensors with 50-150 μm thickness. Prototypes of CLICpix readout ASICs implemented in 65 nm CMOS technology with 25 μm pixel pitch have been produced. Hybridisation concepts have been developed for interconnecting these chips either through capacitive coupling to active HV-CMOS sensors or through bump-bonding to planar sensors. Recent R&D achievements include results from beam tests with all types of hybrid assemblies. Simulations based on Geant4 and TCAD are used to validate the experimental results and to assess and optimise the performance of various detector designs. The R&D project also includes the development of through-silicon via (TSV) technology, as well as various engineering studies involving thin mechanical structures and full-scale air-cooling tests. An overview of the R&D program for silicon detectors at CLIC will be presented.

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Vertical integration technologies for tracking detectors

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In the past ten years, 3D vertical integration technologies have generated a wide interest in the silicon pixel sensors and front-end electronics communities. They have the potential to lead to the fabrication of multilayer high performance devices with no dead area, where each layer is optimized for its function (particle sensing, analog signal amplification and filtering, digital memory and readout,...). This paper will review the results that the community got so far, and assess the current status of R&D work on 3D integration applied to particle detection systems. Finally, the prospects of 3D integration for the future generation of tracking detectors will be discussed.

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Workshop Summary

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