

Wire-bonding and Assembly Studies for the Outermost Layer of Silicon Vertex Detector in the Belle-II experiment

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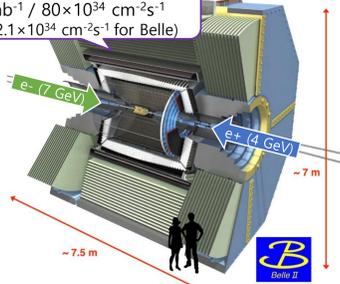
(on behalf of the Belle-II SVD Collaboration)

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The vertex detector (VXD) for the Belle II experiment at the SuperKEKB in Japan is aimed at providing precise information on vertexing and low-momentum tracking. The VXD consists of a two-layer pixelated detector (PX) and a four-layer silicon microstrip detector (SVD), and is designed to operate under the high-luminosity environment of Belle-II. For the SVD, a novel chip-on-sensor concept called "Origami" is developed to reduce multiple Coulomb scattering as well as capacitive noise. The wire-bonding and assembly procedures for the outermost layer of the SVD, especially wire-bonding of the Origami modules, have been fine-tuned. In order to optimize the bonding parameters, we measure pull forces required to break the wires by pulling them and observing the shape types of broken wires and bond footprints. An issue is found with the precision of the positioning of the tilted forward sensor, which has been mitigated by introducing a shim method, resulting in an improved mechanical precision. In this paper, we present the results of wire-bonding study and the aforementioned shim method.

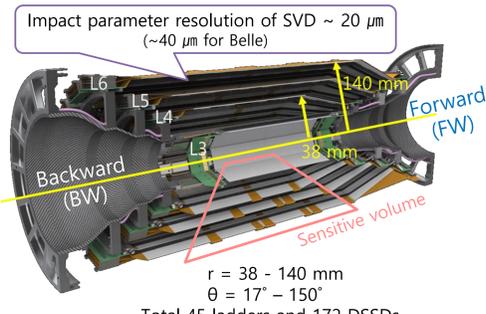
Silicon Vertex Detector for Belle II experiment at SuperKEKB

Target integrated/peak luminosity
= 50 ab⁻¹ / 80 × 10³⁴ cm⁻²s⁻¹
(1 ab⁻¹ / 2.1 × 10³⁴ cm⁻²s⁻¹ for Belle)



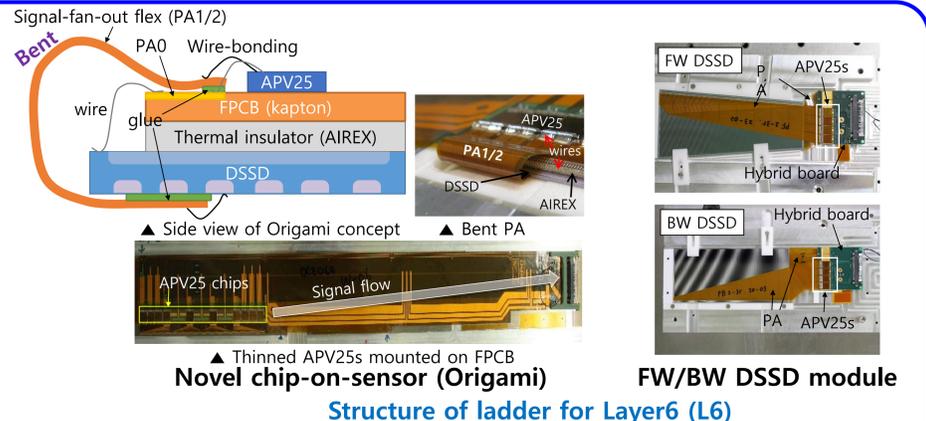
Belle II detector

- 7 GeV electron and 4 GeV positron
- Observing events from B meson decays - especially rare/violated decay modes
- Study new physics beyond the SM
- Start at 2018



Silicon vertex detector (SVD)

- Vertex detector = pixel detector + SVD → providing improved position resolution
- Four cylindrical layers with ladder structure
- Ladder = assembly of double-sided silicon strip detector (DSSD) modules
- APV25 read-out chip for fast processing



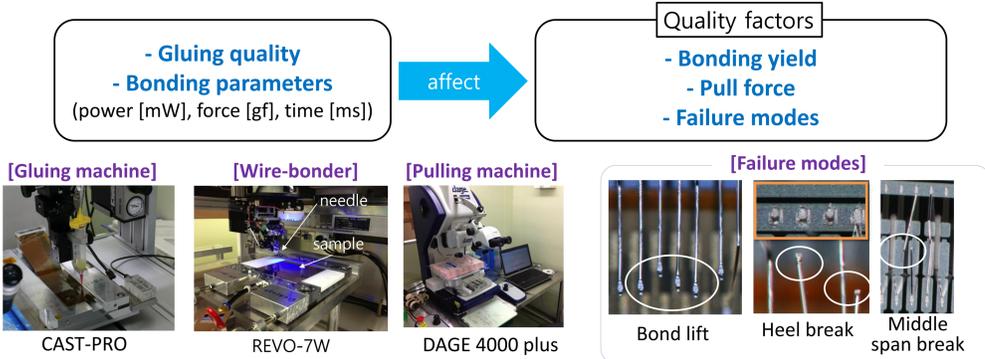
Novel chip-on-sensor (Origami)

Structure of ladder for Layer6 (L6)

- Origami concept to reduce capacitive noise* and multiple scattering**
- * shorten distance between the DSSD and the chip
- ** thinned APV25 chips and FPCB made of kapton
- Detector concept for signal read-out
 - three central DSSDs in sensitive volume, with "Origami" concept
 - two DSSDs on the edges, with electronics on hybrid boards

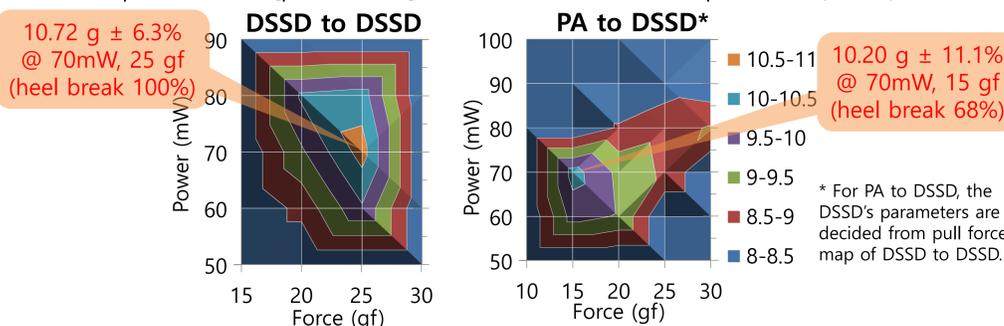
Study of Wire-bonding for SVD Layer6 ladders

The components of bonding samples are attached using the glue (Araldite 2011) and electrically connected using the wire bonding. **Quality of the wire-bonding** is determined by visual inspection and pull force in gf, affects to strength of the wire bonds.



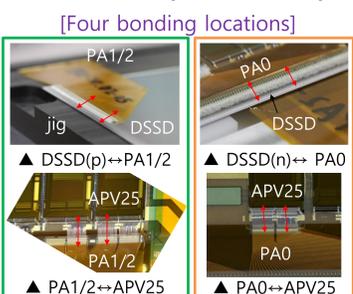
Pull Force Map to optimize the bonding parameters

- The bonding parameters are needed to optimize for each substrate such as DSSD and PAs.
- DSSD to DSSD for searching the parameters for DSSD (Si substrate).
- DSSD to PA for searching the parameters for PA bonding pads (Ni/Au)
- For each parameter set [power, force], 10 wires with a fixed time parameter (25 ms)



Quality Assurance (QA) of wire-bonding for Origami module

- Origami module = one DSSD + Origami concept
- Four locations of wire-bonding for the Origami module
 - ▷ DSSD (p-side) ↔ PA1/2 ↔ APV25
 - ▷ DSSD (n-side) ↔ PA0 ↔ APV25
- Based on the **pull-force maps** and **failure modes**, the bonding parameters are determined.



QA Requirements

- ① test with at least 30 wires for each location
- ② average pull force > 5 g, and standard deviation < 20%
- ③ bonding yield > 99%
- ④ >80 (50)% heel or mid-span breaks if mean=5-9 g (>9 g)

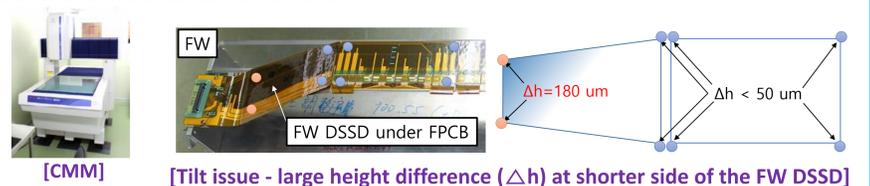
Location	Bonded wires	Bonding parameters Power, Force, Time	Pull-force (g)
DSSD ↔ PA1/2	128	65, 20, 25	10.15 ± 3.4%
APV25 ↔ PA0	125	70, 15, 25 (APV) 80, 15, 25 (PA0)	10.04 ± 7.9%
DSSD ↔ PA0	126	70, 20, 25	10.15 ± 13.3%
APV25 ↔ PA1/2	160	70, 20, 25	7.58 ± 10.6%

* 100% heel break except for APV25 ↔ PA0 (~82%)

→ The optimized bonding parameters satisfy the QA requirements

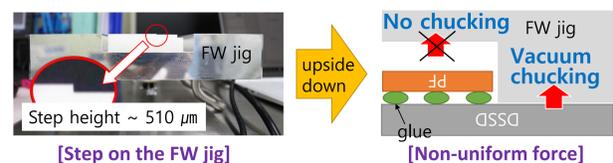
Mechanical Precision of FW DSSD in L6 ladder assembly

Mechanical precision of the ladders is important to avoid crush with other ladders during commission of SVD, and to improve position precision of decay vertices. Position of DSSDs are measured by using **CMM (Coordinate measuring machine)**. While assembling an L6 ladder, a **tilt issue on the FW DSSD** was found and we studied to solve it.



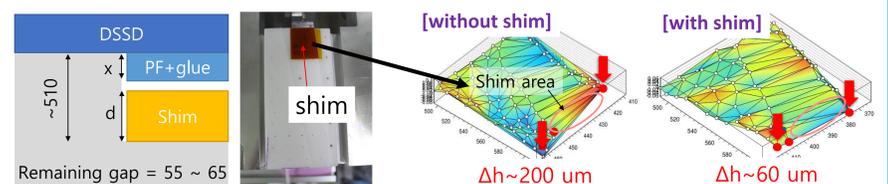
Causes of the issue

- **Non-uniform force** of the FW jig holding the FW DSSD module by vacuum.
- **Tension** from the hybrid board fixed on ladder jig.



Shim method

- Kapton tape, as a shim, on the step of the FW jig to compensate the gap



- Study for optimizing the shim
 - remaining gap(d_r) = 510 - x - d [μm]
 - optimized value: d_r = 30-60 μm
- Measurement results
 - height measured using CMM
 - Δh is drastically reduced with the shim.

- The shim method has been applied to assembly of class A L6 ladders.

L6 ladder ID	Δh at shorter side of the FW DSSD
A02	12 μm
A03	15 μm

→ The shim method is good for the tilt issue

Summary and Plan

- We are assembling L6 of the SVD for Belle II experiment.
- We studied to optimize parameters of wire-bonding and mechanical issues, the tilt on the FW DSSD, in the L6.
 - The optimized bonding parameters satisfy the QA requirements.
 - The shim method can compensate the height difference at shorter sides of the FW DSSD, and has been employed to assembly of L6 ladders.
- The Belle II experiments will start physics run at end of 2018.