A monolithic pixel sensor with fine space-time resolution based on silicon-on-insulator (SOI) technology for the ILC vertex detector

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Introduction

- International linear collider (ILC)
  - Precise measurement of Higgs boson and the search for new particle
- A monolithic pixel sensor optimized for vertex detector system
  - We are developing new a sensor with fine position and time resolutions based on the SOI technology.

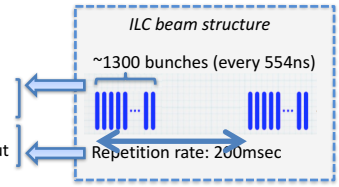
Summary

- SOFIST: New pixel sensor optimized for ILC vertex detector system
  - Pixel storing both position and timing information
- Development status
  - Ver.1: Analog signal pixel → 20x20μm²
  - Ver.2: Time-stamp and Self-triggering pixel → 25x25μm²
- Future prospect
  - Ver.3/3D: Pixel implementation by 3D-stacking → 20x20μm²

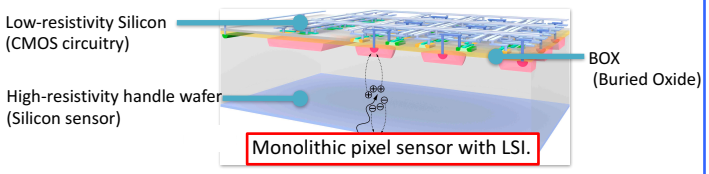
1. Target/Motivation

Requirements of the silicon pixel sensor for the ILC vertex system.

1. Single point resolution: σ ~ 3um
   - Smaller pixel size (~20um)
2. Event separation during beam train
   - Bunch identification by timing
3. Data readout between beam trains
   - On-chip ADC and Sparse readout



2. Silicon-on-insulator (SOI) pixel sensor

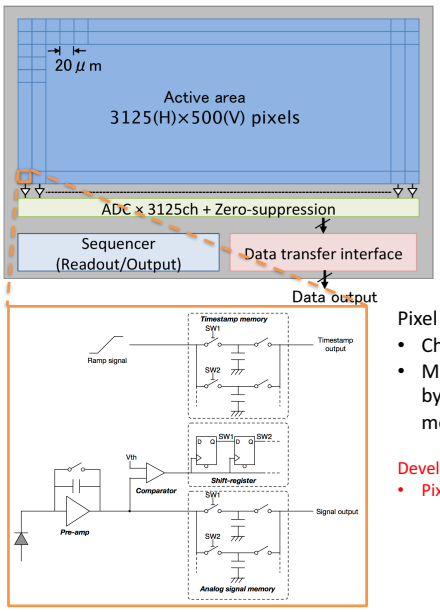


Advantages of SOI pixel sensor

- Monolithic detector: → Low material budget
- No mechanical bump bonding: → Smaller pixel
- Standard CMOS: → Complex functions in pixel circuit
- Low parasitic capacitance: → High conversion gain, Low noise

3. SOFIST: SOI sensor for ILC vertex detector

SOI sensor for Fine measurement of Space and Time



SOFIST structure

- Chip size: 62.5x10mm²
- Pixel: 20x20um□
- Readout
  - ✓ Column-ADC
  - ✓ 0-suppression logic

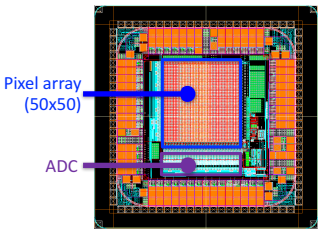
Pixel architecture

- Charge signal + Hit-timing
- Multi. hits accumulation by storing on-pixel analog memories.

Development issue

- Pixel layout within 20x20um□

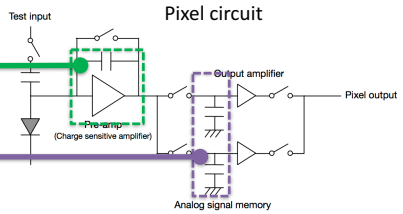
4-1. SOFIST Ver.1 (for Analog signal readout)



Chip size	2.9x2.9mm²
Pixel circuit	Size: 20x20um² Analog memory × 2
Readout	Column-ADC

Process: Lapis 0.2um SOI
Wafer: N-type (FZ)

Pixel circuit



- Charge sensitive amplifier
  - Gain: 32uV/e-
  - 1MIP(4000e-) ~0.13V
- Analog signal memory
  - Storing 2 hit signals

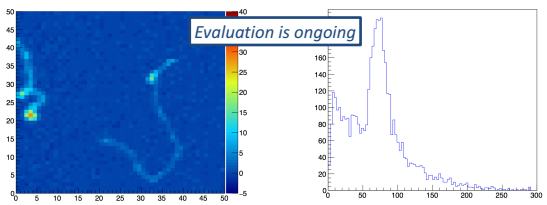
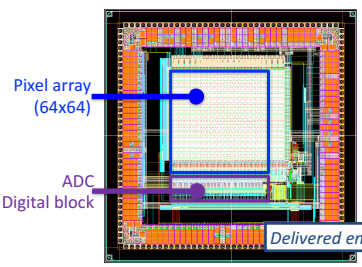


Image of β-ray track

β-ray(⁹⁰Sr) signal spectrum

4-2. SOFIST Ver.2 (for Timestamp readout)

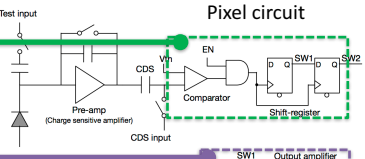


Chip size	4.45x4.45mm²
Pixel circuit	Size: 25x25um² Self-triggering logic Timestamp memory
Readout	Column-ADC 0-suprression logic

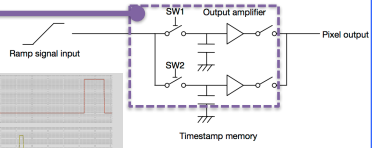
Process: Lapis 0.2um SOI
Wafer: P-type (DSOI)

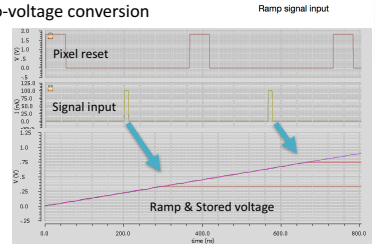
Pixel circuit

- Self-triggering logic
  - Comparator + D-FFx2



- Analog time-stamp
  - Holding ramp signal
  - Time-to-voltage conversion





5. SOFIST Ver.3/3D (Pixel integration)

Further optimization of pixel circuit

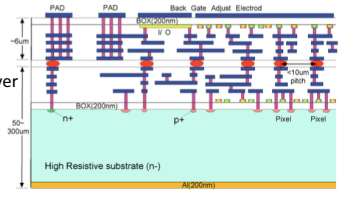
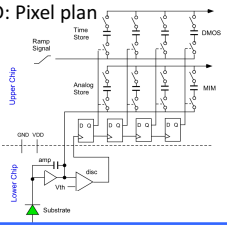
- Pixel integration with both analog signal readout and time-stamp
- Circuit Implementation within 20x20μm²
  - **3D circuit technology: stacking some circuit layers on SOI wafer**
  - **3D design sensor will be submitted in 2017**

SOI-3D sensor

Top circuit layer

Bottom circuit layer

Sensor layer



SOFIST-3D: Pixel plan