**Abstract**

The AM06 is the 6th version of a large Associative Memory chip designed in 65 nm CMOS technology. The AM06 operates as a highly parallel ASIC processor for pattern recognition in the ATLAS experiment at CERN. It is the core of the Fast TracKer electronic system, which is tailored for on-line track finding in the trigger system of the ATLAS experiment. The Fast TracKer system is able to process events up to 100 MHz real time.

The AM06 is a complex chip, and it has been designed combining full-custom memory arrays, standard logic cells and IP blocks. It contains memory banks that store data organized in 18 bit words; a group of 8 words is called a pattern. The chip silicon area is 168 mm²; it contains 421 millions of transistors and it stores 2¹² patterns. Moreover, the AM is suitable also for interdisciplinary applications (i.e., general purpose image filtering and analysis). In the near future we plan to design a more powerful and flexible chip in 28 nm CMOS technology.

The Fast TracKer (FTK) System in the ATLAS Experiment

After the next upgrade, the High-Luminosity LHC will reach a luminosity of 2 - 10³⁵ cm⁻² s⁻¹, and experiments will produce a huge amount of data, thus requiring a tight selection of events to be transferred to the mass storage system. In order for the online system to achieve this, it has to work with as complete information about the events as possible. The Fast TracKer (FTK) is an electronic system in the ATLAS experiment that rapidly finds and reconstructs tracks in the inner silicon detector layers (pixel and strip) for every event that passes the level-1 trigger, at 100 kHz event rate. It uses 12 logical layers (the 4 pixel layers, and the 8 strip layers from the SCT detector, which has 4 physical layers with one axial and one stereo side each) over the full rapidity range covered by the barrel and the disks.

The FTK receives the hits at full rate as they are sent from the pixel and SCT Read Out Drivers (RODs), following a level-1 trigger accept. After processing, the FTK fills the DAQ Read Out System (ROS) with the helix parameters and hits for all tracks with p_T above a minimum value, typically 1 GeV.

The patterns are determined in advance from a full ATLAS simulation of single tracks, and are stored in the specific ASICs called Associative Memory (AM) chips.

The Associative Memory (AM) chip

The latest version of the AM chip is the AM06; its architecture is based on the serializer/deserializer (SER/DES) interface and on the AM core. The input boxes are organized in 11 serial links, each of them receiving serialized data. Input 16 bit words have a rate of 100 MHz, and are serialized with an 8b/10b encoding, thus giving a serial data rate equal to 2 Gbit/s. SER/DES input blocks convert the serial input to parallel data, which are sent to the core memory blocks.

The AM06 has a standard JTAG interface for configuration and testing. One of the JTAG registers contains the ID code of the AM chip family.

The AM06 characterization and volume test

The AM06 chip has been characterized with the test system at an INFN laboratory in Milano. The test setup is made of an FPGA board with a Xilinx Virtex6 FPGA, and a dedicated mezzanine board with a zero-insertion-force socket for the device under test.

The test procedure is controlled remotely by a PC connected to the internet. A set of routines written in Python allow us to test the AM chip in different conditions. The test sequence has 100% coverage against single bit errors in the AM core blocks, in the readout, and in the main functions used to configure and run the AM chip.

From the eye diagram of one of the AM06 serial links at 2 Gbit/s, we observe that the jitter is about 25 ps. A similar result has been obtained for all the chip serial links, thus confirming the good quality of the serial communication.

Conclusion

The AM06, the 6th version of a large Associative Memory chip for FTK system is designed in 65 nm CMOS technology. The FTK system includes 7500 AM chips, therefore, the test setup and the measurement software have been developed to define a standard test procedure suitable for the industrial test of a large number of chips. The laboratory characterization shows full functionality of both the AM06 and the test system.

The setup has been implemented successfully at the company, and the operator is able to test the chips in an automated way. The test setup is user-friendly and does not require a specialized training of the operator.

**Eye diagram of AM06 serial link at 2 Gbit/s**

7500 AM06 chips are being fabricated for the FTK system. Therefore, the test setup is finalized to test a large number of chips in a company. The test procedure is automated as much as possible and a graphic interface has been developed to simplify the use of the test system.

The test setup has been assembled successfully at Microtec srl in Altapascia, Italy, where the production lot of 7500 AM06 chips will undergo the test. The test time for each chip has been kept short enough, to limit test costs; moreover, the test procedure is very user-friendly and does not require a specialized training of the operator.