An Associative Memory Chip for the Trigger System of the ATLAS Experiment

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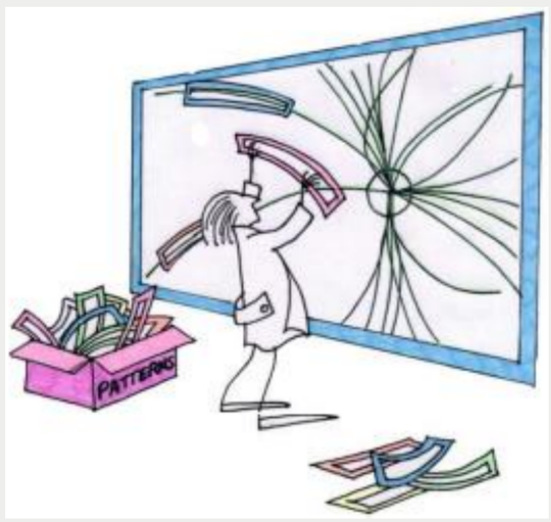
Abstract

The AM06 is the 6th version of a large Associative Memory chip designed in **65 nm** *CMOS technology.*
The AM06 operates as a highly parallel ASIC processor for pattern recognition in the ATLAS experiment at CERN. It is the core of the Fast TracKer electronic system, which is tailored for on-line track finding in the trigger system of the ATLAS experiment. The Fast TracKer system is able to process events up to **100 MHz** *in real time.*
The AM06 is a complex chip, and it has been designed combining full-custom memory arrays, standard logic cells and IP blocks. It contains memory banks that store data organized in 18 bit words; a group of 8 words is called a pattern. The chip silicon area is **168 mm^2***; it contains 421 millions of transistors and it stores* **2^{17}** *patterns.*
Moreover, the AM is suitable also for interdisciplinary applications (i.e., general purpose image filtering and analysis). In the near future we plan to design a more powerful and flexible chip in **28 nm** *CMOS technology.*

The Fast TracKer (FTK) System in the ATLAS Experiment

After the next upgrade, the High-Luminosity LHC will reach a luminosity of 2-3 $\cdot 10^{34}$ cm^{-2} s^{-1}, and experiments will produce a huge amount of data, thus requiring a tight selection of events to be transferred to the mass storage system. In order for the online system to achieve this, it has to work with as complete information about the events as possible.
The Fast TracKer (FTK) is an electronic system in the ATLAS experiment that rapidly finds and reconstructs tracks in the inner silicon detector layers (pixel and strip) for every event that passes the level-1 trigger, at 100 kHz event rate. It uses 12 logical layers (the 4 pixel layers, and the 8 strip layers from the SCT detector, which has 4 physical layers with one axial and one stereo side each) over the full rapidity range covered by the barrel and the disks.



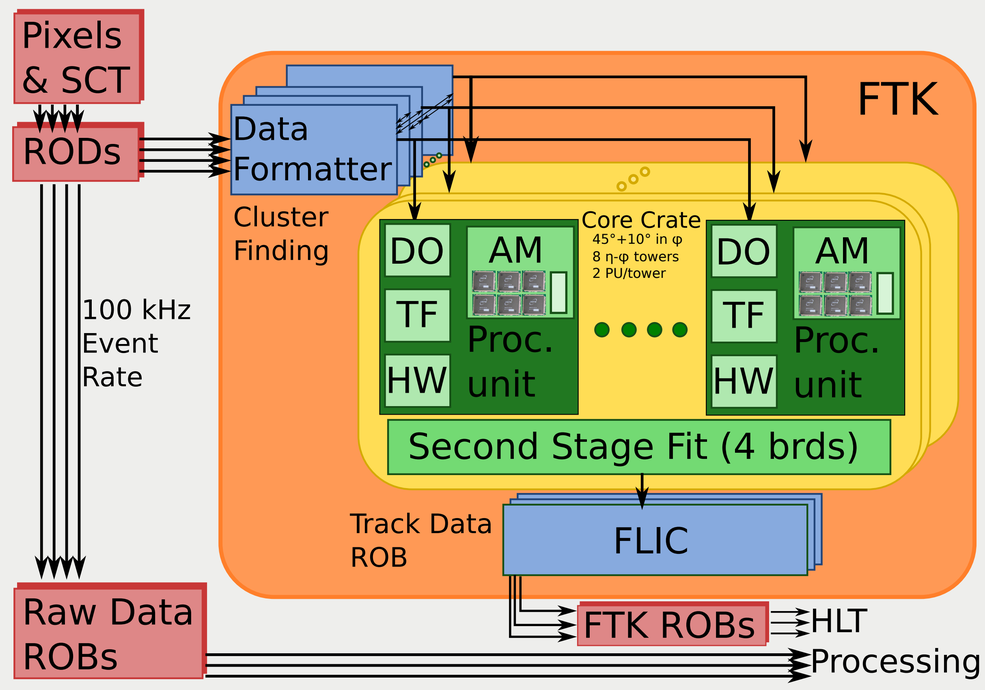
The FTK approach

FTK Architecture

The FTK receives the hits at full rate as they are sent from the pixel and SCT Read Out Drivers (ROD), following a level-1 trigger accept. After processing, the FTK fills the DAQ Read Out System (ROS) with the helix parameters and hits for all tracks with p_T above a minimum value, typically 1 GeV.

- The pixel and strip data are transmitted from the RODs on S-LINK fibers and received by the Input Mezzanines (IM) and the Data Formatters (DF): the IMs perform one or two dimensional cluster finding, for the strip and the pixel layers, respectively.
- The DFs reorganize the data into the towers and transmit the cluster centroids (*hits*) to the Data Organizers (DO).
- The DOs are smart databases mapping the full resolution hits onto lower-resolution hits (called *superstrips*) used for the pattern matching step of the FTK tracking. Given a matched pattern (called *road*) the DOs retrieve the full resolution hits belonging to it; these hits are used for a refined track fitting later.

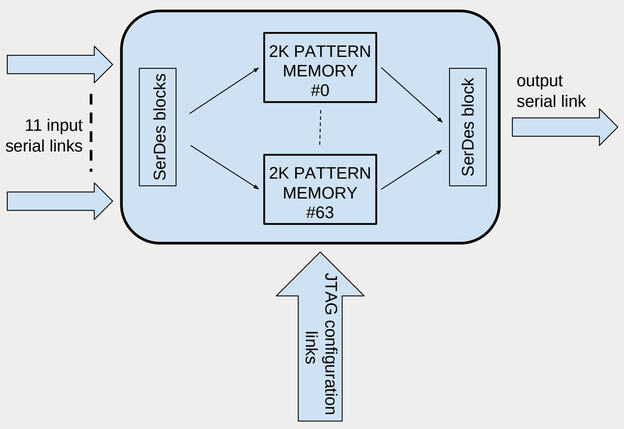
The patterns are determined in advance from a full ATLAS simulation of single tracks, and are stored in the specific ASICs called Associative Memory (AM) chips.



Architecture of the FTK system

The Associative Memory boards contain a very large number of stored patterns, which correspond to the possible combinations of a superstrip in each of 8 silicon layers for real tracks. The AM is a massively parallel system in that all patterns see each silicon hit nearly simultaneously. As a result, pattern recognition in FTK is completed shortly after the last hit has been transmitted from the silicon RODs. When a pattern has 7 or 8 layers hit (such patterns that contain track candidates are referred to as roads), the AM sends the road ID number back to the Data Organizer which fetches the associated full resolution hits and sends them and the road number to the Track Fitter (TF) which provides the high resolution fit of track helix parameters. If in the same road there are multiple tracks satisfying the fit quality criteria, they are passed to the Hit Warrior (HW) function for duplicate track removal. Only 8 out of the 12 silicon layers were used during this first stage (the pattern matching and the track fitting); the rest 4 layers are included in a second stage.
When a track passes the first stage criteria, the road number and the associated hits are sent to the Second Stage Boards (SSBs), together with the hits in the rest 4 layers which are provided by the DFs. The 8-layer track is extrapolated to the 4 additional layers and a full 12-layer fit is carried out. SSB output tracks consisting of the hits on the track, the fit parameters, the helix parameters, and a track quality word that includes the layers with a hit are sent to the FTK-to-Level2 Interface Crate (FLIC). The FLIC organizes the tracks and sends them to the ROSs using the standard ATLAS protocols, and carries out monitoring functions. In the ROS the FTK tracks get buffered waiting for the request from the High Level Trigger.

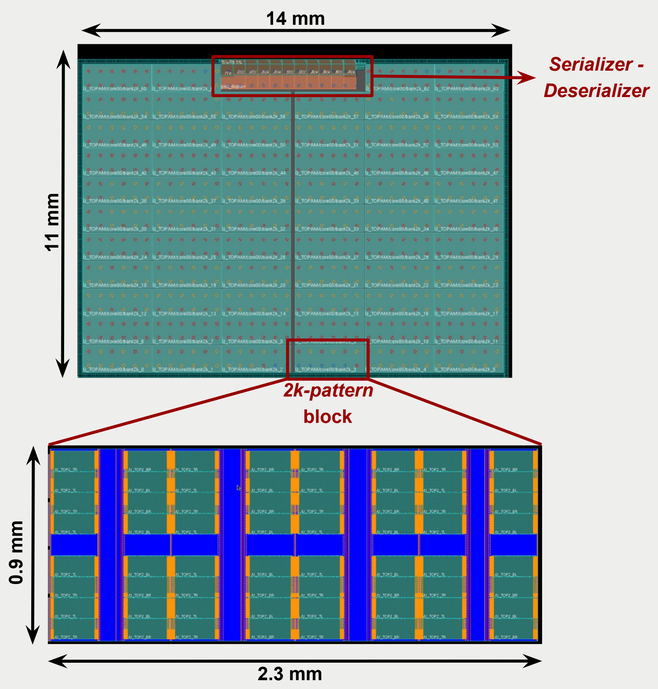
The Associative Memory (AM) chip



AM06 architecture

The latest version of the AM chip is the AM06; its architecture is based on the serializer/deserializer (SER/DES) interface and on the AM core. The input buses are organized in 11 serial links, each of them receiving serialized data. Input 16-bit words have a rate of 100 MHz, and are serialized with an 8b/10b encoding, thus giving a serial data rate equal to 2 Gbit/s. SER/DES input blocks convert the serial input to parallel data, which are sent to the core memory blocks.

The associative memory core is made of 64 blocks, each of them containing 2 k patterns. The core stores the patterns which the AM06 should find among the incoming data.
The AM06 compares the input data with the pre-stored patterns and the addresses of matching patterns are delivered at the output of the AM core. The address of the matching pattern is serialized by the output SER/DES block.

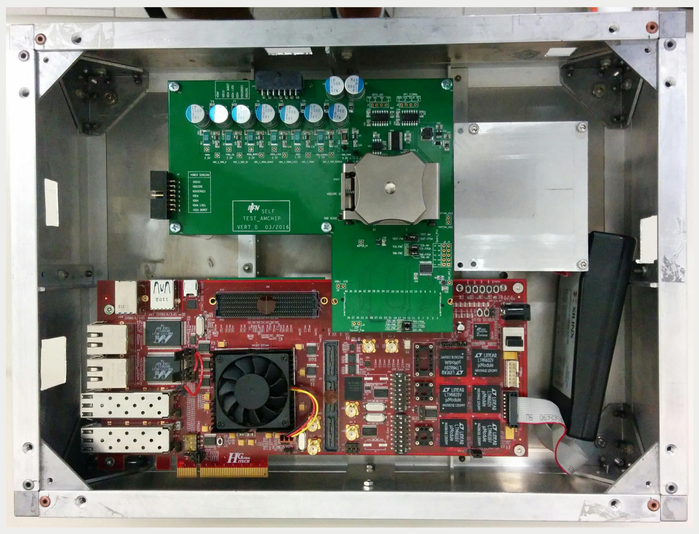


AM06 layout

The AM06 has a standard JTAG interface for configuration and testing. One of the JTAG registers contains the ID code of the AM chip family.

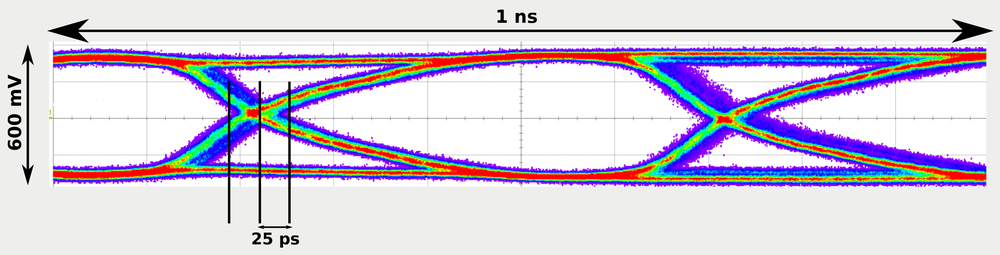
AM06 characterization and volume test

The AM06 chip has been characterized with the test system at a INFN laboratory in Milano. The test setup is made of an FPGA board with a Xilinx Virtex6 FPGA, and a dedicated mezzanine board with a zero-insertion-force socket for the device under test.
The test procedure is controlled remotely by a PC connected to the internet. A set of routines written in Python allow us to test the AM chip in different conditions. The test sequence has 100 % coverage against single bit errors in the AM core blocks, in the readout, and in the main functions used to configure and run the AM chip.



AM06 test setup

From the eye diagram of one of the AM06 serial links at 2 Gbit/s, we observe that the jitter is about 25 ps. A similar result has been obtained for all the chip serial links, thus confirming the good quality of the serial communication.



Eye diagram of AM06 serial link at 2 Gbit/s

7500 AM06 chips are being fabricated for the FTK system. Therefore, the test setup is finalized to test a large number of chips in a company. The test procedure is automated as much as possible and a graphic interface has been developed to simplify the use of the test system.
The test setup has been assembled successfully at Microtest srl in Altopascio, Italy, where the production lot of 7500 AM06 chips will undergo the test. The test time for each chip has been kept short enough, to limit test costs; moreover, the test procedure is very user-friendly and does not require a specialized training of the operator.

Conclusion

The AM06, the 6th version of a large Associative Memory chip for FTK system is designed in 65 nm CMOS technology. The FTK system includes 7500 AM chips, therefore, the test setup and the measurement software have been developed to define a standard test procedure suitable for the industrial test of a large number of chips.
The laboratory characterization shows full functionality of both the AM06 and the test system.
The setup has been implemented successfully at the company and the operator is capable to perform the test of a large number of AM06 chips without any interaction with the test setup developers.

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