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Characterization of HV-CMOS detectors in BCD8 technology and of a controlled hybridization technique

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Radiation detectors built in high-voltage and high-resistivity CMOS technology are an interesting option for the large area pixel-trackers sought for the upgrade of the Large Hadron Collider experiments. A possible architecture is a hybrid design, where CMOS sensors are readout by front-electronics coupled through a thin dielectric layer. A critical requirement is the radiation hardness of both the sensor and interconnection technology up to a dose of 0.1-1 Grad, depending on the distance from the interaction region.

In this paper we present the characterization of detctors built in BCD8 technology by STMicrolectronics. The BCD8 is a 160 nm process integrating bipolar, CMOS and DMOS devices and it is mostly used for automotive application. A version with 70 V voltage capability has been tested to evaluate its suitability for the realization of CMOS sensors with a depleted region of several tens of micrometer. Sensors featuring 50×250 μm2 pixels on a 125 Ωcm resistivity substrate have been characterized showing a uniform breakdown at 70 V before irradiation, as expected by design in this technology, and a capacitance of about 80 fF at 50 V reverse bias voltage.

The response to ionizing radiation is tested using radioactive sources and an X-ray tune, reading out the detector with an external spectroscopy chain. At the nominal 50 V bias, the device can detect soft X-rays, whose ionization yield is comparable to a minimum ionizing particle in the depletion region, demonstrating the detector is suitable also for charged particle detection and tracking application.

Irradiation tests were performed up to proton fluences exceeding 5×10¹⁵ p/cm2 and they show the depletion and breakdown voltages increases with irradiation

A hybridization process for capacitive coupling has been developed. It consists of gluing the CMOS sensor to the readout electronics using a dielectric epoxy, whose thickness is controlled by SU8 pillars deposited on the readout chip surface. Uniformity of better than 100 nm on the pillar surface has been obtained. Assemblies have been performed using the ATLAS FE-I4 readout ASIC and prototype CMOS sensors. Measurements show a planarity better than 1.5 μm peak-to-peak on the 5 mm length of the HV-CMOS chip. To evaluate more precisely the achievable uniformity dummy chips of FE-I4 sizes have been made on 6-inch wafers. The measurement of the 24 capacitors on each chip is expected to achieve a precise estimation of the real thickness uniformity. The goal is to achieve less then 10% variation on the glue thickness (˜0.5 μm).

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