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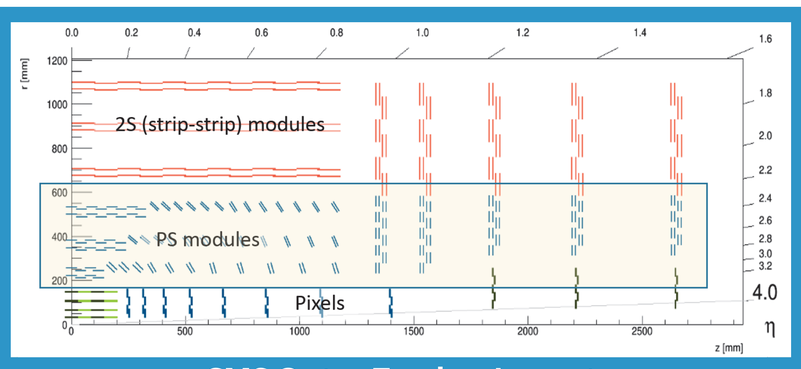
Readout architecture for the Pixel-Strip module of the CMS Outer Tracker Phase-2 upgrade

A. Caratelli, D. Ceresa, J. Kaplon, K. Kloukinas and S. Scarfì

CMS Outer Tracker

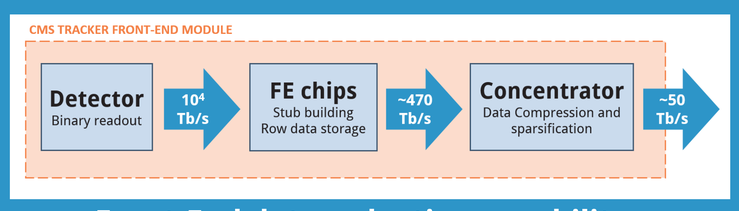


CMS Outer Tracker Layout

The Outer Tracker is required to **contribute information to the Level-1 trigger decision**[1]:

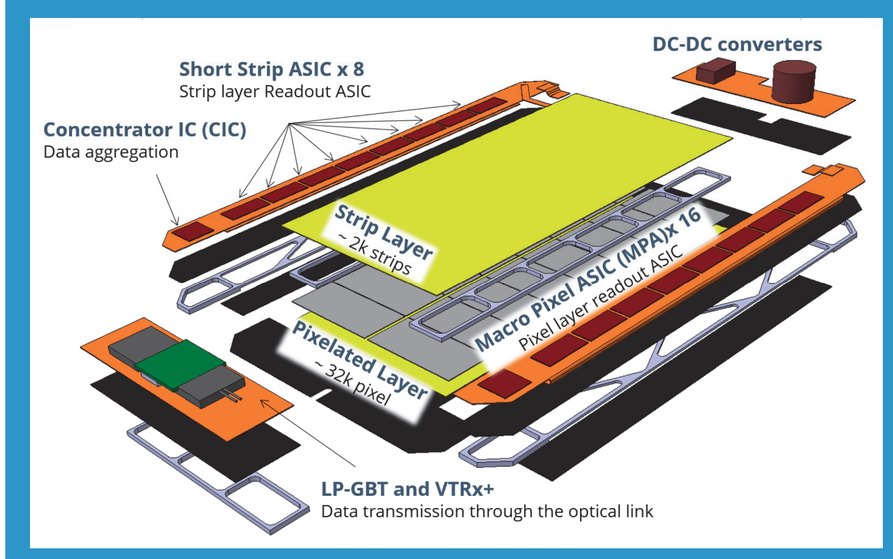
• The Front-End ASICs reject locally signals from low-pT particles, which are not interesting for the Level-1 reconstruction: **rejecting particles with pT below 2-3 GeV** reduces the bandwidth requirements by one order of magnitude or more.

• A second compression step is performed **by gathering the signal of every module over time and space** (CIC - Concentrator chip).

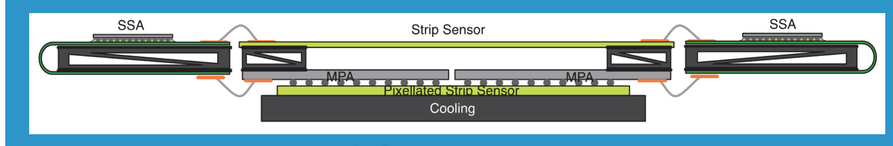


Front-End data reduction capability

Pixel – Strip (PS) module



Module exploded view

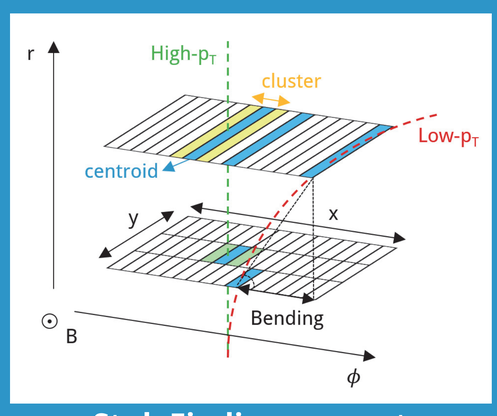


Module section view

The PS module is an assembly of one strip and one pixel sensors.

The correlation of the coordinates measured by the two sensors in the x-y plane facilitates the pT discrimination. This operation is called **Stub Finding**.

The segmentation of the pixel sensor along the z-direction contributes to the required z_0 resolution for the tracks reconstruction.



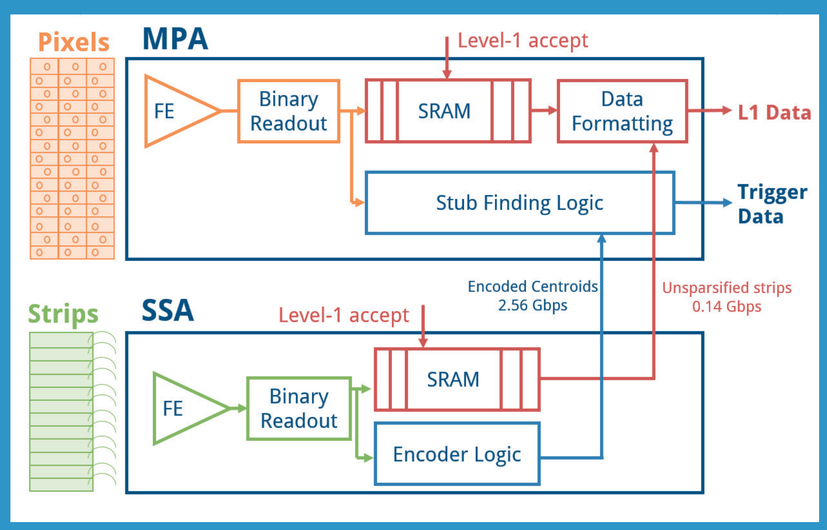
Stub Finding concept

Readout Architecture

PS module readout ASICs:
• SSA: the **Short Strip ASIC**, for the strip layer;
• MPA: the **Macro Pixel ASIC**, for the pixel layer;
• CIC: the **Concentrator IC** for data aggregation.

Signal processing at the FE electronics presents certain design challenges:
• High data volume **~ 10^4 Tb/s** (with Binary readout);
• Limited power budget **< 100 mw/cm².**

Low power features:
• **65 nm CMOS technology**;
• **Multiple Supply Voltage design (MSV)**;
• Memory Gating Logic;
• Clock Gating ;
• Low current sLVS driver/receiver[3] @ 320 Mbps.



Readout Architecture diagram

The module transmits to the CMS Tracker backend:

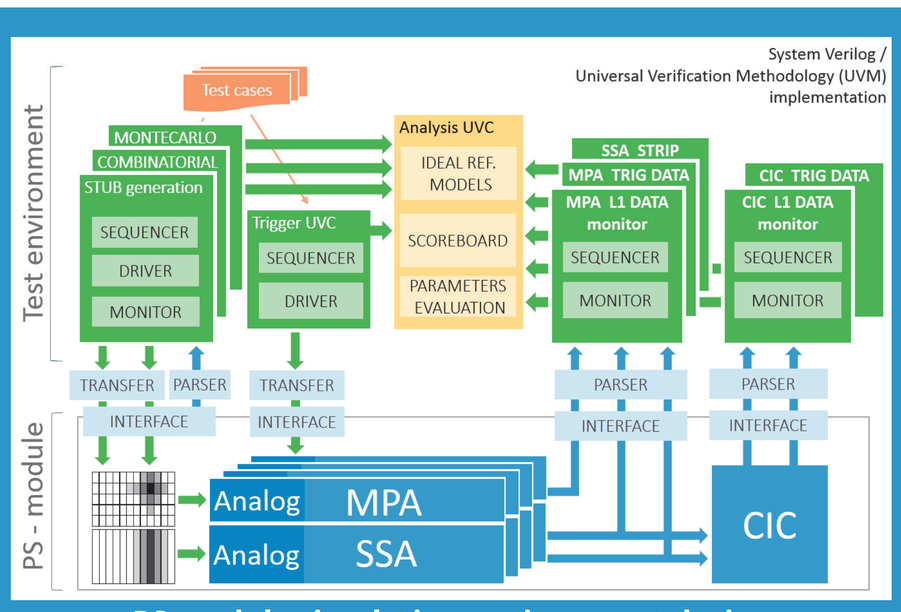
• **Trigger Data:** MPA generates primitives for L1 trigger by combining strips and pixel hits trough the Stub Finding.

Strips are provided by the SSA as encoded coordinate of cluster centre (centroid) at each Bunch Crossing (BX frequency = 40 MHz).

Particle curvature (bending) is calculated in the MPA as the difference between Pixel and Strip centroid. **Only high-pT particles (small bending) are sent in output.**

• **L1 Data:** Full events are stored locally in **radiation tolerant SRAM** memories[4] and provided to the back-end only if requested by a L1 trigger (L1 rate = 750 KHz).

System level simulation model



PS module simulation environment design

The PS module test-bench is a flexible verification environment based on **System Verilog** and **UVM** which allow to:

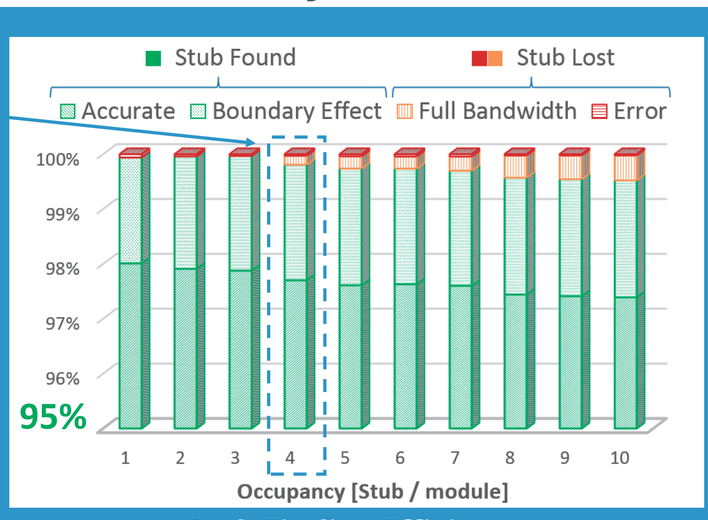
• generate large data sets of pixel hits and triggers with given constrained random distributions within the simulation environment;

• import simulation data from external **full detector/experiment Monte Carlo simulations** and detailed sensor simulations;

• run directed tests for debugging specific functions or problems and verifying exception handling procedures.

Efficiency results

Max. Occupancy in Tracker[5]



Stub Finding Efficiency

As shown in the plot above, MPA/SSA RTL implementation is fully verified and its **efficiency is > 99%** respect the ideal model.
The simulation environment evaluates also:

• **Boundary effect** counts the non accurate (+/- 50 um) position or bending of the stubs due to the dead area among MPAs;

• **Full Bandwidth** shows the percentage of stubs lost because of the limited bandwidth of MPAs and the CIC;

• **Error** shows the percentage of stubs lost because of artefacts introduced by the stub finding logic (**< 0.03 %**).

[1] Technical Proposal for the Phase-II Upgrade of the CMS Detector, *CMS Collaboration*.
[2] Macro Pixel ASIC (MPA): the readout ASIC for the pixel-strip (PS) module of the CMS outer tracker at HL-LHC, *D. Ceresa et Al,* JINST, Vol. 9, Nov. '14.
[3] Design of low-power, low-voltage, differential I/O links for High Energy Physics applications, *G. Traversi et Al,* JINST Vol. 10, Jan. '15.
[4] The development of a radiation tolerant low power SRAM compiler in 65nm technology , *R. Brouns, IMEC*, AMICSA 2014.
[5] Data transmission efficiency of the phase II tracker front-end system using new GBT transmission scheme, *S. Viret*, CMS Internal Note.