RD53 status and plans

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On behalf of the RD53 Collaboration

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25-30 September 2016 - La Biodola, Isola d'Elba, Italy

Outline

- RD53 – Challenges & Goals
- The RD53A demonstrator
- CHIPIX65 and FE65P2 demonstrators
- Analog Very Front Ends
- Characterization of small demonstrators and test structures

RD53 – An overview

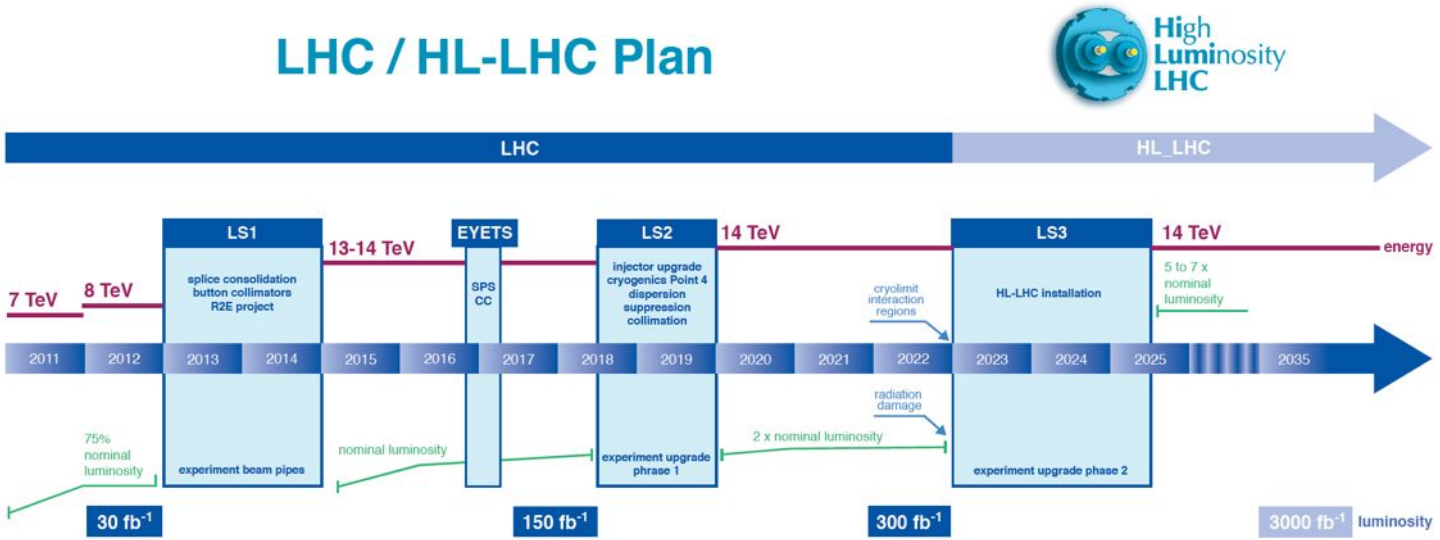
- Focused R&D program aiming at the **development of pixel chips** for ATLAS/CMS **phase 2 upgrades**
- 19 institutions from Europe and US
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, RAL, Seville, Torino, UC Santa Cruz.

- **65 nm CMOS** is the common technology platform
- RD53 Goals:
  - Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
  - Development of **tools and methodology** to efficiently design large complex mixed signal chips
  - Design of a **shared rad-hard IPs library**
  - Design and characterization of common engineering run with **full sized pixel array chip**

Pixel Detector Requirements at HL LHC

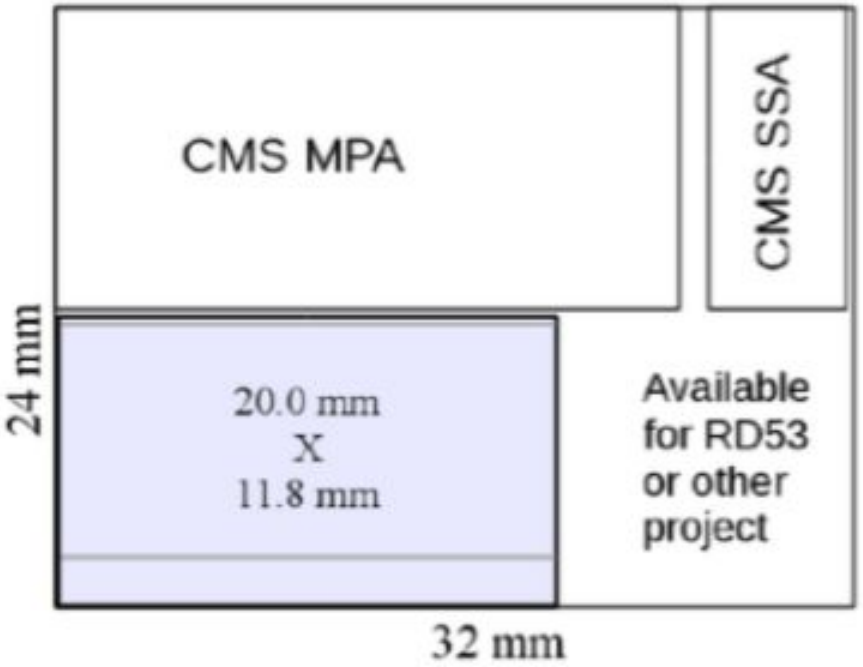
Very **challenging requirements** for the innermost layers of the pixel detectors in ATLAS and CMS

- Very **high particle rate** → pixel hit rates up to 3 GHz/cm^2
- **Small pixels**: 50x50um^2 → increased resolution, improved track separation
- **Large chips**: ~2cm x 2cm (1 billion transistors)
- Increased **trigger rate**: 1 MHz with 12.8us trigger latency
- **Low mass, low power systems** < 0.5W/cm^2
- **Low threshold**: 600-1000 e- → severe requirements on noise and dispersion
- **Harsh radiation environment**: 1 Grad(SiO_2) TID; 10^{16} eq. n/cm^2 fluence



RD53A - Full Scale prototype

- **400 x 192 pixel, 50um x 50um pixel, 20mm x11.8mm chip**
- **Goal: demonstrate in a large format IC**
  - suitability of **65nm technology** (including radiation tolerance)
  - **high hit rate**: 3 GHz/cm^2
  - **trigger rate**: 1 MHz
  - **Low threshold operation** with chosen **isolation** strategy and **power distribution**
- **Not intended to be a production chip**
  - will contain design variations for testing purposes (with **different versions of the analog very front-end)**
  - wafer scale production will enable prototyping of bump bonding assembly with realistic sensors in new technology



- To be completed: December 2016
- To be submitted: End of March 2017

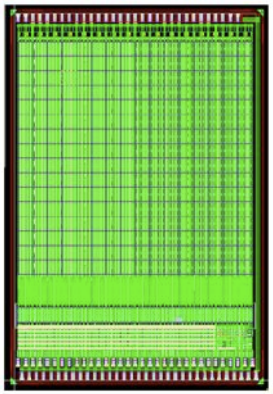
Specs document:

http://cds.cern.ch/record/2113263

65 nm CMOS prototypes

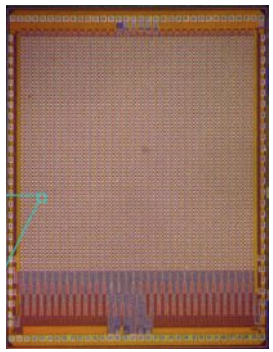
Small demonstrators and test structure chips have been submitted:

- **INFN** (Pavia, Torino) submitted (May 2015) small prototypes with two different versions (asynchronous, synchronous) of the analog front -end. Encouraging results from test

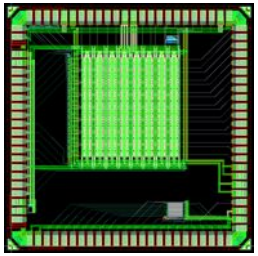


- These two different analog front-end are included in the **CHIPIX65** demonstrator (July 2016)

- Another design for the analog front-end (asynchronous) is included in the **FE65-P2** demonstrator, designed by **LBNL**, that is currently being tested, with promising results



- **Fermilab/INFN** submitted (May 2016) a 16x16 matrix including analog front-end with zero dead time and Flash ADC; characterization will start in the next weeks



FE65-P2 and CHIPIX65 Demonstrators

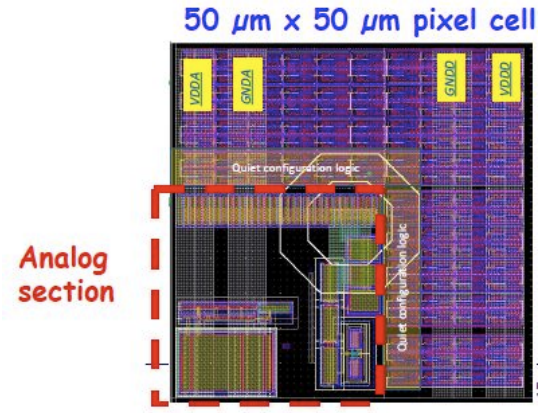
FE65-P2

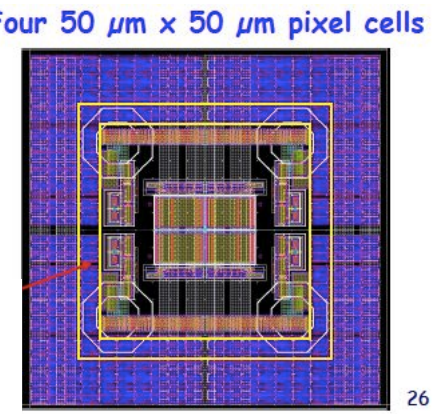
- 64x64 matrix, 50um x50 um bump pattern
- Dimensions: 3.5mm x 4.2mm
- Single Analog VFE architecture with 8 different subversion
- 4-bit ToT signal digitization
- In-time threshold< 1000 e- while consuming <4uA/pixel
- Noise ~35- @ 100fF input capacitance
- 2x2 Analog Islands

CHIPIX65

- 64x64 matrix, 50x50 μm^2 pixel
- Dimensions: 3.5mm x 5.1mm
- Multiple Analog VFE
- 5-bit ToT signal digitization
- In-time threshold< 1200 e-
- Noise ~100e- @ 50fF input capacitance
- 2x2 Analog Islands on 4x4 pixel region digital architecture
- Includes RD53 IPs (DAC, ADC, SER, sLVS-TX /RX, Bandgap, CERN I/O Pads)

The "analog island" concept





Towards the RD53A full scale chip

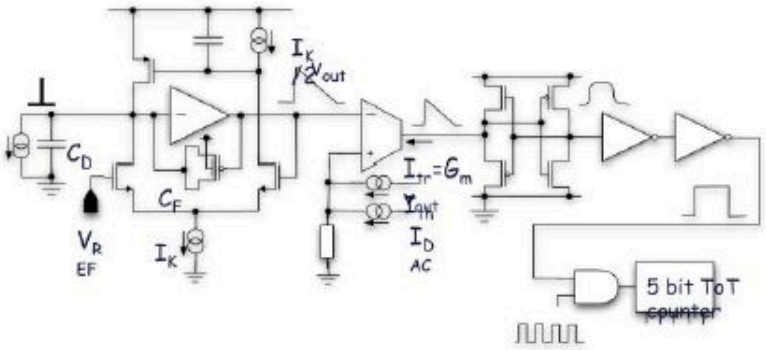
- CHIPIX65 and FE65P2 are a full exercise of chip integration and constitute a trial version before moving to the full size prototype

	Pixel Matrix	Analog VFE	Analog / Digital Isolation	IP-Block	Pixel Region & Arch	Bias-Distrib	Powering	Digital CORE
FE65P2	64x64 pixels	AFE_LBNL	Analog in deep n-well Digital in deep n-well PAD in deep n-weel	few and not RD53A	(2x2) Distributed Latency Buffer	Single stage mirroring	standard	(4x64)
CHIPIX65 demonstrator	64x64 pixels	AFE_TO AFE_PV	Analog in deep n-well	**RD53A IP-blocks**: DAC, ADC, SER, sLVS-TX, sLVS-RX, Bandgap, CERN I/O Pads	(4x4) central Latency Buffer	Double stage mirroring	standard	(4x4)
RD53A	400x192 pixels	AFE_LBNL AFE_TO AFE_PV AFE_FNAL -- tbc : review	Analog in deep n-well Digital in deep n-well PAD in substrate tbc	**RD53A IP-blocks**: DAC, ADC, SER, sLVS-TX, sLVS-RX, Bandgap, CERN I/O Pads, PLL , ShuntLDO, T-sens, Rad-sens	tbd	Double stage mirroring	standard / Serial-Poweering	(8x8) / (4x16)

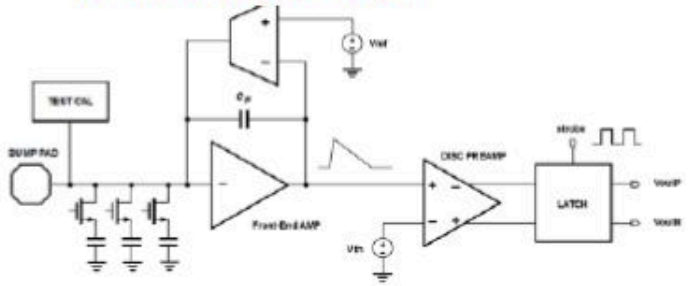
L. Demaria et al, "Recent Progress of RD53 Collaboration towards the Next Generation of Pixel Readout Chips for HL-LHC", presented @ PIXEL 2016, 5-9 September, Sestri Levante

Analog front-ends

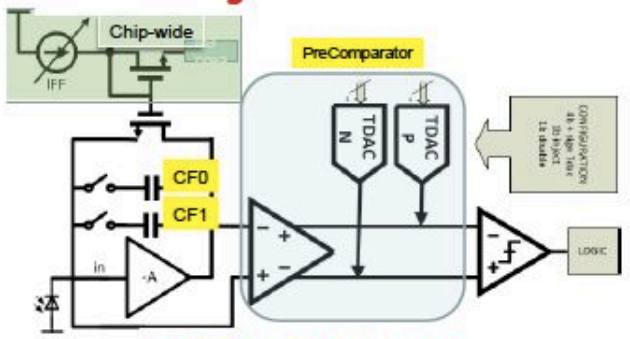
INFN Pavia/Bergamo design



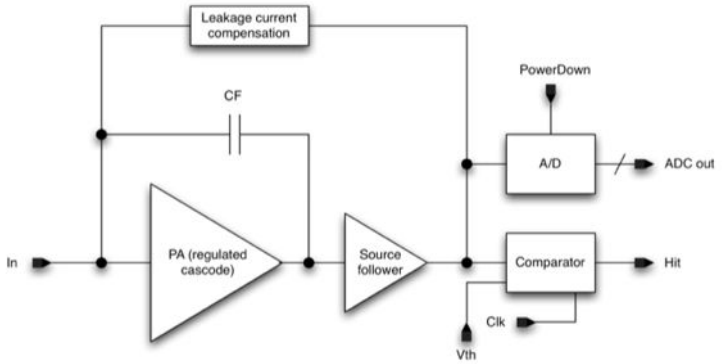
INFN Torino design



LBNL design in FE65-P2

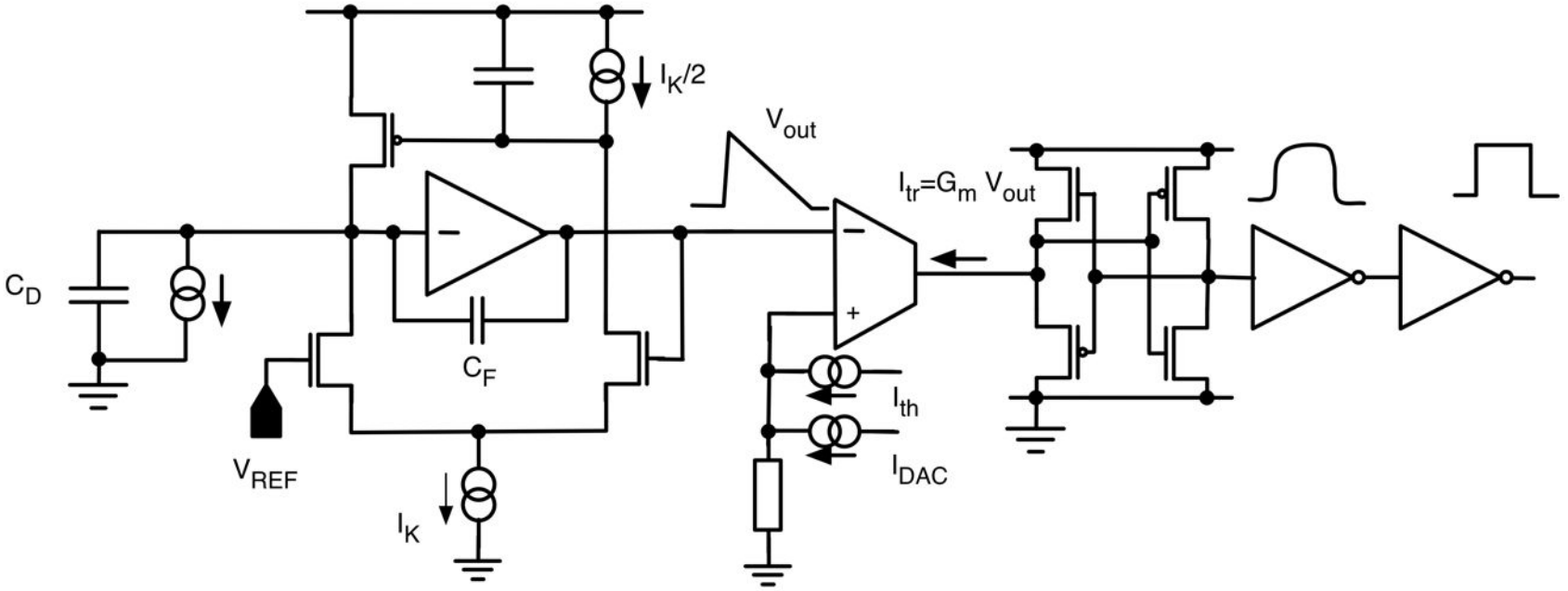


INFN-FNAL design



- **4 different version** are being developed for the integration in the full scale prototype
- They have to be **fully tested** (also after irradiation) in their (almost) final version (schematic and layout) so that they qualify to be safely included in RD53A

Bergamo/Pavia Analog Front-end

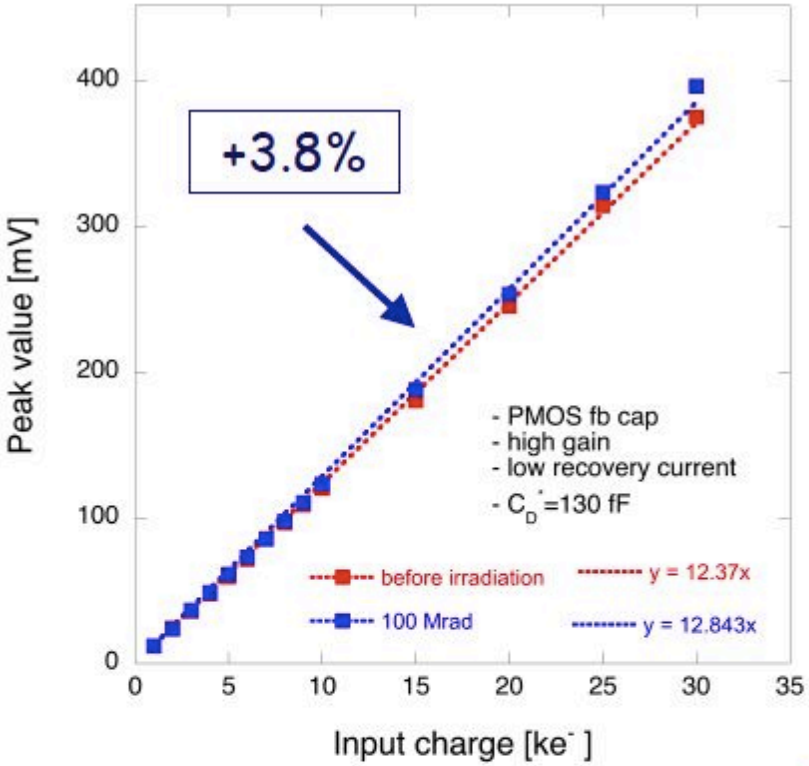


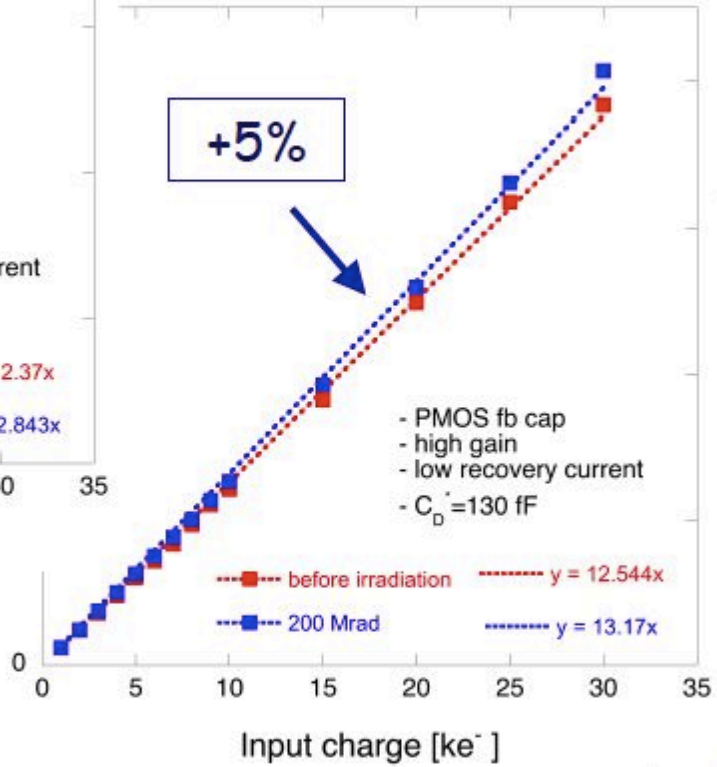
- **Single amplification stage** for minimum power dissipation
- **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- High speed, low power **current comparator**
- **4 bit local DAC for threshold tuning**
- **In-pixel calibration circuit**

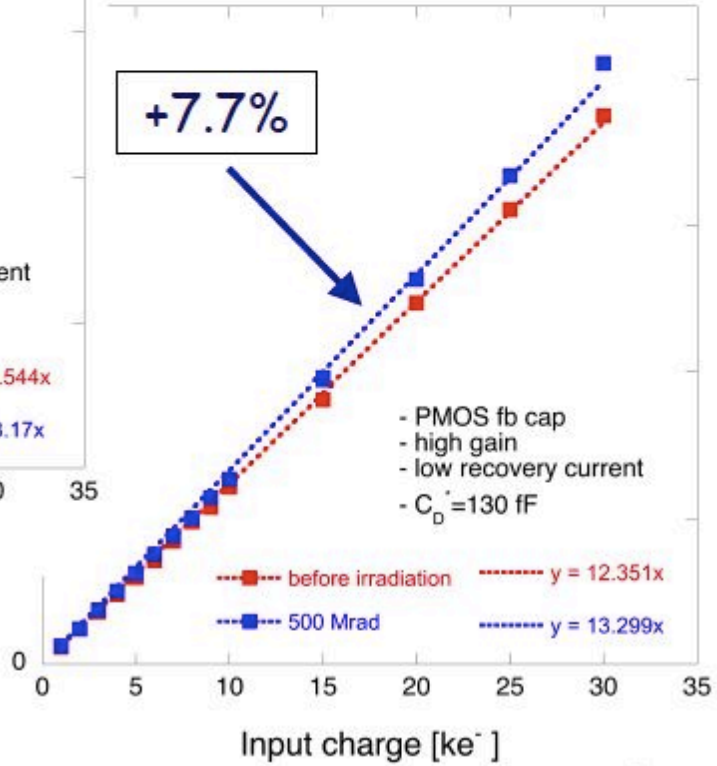
- **30000 electron** maximum input charge, ~450 mV preampli output dynamic range
- Selectable gain and recovery current
- Overall **current consumption**: ~4 uA

Radiation effects on charge sensitivity

- Chip irradiated up to 800 Mrad TID
- Two separate irradiation campaigns (samples irradiated with and w/o biased applied)

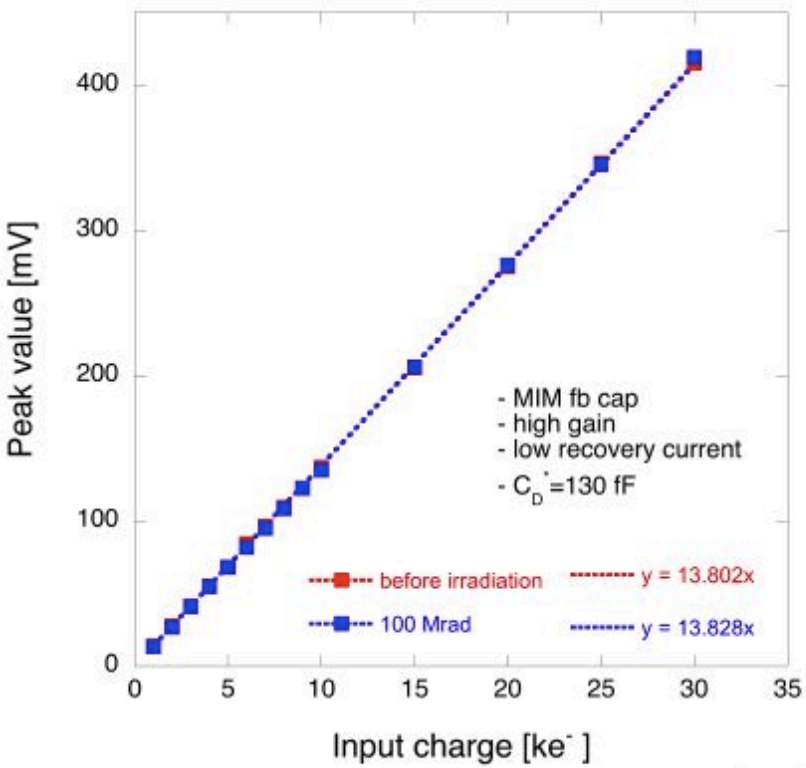




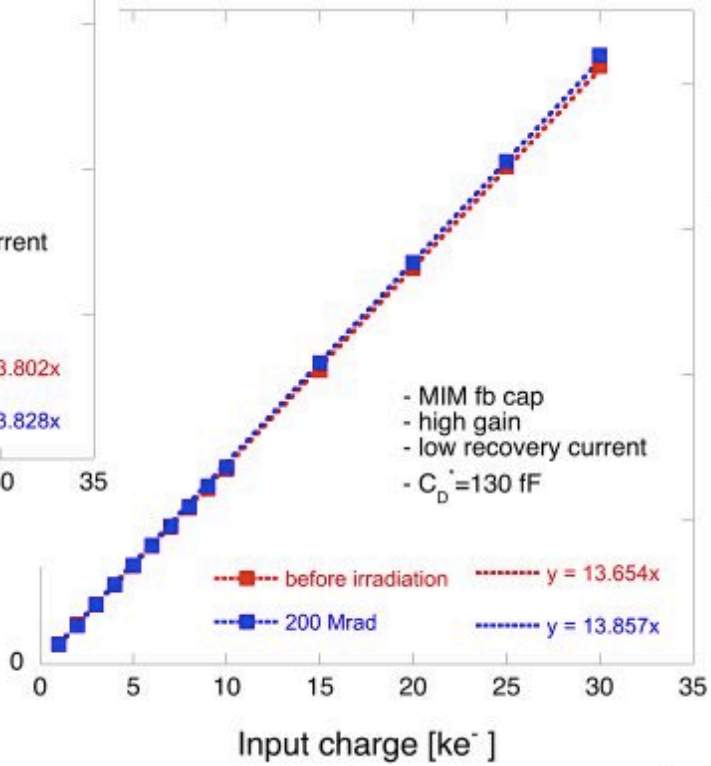


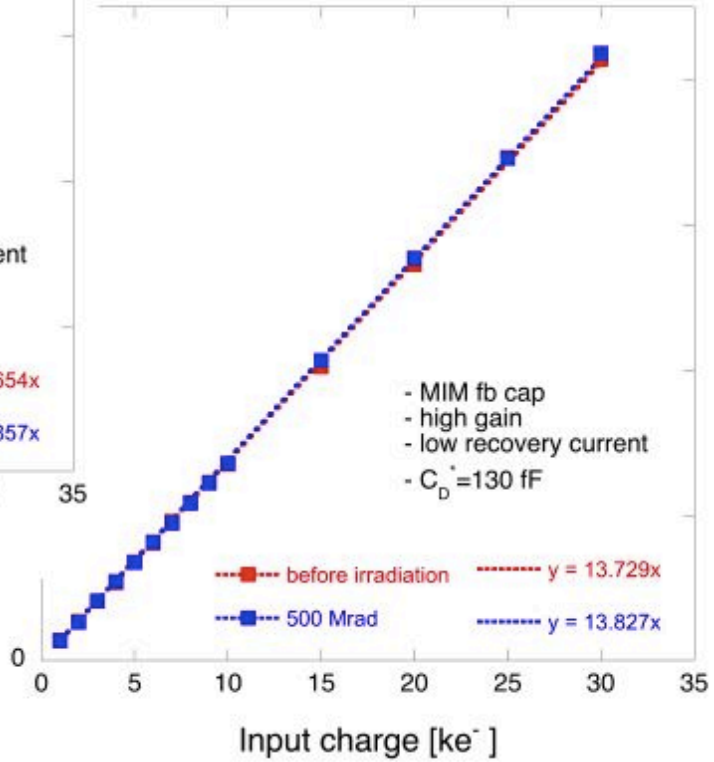
- Slight increase of the **charge sensitivity** with the dose
- Effect independent of bias condition (DUT biased or unbiased) during irradiation

Charge sensitivity: MIM feedback cap

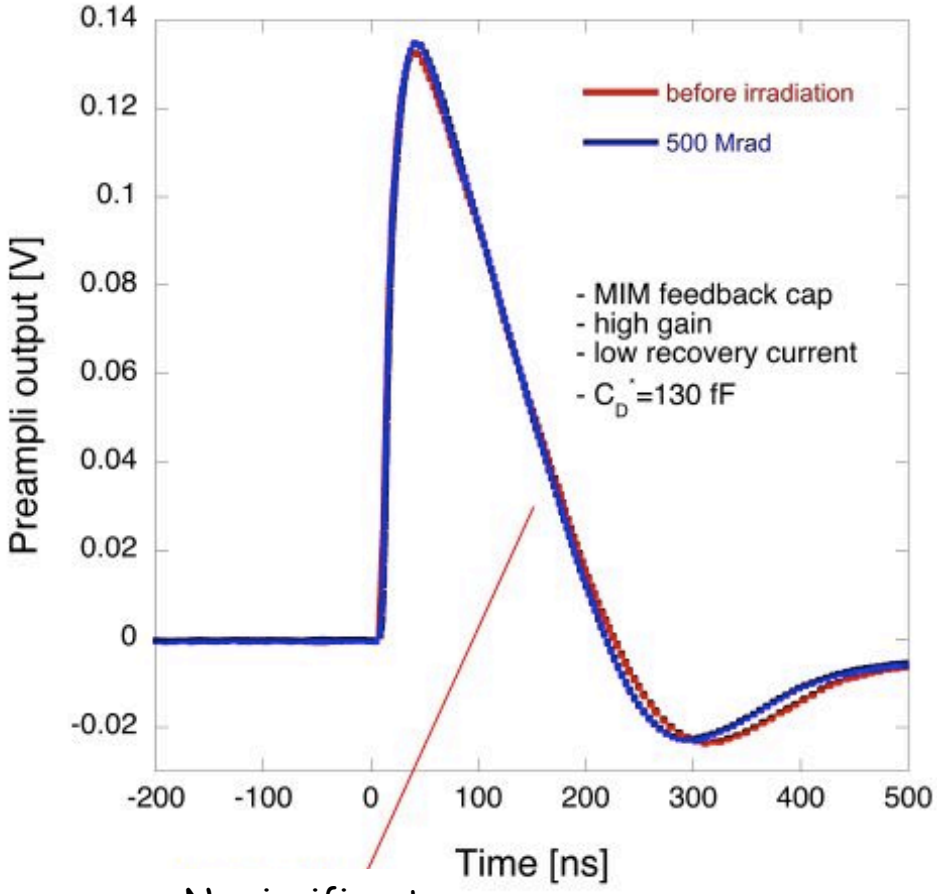


- No effect observed in the case of the CSA with MIM feedback cap

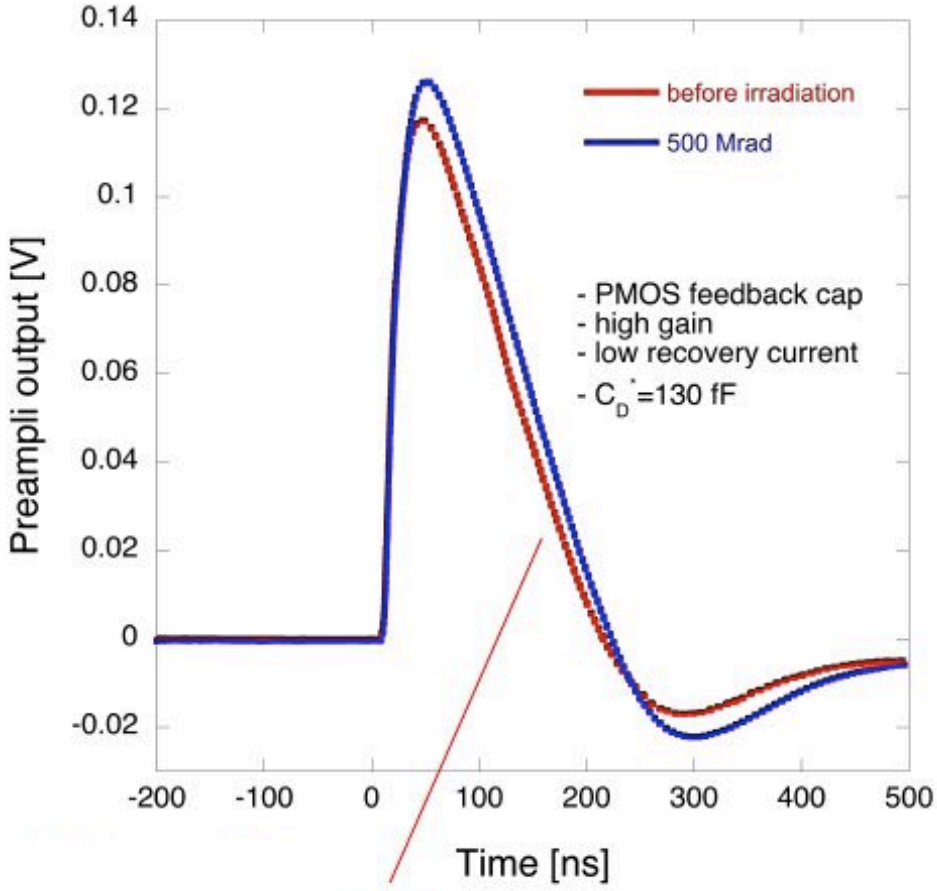




CSA response @500 Mrad



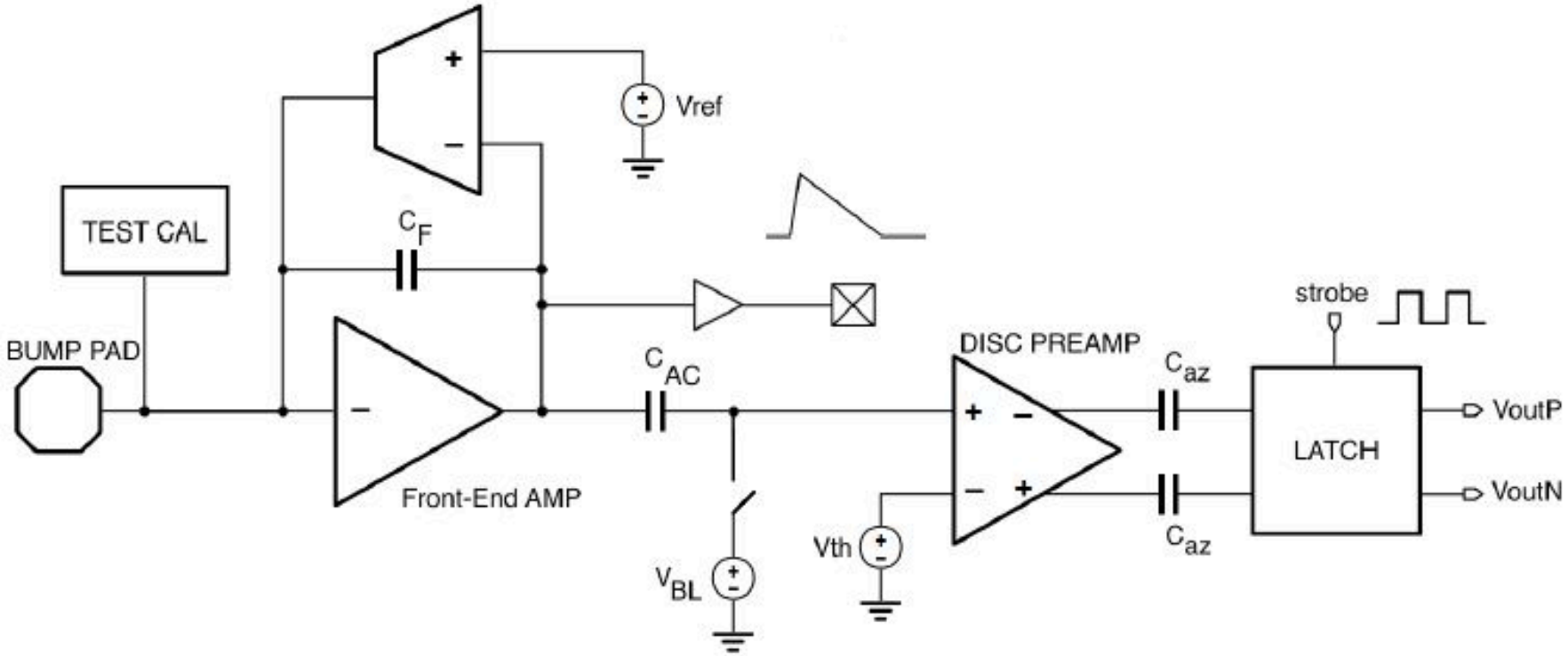
No significant differences @ 500 Mrad



slope difference fully consistent with the observed change in charge sensitivity (and the relevant change in CF)

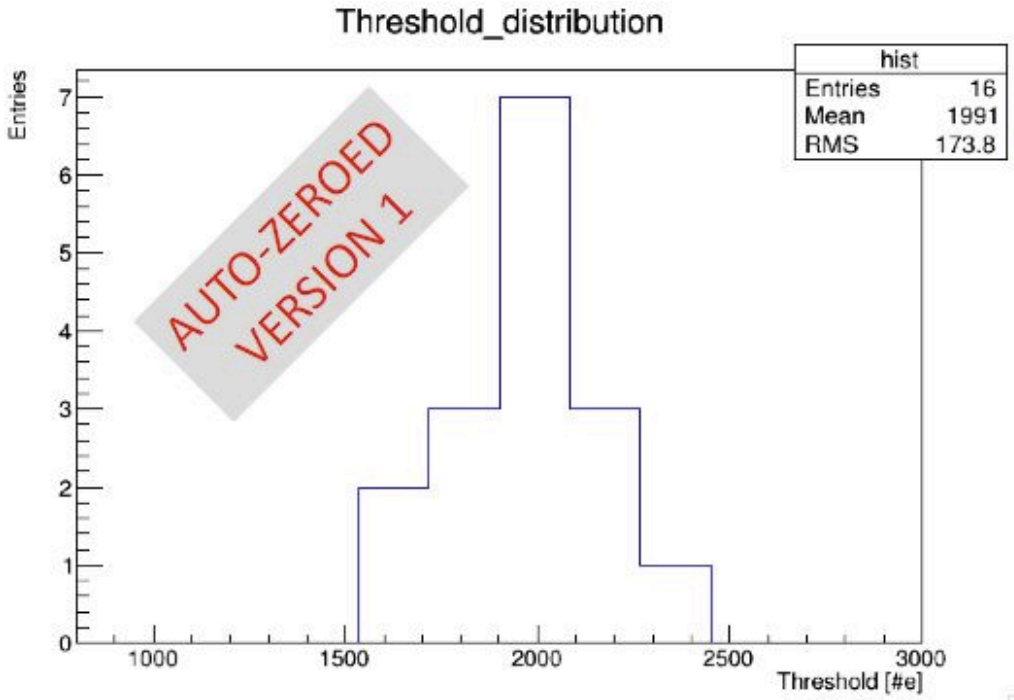
L. Ratti et al, "Charge preamplifier in a 65 nm CMOS technology for pixel readout in the Grad TID regime", presented @ RADECS 2016, 19-23 September, Bremen

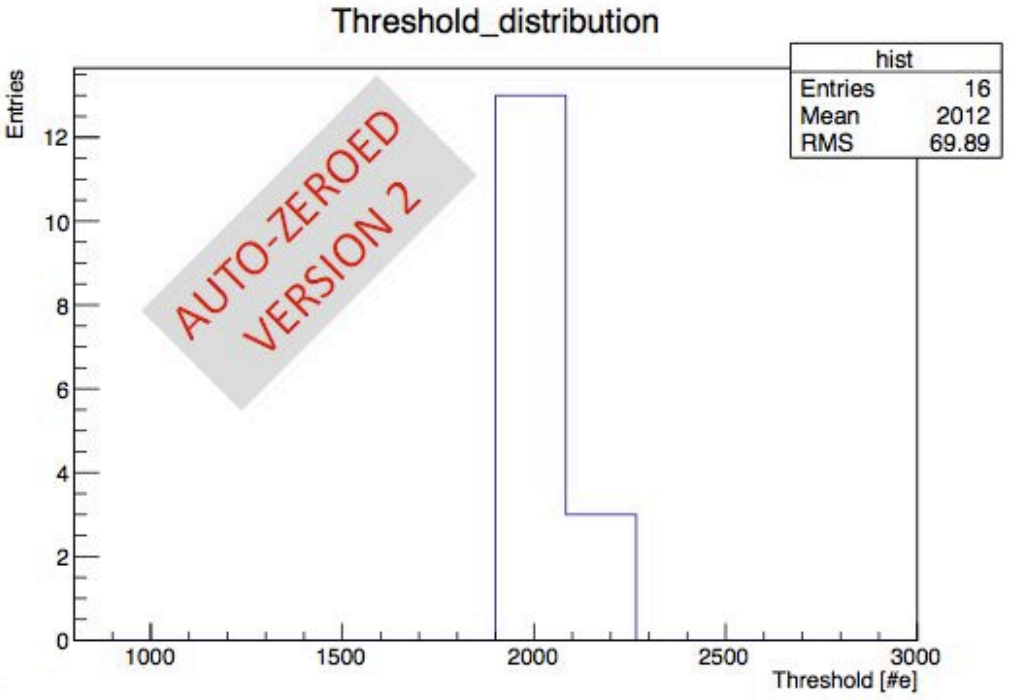
Torino Analog Front-end



- **One stage CSA** with **Krummenacher** feedback
- **Synchronous discriminator**, AC coupled to CSA, including offset compensated differential amplifier and latch → **no threshold trimming needed**
- **Fast Time-over-Threshold**
- **Local oscillator** strobing Latch (to 800MHz)
- **In-pixel calibration circuit**

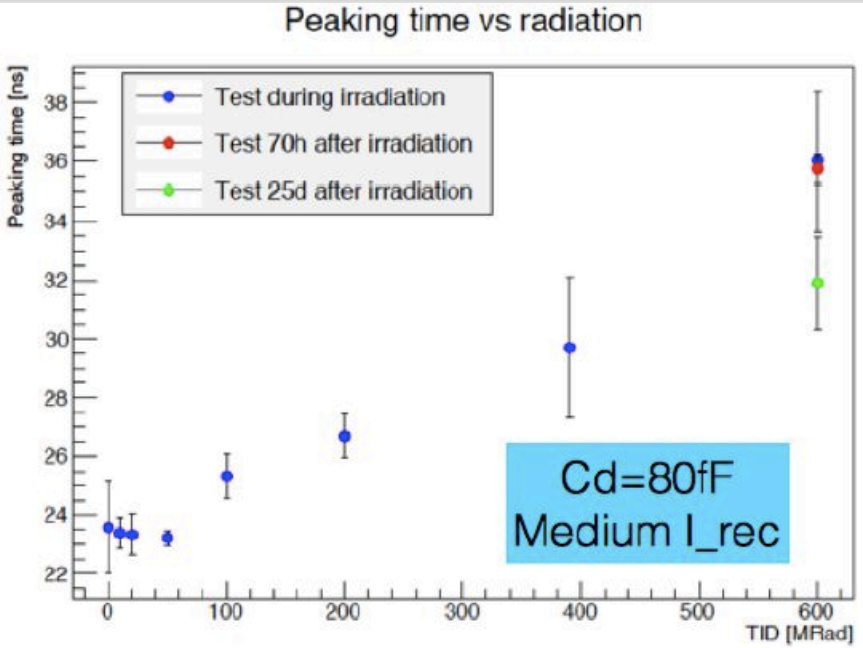
Threshold dispersion

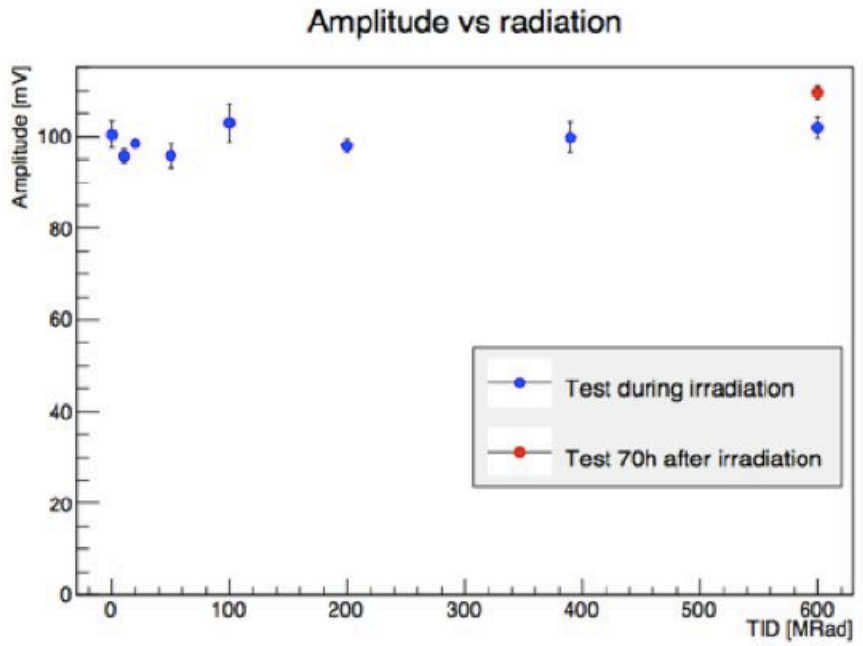




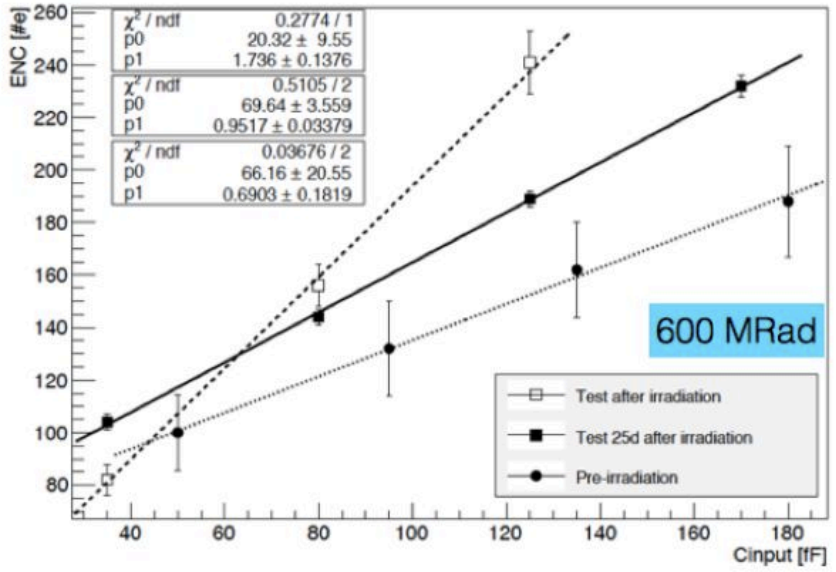
- **Threshold dispersion**: 70 e rms in the improved FE (version 2)
- In agreement with the reduction of the latch dynamic offset implemented in the version 2 prototype

Radiation effects on analog parameters



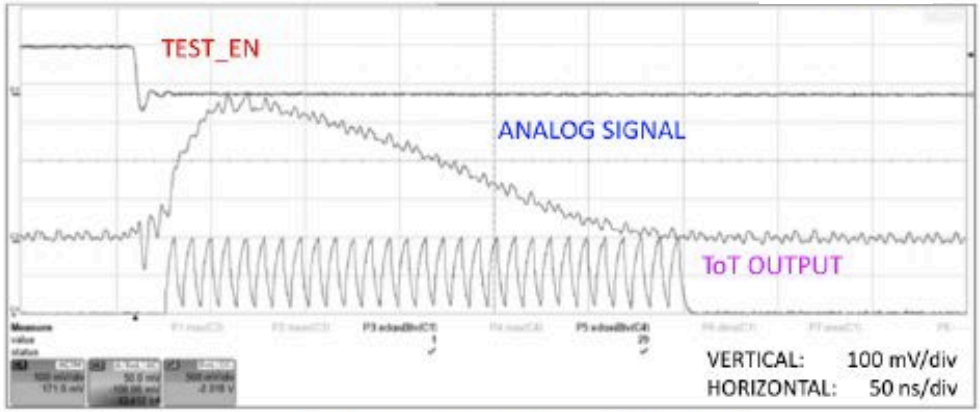


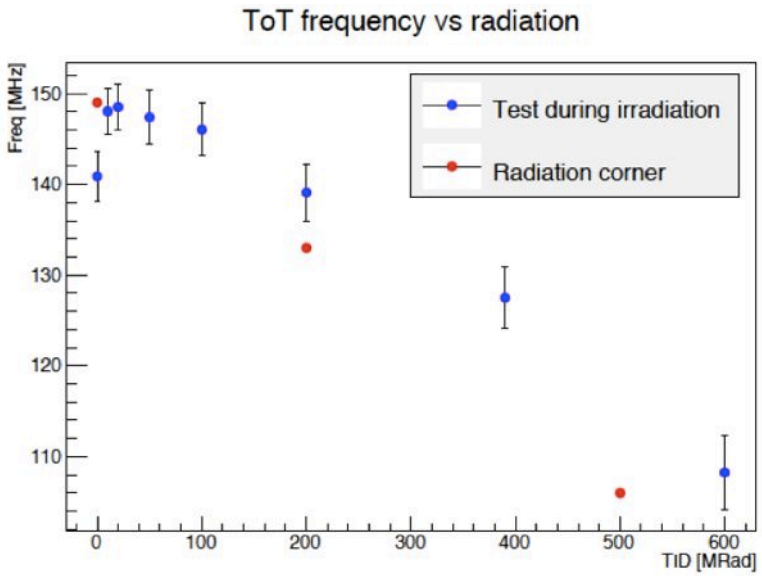
- Chip irradiated up to 600 Mrad (powered, biased, clocked, readout active as during HL_LHC) @ CERN X-ray machine
- Peak time for C_D=80 fF: **increase with TID** then partial recovery
- Preamplifier **peak amplitude**: no relevant variation seen
- For C_D = 50 fF increase of 10% (measured in low-gain configuration)

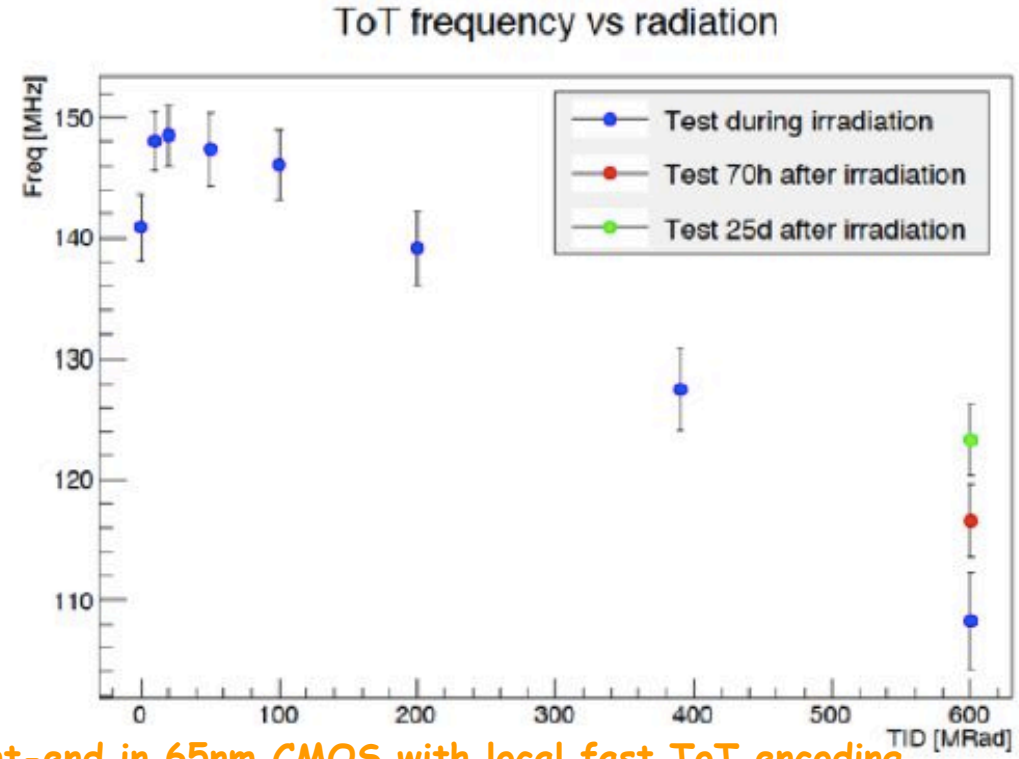


ToT frequency

- Local oscillator set to 140 MHz
- Slow down with TID
- Partial recovery with time (annealing)
- Trend of the ToT freq is reproduced with a reasonable (10-15%) discrepancy

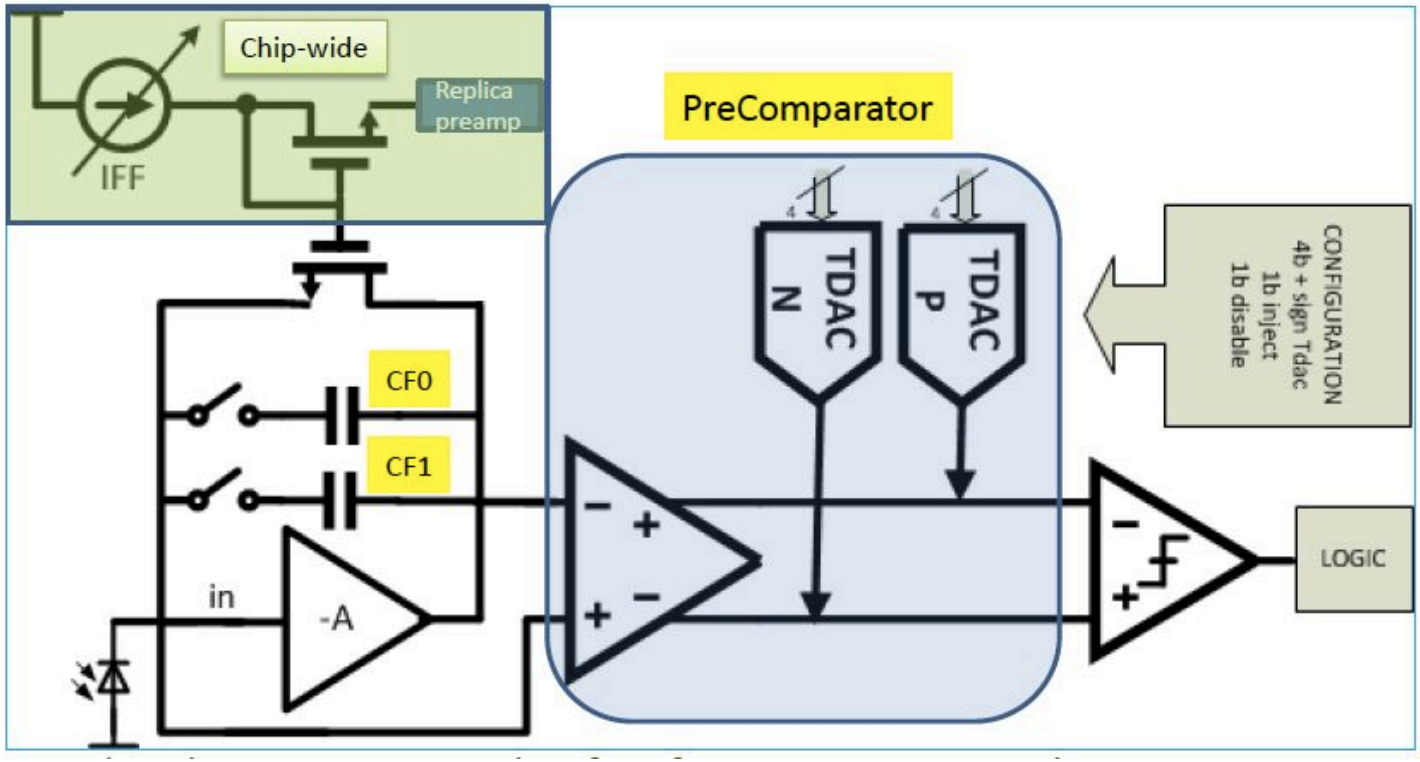






E. Monteil et al, "A synchronous analog very front-end in 65nm CMOS with local fast ToT encoding for pixel detectors at HL-LHC", presented @ TWEPP 2016, 26-30 September, Karlsruhe

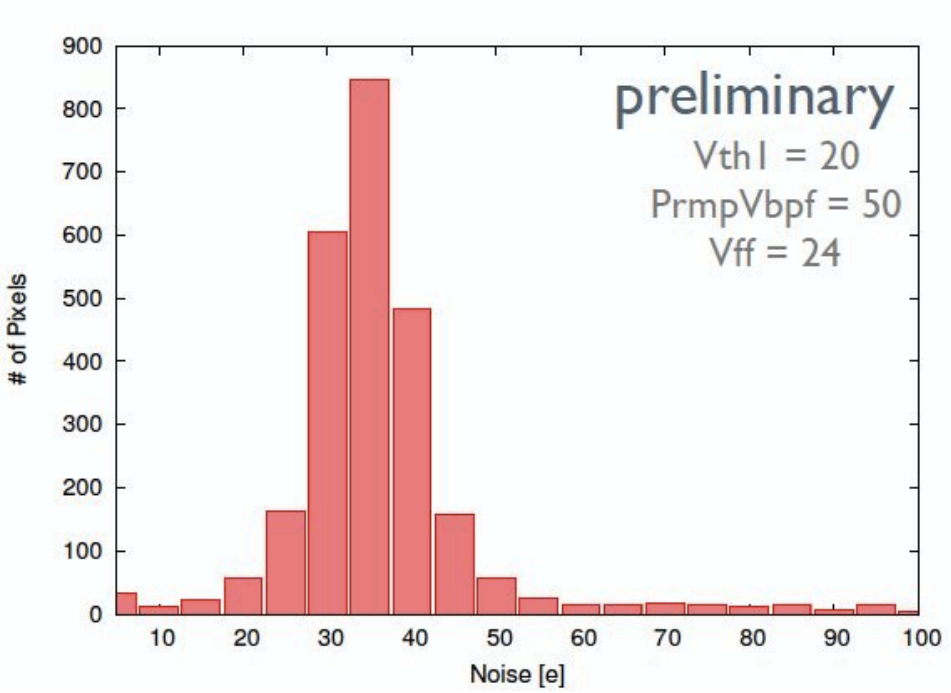
LBNL Front-end

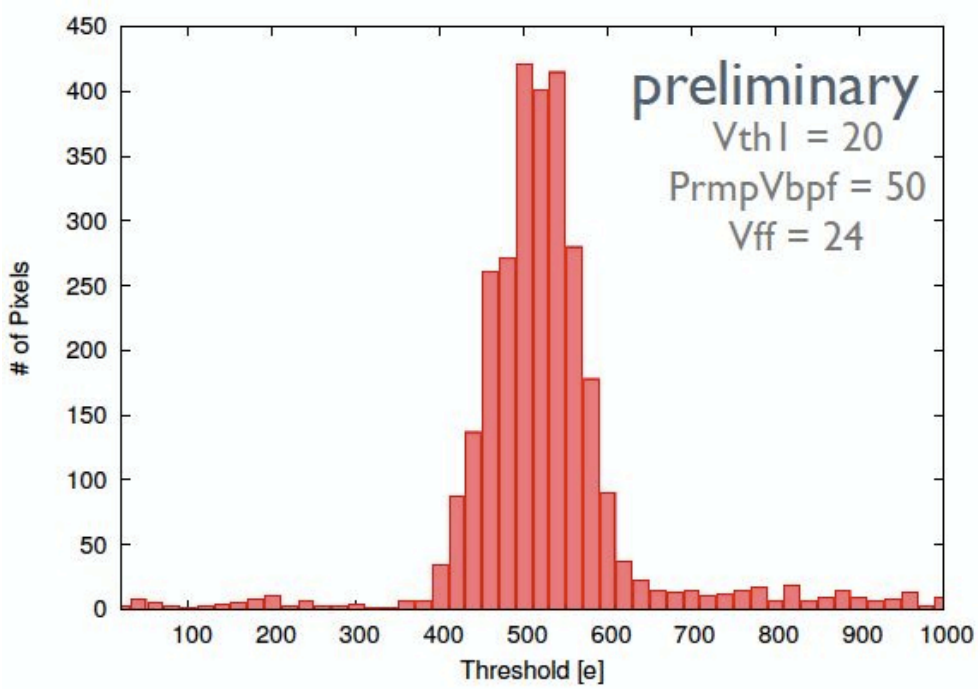


- **Continuous reset integrator** first stage with **DC-coupled pre-comparator stage**
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation** (not shown) a la FEI4
- **Threshold adjusting** with global 8bit DAC and two per pixel 4bit DACs

Noise and threshold

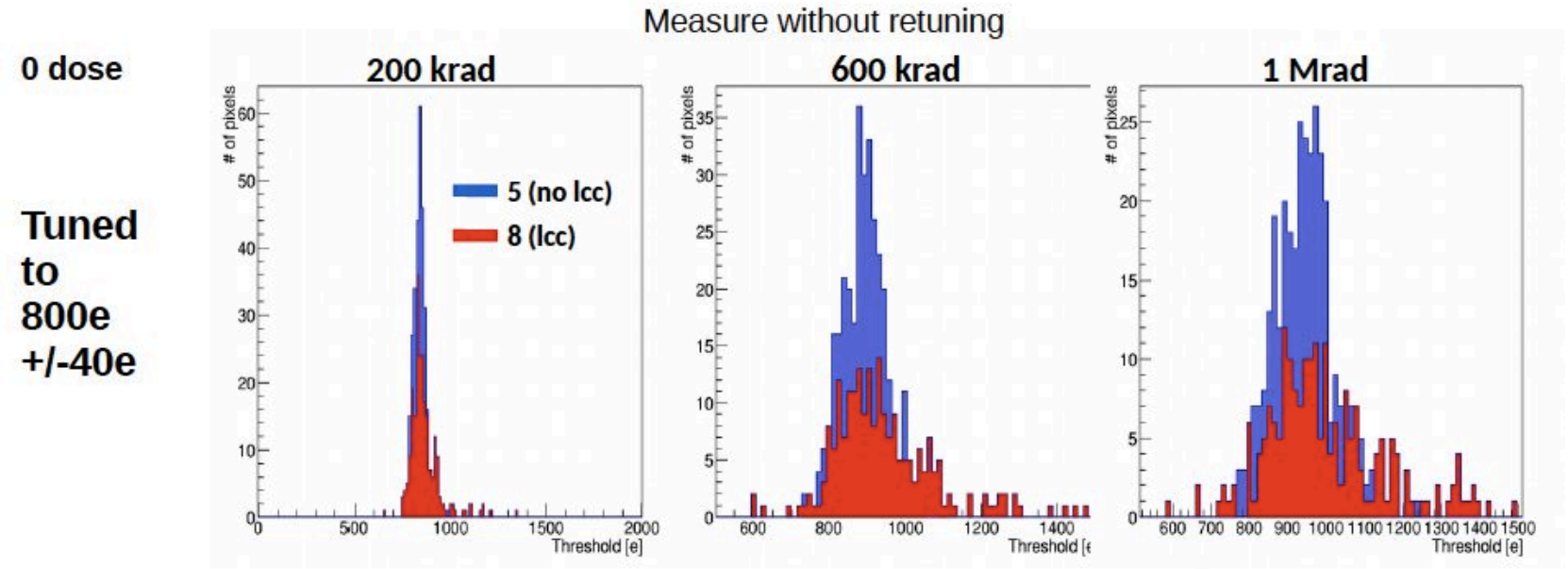
FE65-P2 Early results with bare chip





- Very good performance in terms of **noise** and **threshold dispersion**:
  - ENC ≈ 35e rms @ C_D=50fF
  - Threshold dispersion after tuning ≈ 40 e rms

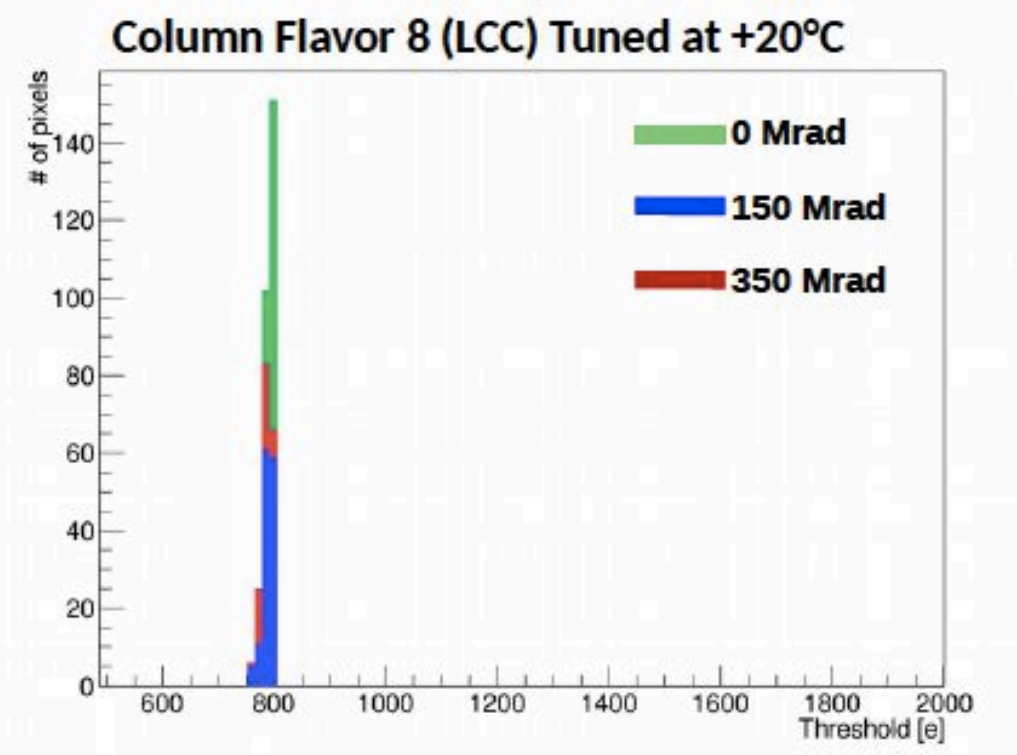
Threshold Evolution with Radiation

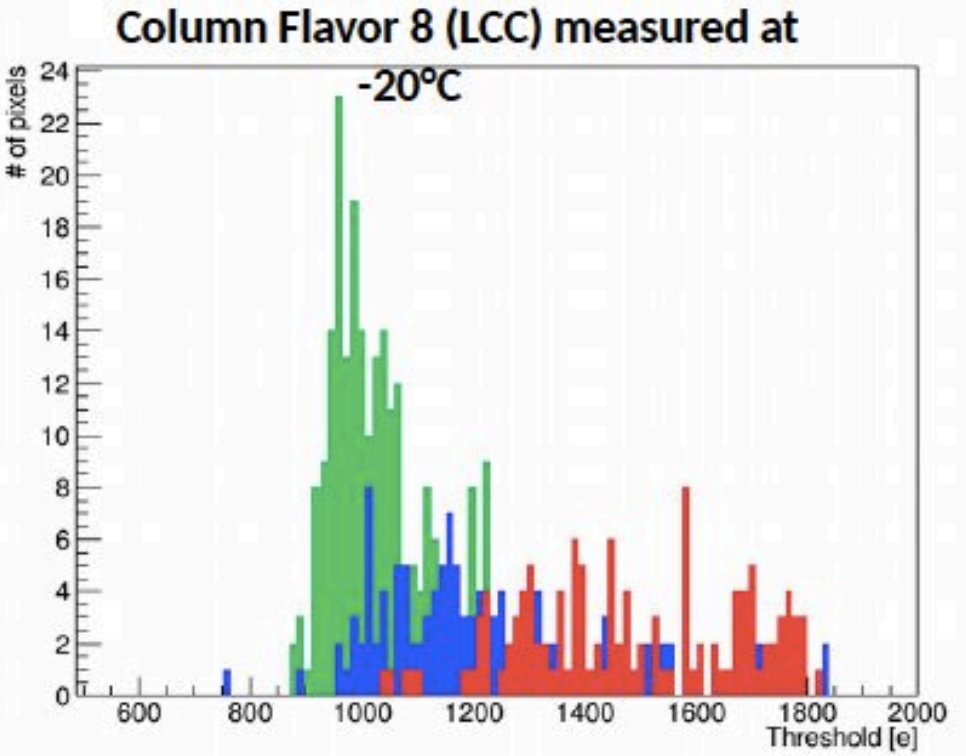


Example of Column 5 (without Leakage Current Compensation circuit) and Column 8 (with Leakage Current Compensation circuit)

- Chip irradiated up to **350 Mrad TID**
- **Threshold shift**
  - 15.2 e/Mrad for the column without leakage current compensation circuit
  - 22.2 e/Mrad for the column with leakage current compensation circuit
- **Threshold dispersion:**
  - 7.0 e/Mrad for the column without leakage current compensation circuit
  - 20.9 e/Mrad for the column with leakage current compensation circuit

Threshold Evolution with Temperature

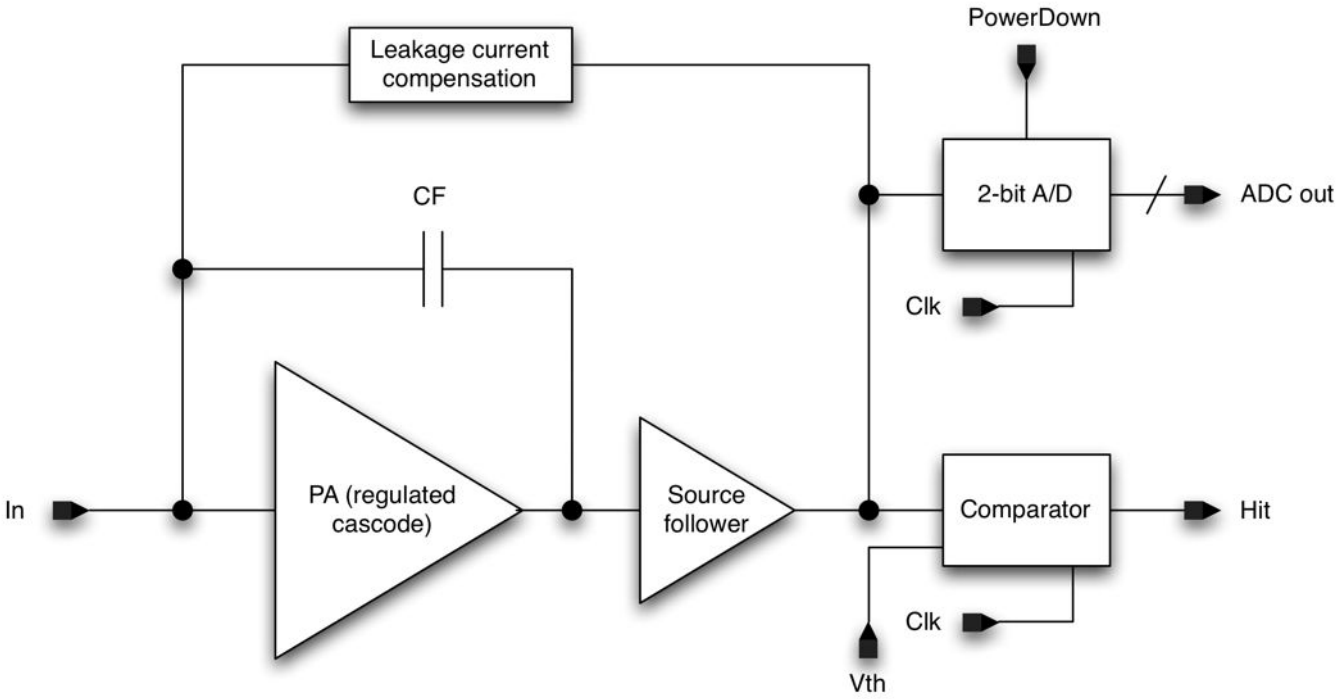


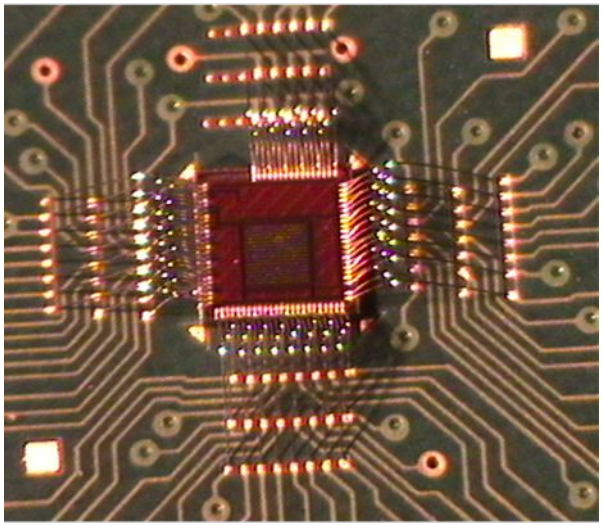


- **Threshold shift (@ 350Mrad):**
  - 17.1 e/°C for the column without leakage current compensation circuit
  - 16.7 e/°C for the column with leakage current compensation circuit
- **Threshold dispersion (@ 350Mrad):**
  - 5.86 e/°C for the column without leakage current compensation circuit
  - 6.66 e/°C for the column with leakage current compensation circuit

M. Garcia-Sciveres, "High Luminosity LHC Pixel Readout Test Chip and RD53A Prototype Plans", presented @ ICHEP 2016, 3-10 August, Chicago

Fermilab/INFN analog front-end

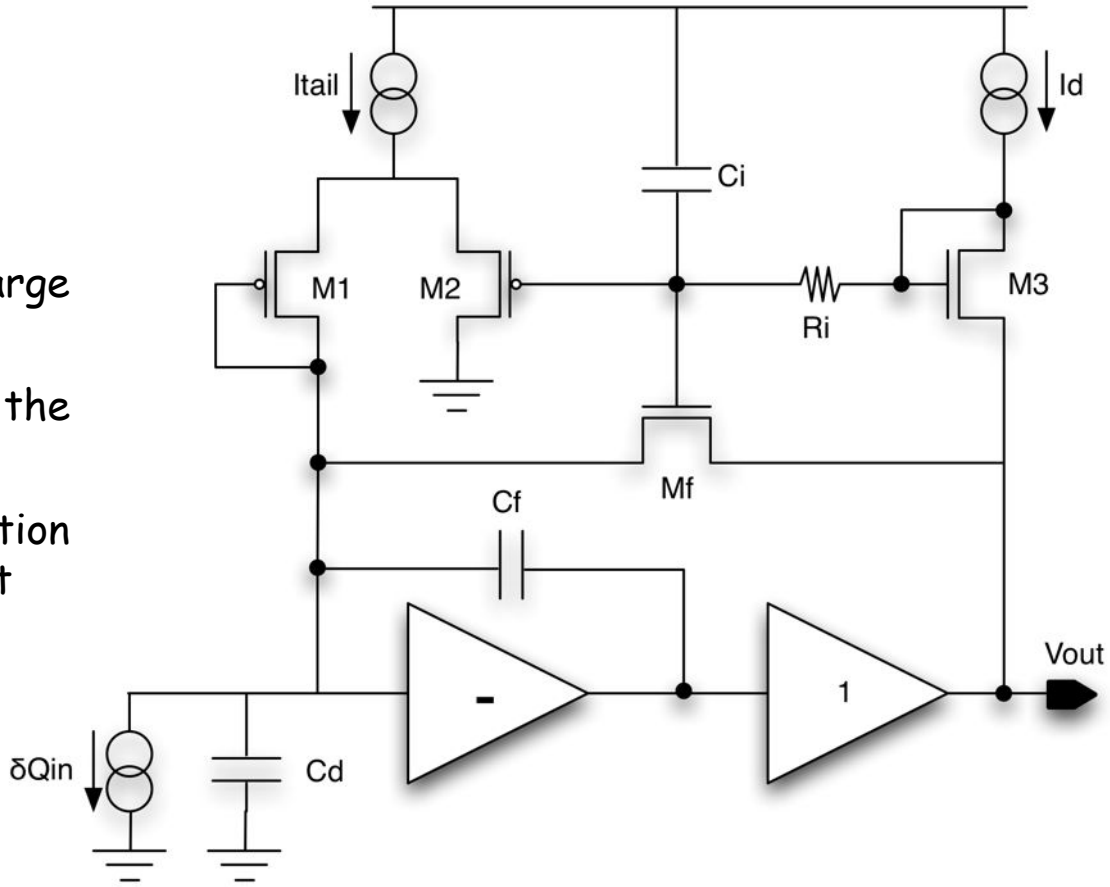




- ✓**Synchronous** front-end with **zero dead time**
- ✓Preamplifier (Regulated cascode) featuring a leakage current compensation circuit
- ✓**Digital conversion** immediately after the preamplifier
- ✓ 35 e rms **threshold dispersion**, ≈ 80 e rms **ENC** @ CD=50
- ✓A mini@asic including a 16x16 matrix with a simple readout has been sumbitted in June, Test board assembled → chip ready for the characterization

Charge sensitive amplifier

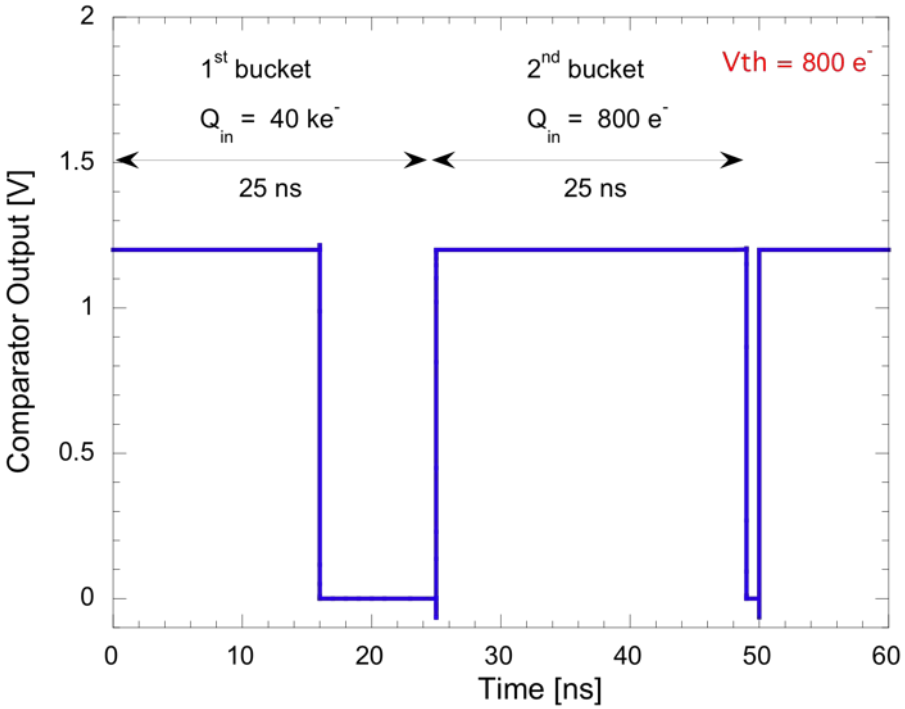
- ✓**Regulated cascode** design
- ✓Active feedback transistor Mf:
  - ✓**1/gm resistor** for small signals
  - ✓**Constant current source** for large signal.
  - ✓M1 provides a DC path for the **detector leakage current**
  - ✓Ri + Ci ensures low frequency operation of the leakage compensation circuit
- ✓**Current consumption** ~ 4.0 *μA*

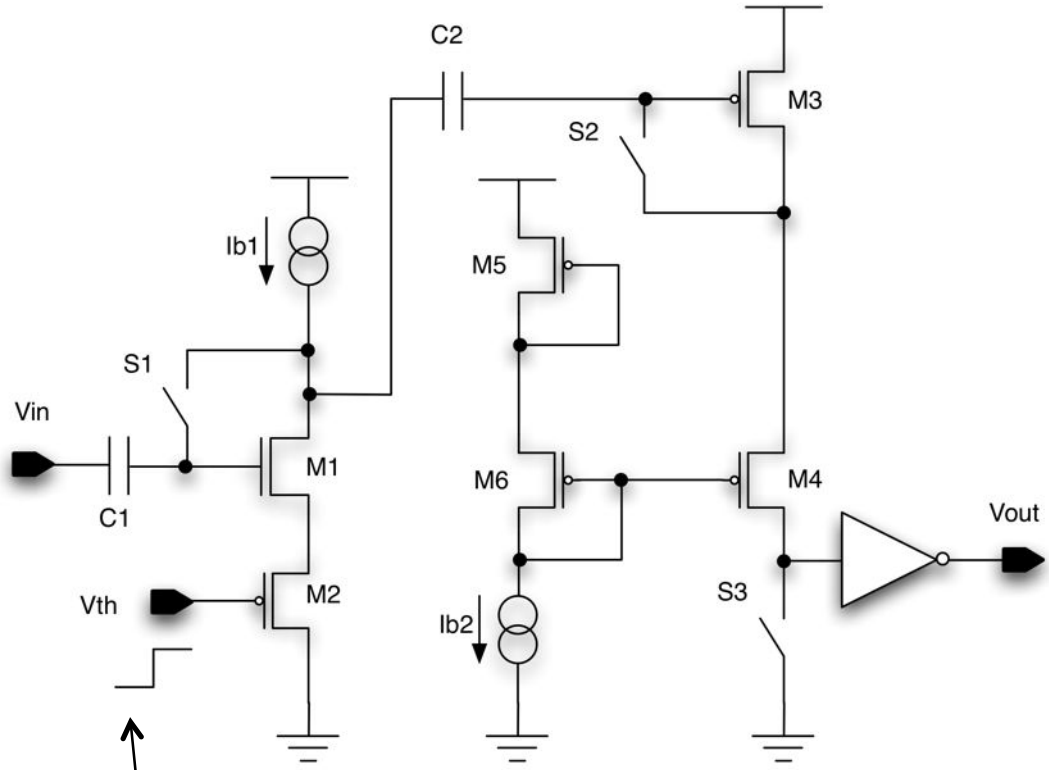


Comparator

- ✓ Compact, single-ended architecture
- ✓ **AC coupled** to the preamplifier
- ✓ **Correlated double sampling:**
  - ✓ Auto-zeroed
  - ✓ Increased pileup immunity
  - ✓ No need for trimming DAC

Simulation results





Vth step generated in-pixel

- ✓ 12.5ns **reset phase**; 12.5ns **active comparison**
- ✓ **~ 1μA current consumption**

L.Gaioni et al, "A 65 nm CMOS analog processor with zero dead time for future pixel detectors", presented @ VCI 2016, 15-19 February, Vienna

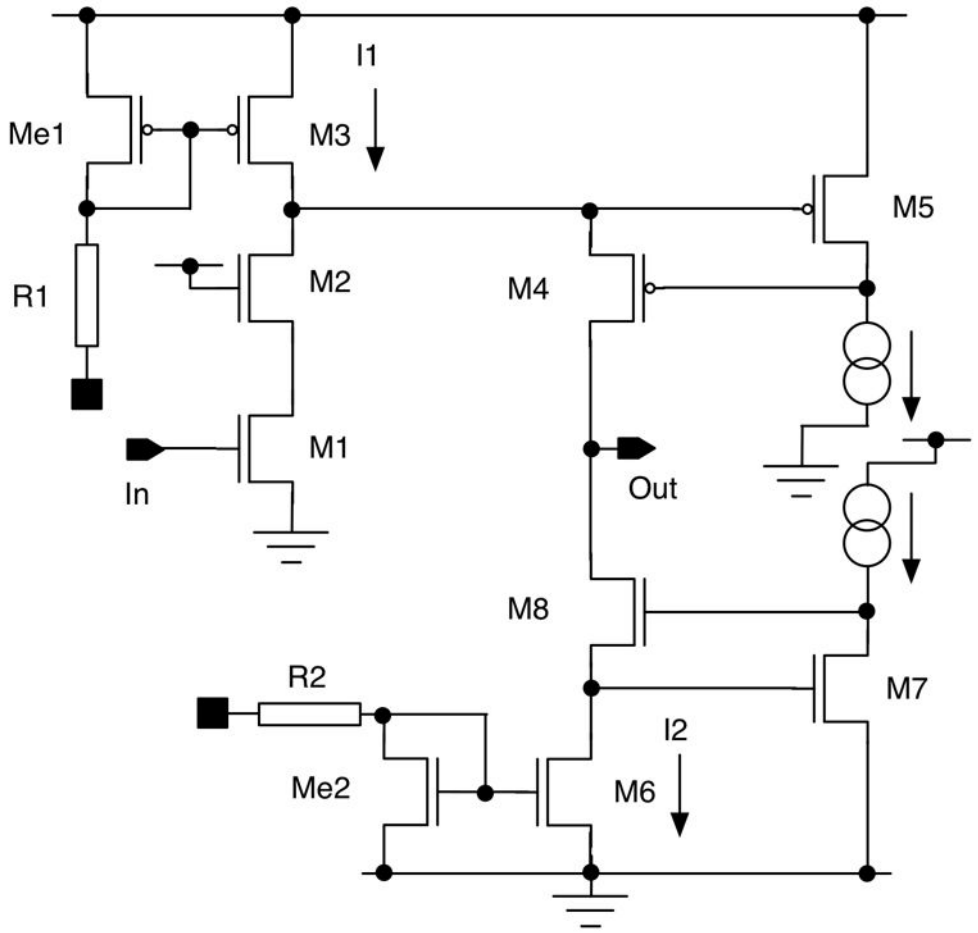
Conclusions

- **Critical features** of future pixel detectors include **hit rate**, **low threshold**, **low noise** operation and **radiation hardness**
- The **RD53A demonstrator** is being developed in the framework of the RD53 Collaboration in a **65 nm CMOS technology**
- The full scale chip will be submitted at the end of March 2017. Goal of the RD53A chip is to demonstrate the feasibility of the 65 nm technology in facing the challenging requirements set by the **future experiment upgrades at the HL_LHC**
- **FE65-P2** and **CHIPIX65** demonstrators represent very important steps towards the integration of the full scale chip
  - Excellent bare chip results have been obtained for the FE65-P2
  - CHIPIX65 demonstrator to be characterized soon. Smaller test structures including analog FE have been characterized, with very promising results

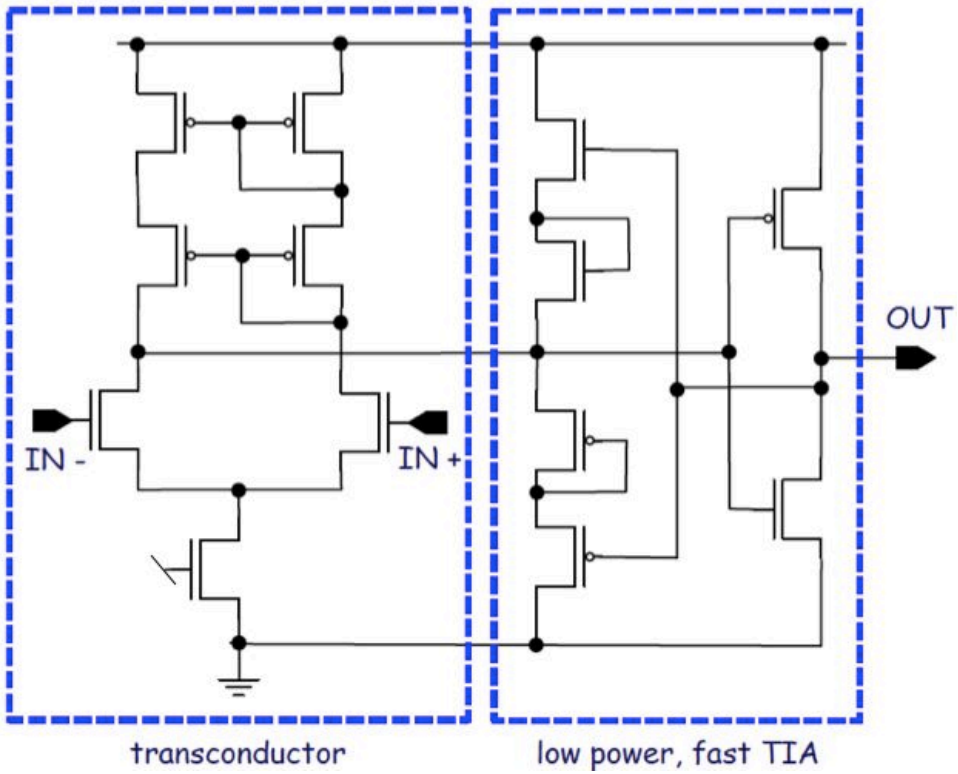
Backup slides

PV/BG AFE schematic diagrams

Preamplifier



Comparator

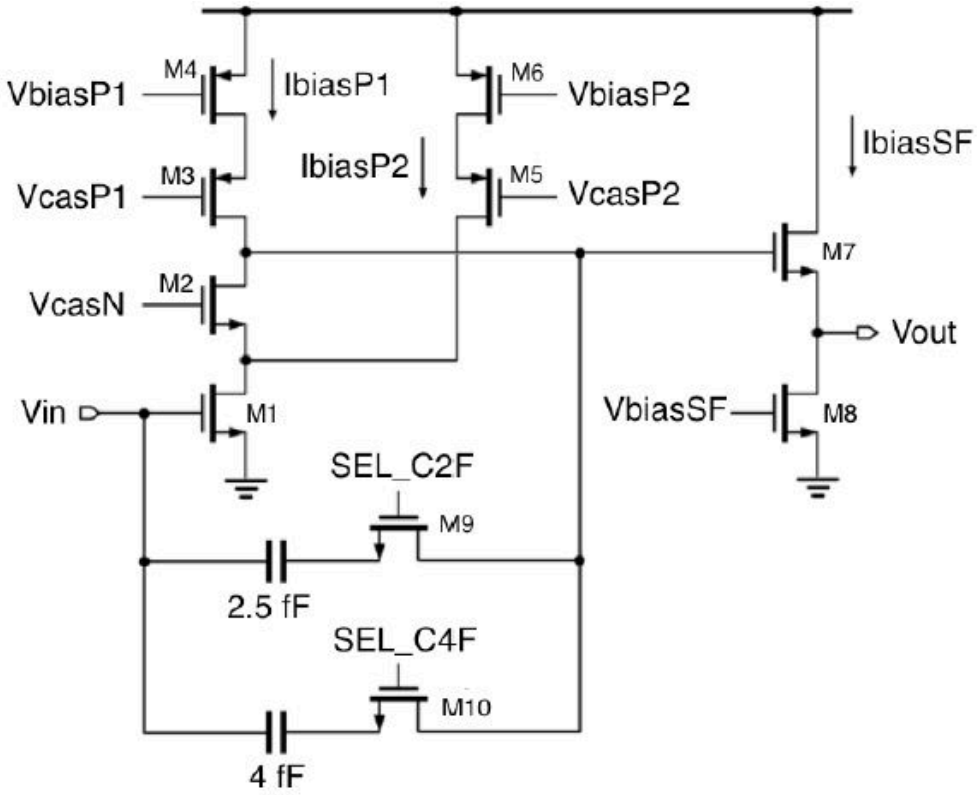


- Gain stage based on a **folded cascode** configuration (~3 uA absorbed current) with a regulated cascode load

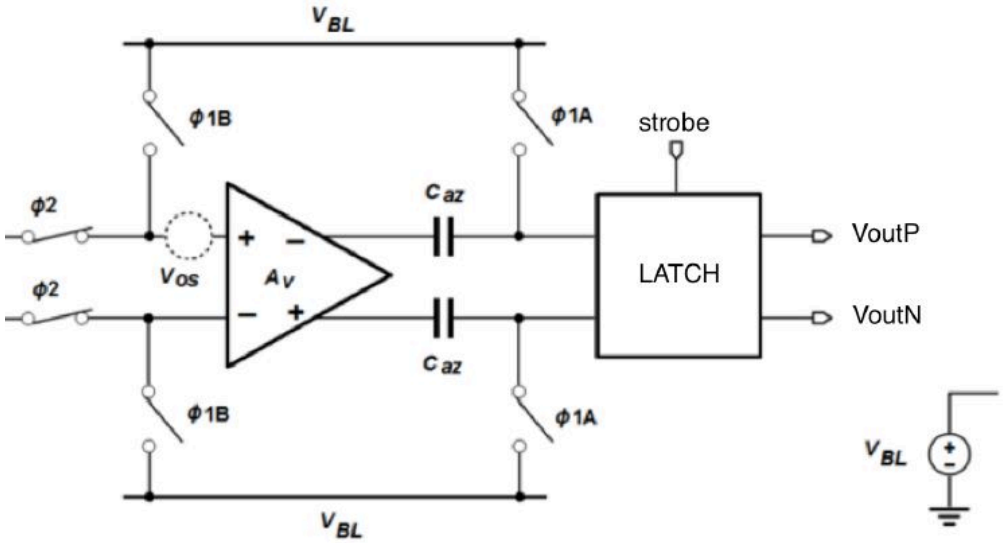
- Low power, **fast discriminator** (<1 uA absorbed current) including Gm stage and a transimpedance amplifier providing a low impedance path for fast switching

TO AFE schematic diagrams

Preamplifier



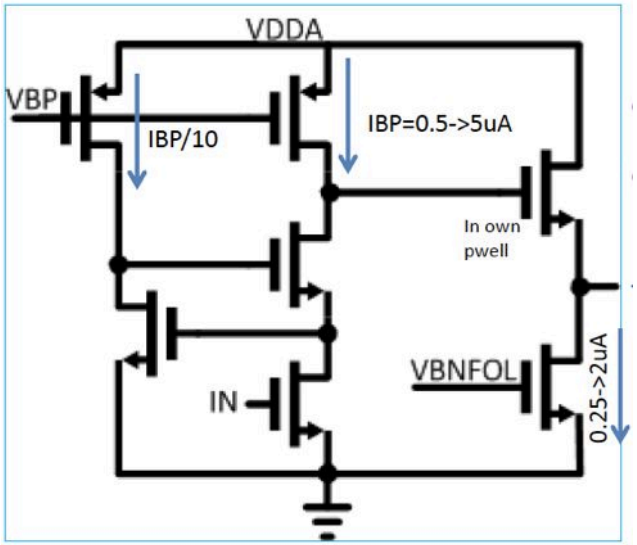
Comparator



- Cascode with current splitting and source follower
- Two selectable values of feedback capacitance

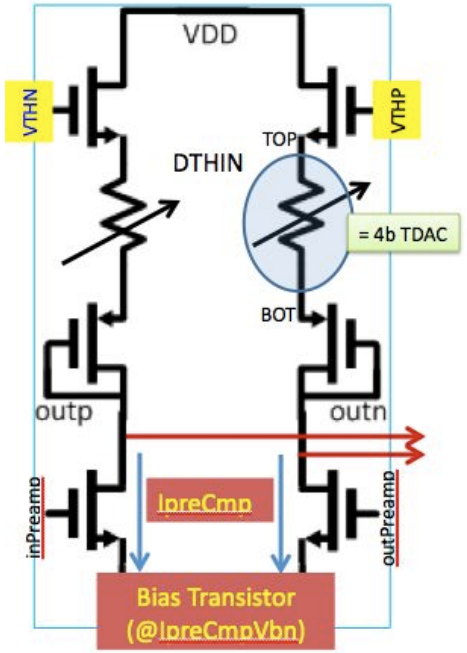
- Offset (and mismatch) cancellation based on **comparator autozero** (store offset on a capacitor, and then subtract it from signal + offset)

LBNL AFE schematic diagrams



Preamplifier

- Gain stage with active cascode
- Simple follower as buffer



Pre-comp

- Fully differential amp w/ resistive load
- Acts as single-to-differential converter
- Global Vth DACs generates effective differential supplies
- Local DTHn trims binary-weighted resistive load
- Sets output CM and differential OP for comp