Operational Experience of the ATLAS SemiConductor Tracker and Pixel Detector

Dave Robinson

Cavendish Laboratory, University of Cambridge, UK

On behalf of the ATLAS Inner Detector

VERTEX 2016

25th International Workshop on Vertex Detectors

La Biodola 25-30 September 2016
The ATLAS Inner detector

<table>
<thead>
<tr>
<th></th>
<th>Channels</th>
<th>Element Size</th>
<th>Resolution (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRT</td>
<td>$3.5 \times 10^5$</td>
<td>4mm</td>
<td>130</td>
</tr>
<tr>
<td>SCT</td>
<td>$6.3 \times 10^6$</td>
<td>80µm x 12cm</td>
<td>17 x 570</td>
</tr>
<tr>
<td>Pixels</td>
<td>$80 \times 10^6$</td>
<td>50µm x 400µm</td>
<td>10 x 115</td>
</tr>
<tr>
<td>IBL</td>
<td>$12 \times 10^6$</td>
<td>50µm x 250µm</td>
<td>8 x 40</td>
</tr>
</tbody>
</table>

IBL covered in Yosuke’s talk
The Pixel Detector

- 3 hit system $|\eta|<2.5$
- 3 barrels and 3 disks
- $1.7m^2$ of silicon
- $C_3F_8$ evaporative cooling

- 1744 modules
  - One size 62.4x21.4mm
  - 250µm thick n-on-n sensor
  - 328x144 pixels
- 16 FE chips per module
  - Charge measurement using 8-bit ToT information
  - Zero suppression in FE chip, MCC builds event
The Semi Conductor Tracker (SCT)

- 61 m² of silicon with 6.2 million readout channels
- 4088 modules arranged in 4 Barrels and 18 Disks (9 each end)
- Barrels: |\eta| < 1.1 to 1.4, End-caps: 1.1 to 1.4 < |\eta| < 2.5
- 30cm < R < 52cm, space point resolution rϕ ~16\mu m

- \(C_3F_8\) Cooling (-7°C to +4.5°C silicon) to limit radiation damage
- Radiation hard: tested to \(2 \times 10^{14}\) 1-MeV neutron equivalent/cm²
- Lightweight: 3% X0 per layer
- Mechanically rigid
The SCT Module (basic detector unit)

- Back-to-back sensors, glued to highly thermally conductive substrates for mech/thermal stability, wire-bonded to form ~12cm long strips
- 40mrad stereo angle between opp sides
- 1536 channels (768 on each side)
- 5.6W/module (rising to ~10W after 10 yrs LHC)
- Binary readout (hit=signal>threshold)
- 3 consecutive time bins sampled per trigger

- 2112 barrel modules
  - one shape

- 1976 end-cap modules
  - 3 shapes
• Challenges in delivering optimal DAQ efficiency and Data Quality from the ATLAS silicon tracking detectors
  – Routine optimisation
  – Unforeseen technical issues
  – DAQ for increasing pileup and trigger rate
  – Radiation damage effects
• Focus mainly on the SemiConductor Tracker
  – Plus non-common issues with Pixel detector
• Tracking performance metrics *not* covered
  – Hit efficiency, Lorentz Angle, dE/dx etc
The LHC Roadmap and Performance

**LHC**

<table>
<thead>
<tr>
<th>Run 1</th>
<th>Run 2</th>
<th>Run 3</th>
<th>Run 4 - 5...</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>LS1</strong></td>
<td><strong>EYETS</strong></td>
<td><strong>LS2</strong></td>
<td><strong>LS3</strong></td>
</tr>
<tr>
<td>splice consolidation button collimators R2E project</td>
<td>13 TeV</td>
<td>injector upgrade cryo Point 4 DS collimation P2−P7(11 T dip.) Civil Eng. P1-P5</td>
<td>14 TeV</td>
</tr>
<tr>
<td>2011</td>
<td>2013</td>
<td>2015</td>
<td>2019</td>
</tr>
<tr>
<td>experiment beam pipes</td>
<td>nominal luminosity</td>
<td>experiment upgrade phase 1</td>
<td>cryo limit interaction regions</td>
</tr>
<tr>
<td>7 TeV</td>
<td>8 TeV</td>
<td>13.5-14 TeV</td>
<td>14 TeV</td>
</tr>
<tr>
<td>2017</td>
<td>2018</td>
<td>2020</td>
<td>2022</td>
</tr>
<tr>
<td>30 fb⁻¹</td>
<td>150 fb⁻¹</td>
<td>300 fb⁻¹</td>
<td>3000 fb⁻¹</td>
</tr>
<tr>
<td>2023</td>
<td>2025</td>
<td>2026</td>
<td>2037</td>
</tr>
</tbody>
</table>

**ATLAS Online Luminosity**

- **LHC Delivered**
- **ATLAS Recorded**

Total Delivered: 29.3 fb⁻¹
Total Recorded: 27.1 fb⁻¹

**ATLAS Online Luminosity**

- 2011 pp \(\sqrt{s} = 7\) TeV
- 2012 pp \(\sqrt{s} = 8\) TeV
- 2015 pp \(\sqrt{s} = 13\) TeV
- 2016 pp \(\sqrt{s} = 13\) TeV
The ATLAS tracker was designed for a nominal luminosity of $1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ with a $\langle \mu \rangle$ of ~23 at a 70kHz L1 rate.

This has been routinely exceeded in 2016, with ATLAS striving for a L1 trigger rate of 100Hz to fully exploit physics potential.

Overcoming existing bandwidth constraints has been a specific challenge, in addition to the ‘conventional’ challenges associated with operating complex tracking systems.
Operations Experience in a nutshell

*In general, smooth and efficient operation*

<table>
<thead>
<tr>
<th>Year</th>
<th>Pixel</th>
<th>SCT</th>
<th>Pixel</th>
<th>SCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>99.9</td>
<td>99.8</td>
<td>97.5</td>
<td>99.1</td>
</tr>
<tr>
<td>2012</td>
<td>99.9</td>
<td><strong>99.1</strong></td>
<td>95.0</td>
<td>99.0</td>
</tr>
<tr>
<td>2015</td>
<td><strong>93.5</strong></td>
<td>99.4</td>
<td>98.0</td>
<td><strong>98.6</strong></td>
</tr>
<tr>
<td>Today</td>
<td>98.9</td>
<td>99.9</td>
<td><strong>98.3</strong></td>
<td><strong>98.7</strong></td>
</tr>
</tbody>
</table>

*Points of note*

- TX optical failures in Run1
- Refurbishment of Pixel detector during LS1
- DAQ firmware issues impacting efficiency
- DAQ upgrades to address bandwidth limitations

In general, smooth and efficient operation

VERTEX2016  D Robinson
The SemiConductor Tracker

- Optical link monitoring and issues
- DAQ Upgrade for higher pileup and luminosity
- Radiation Damage effects
  - Current, depletion voltage, noise and gain
- Calibration and optimisation
SCT DAQ and Optical Communication
Off-detector schematic largely common with Pixels

- ATLAS Central DAQ
- TTC Interface Module
- Read Out Driver (ROD)
- Back Of Crate (BOC)
- Front end module

- TTC (optical)
- ROD (optical)
- ROD Busy
- TTC Busy
- Commands and Triggers
- 40 MHz Clock

- Formatted Data (optical)
- S-link (1/BOC)
- Clock and Control (optical) 48/BOC
- Data (optical) 48 pairs / BOC

- ATLAS Trigger System
- P-I-N
- VCSEL

VERTEX2016  D Robinson
Optical Links
Monitoring and use of Redundancy

- ATLAS Central DAQ
- TTC Interface Module
- Front end module
- ATLAS Trigger System

**Read Out Driver (ROD)**
- x16/crate
- Commands and Triggers
- 40 MHz Clock

**Back Of Crate (BOC)**
- x16/crate
- Clock and Control (optical) 48/BOC
- Data (optical) 48 pairs / BOC

**Formatted Data (optical)**
- S-link (1/BOC)

**Vertex 2016**
D Robinson
Optical Links – Module Communication

On-detector IPIN & VCSELs \( \times 4088 \)

Back of Crate Cards \( \times 128 \)
Up to 48 modules/BOC
Optical monitoring

IPIN trends

TX Channel Deaths

RX Optical Thresholds
Run1 TX Failures

Channel failures in the 12-channel VCSEL arrays assembled to ‘TX plugins’ mounted on the BOC

- Affected both SCT and Pixel
- At its worst, ~30 deaths/week
- SCT deployed redundancy
  - (Pixels could not)
- Truelight originals
  - ESD from inadequate factory precautions
- Truelight first replacements
  - Humidity ingress (non hermetic seal)
- AOC second replacements
  - CTE mismatch (epoxy - VCSEL array)
    - But death rate very low, still used today
- LightABLE engines
  - Only one infant mortality in Run2
**Optical link Redundancy Options**

Standard Readout: 6 chips / FE link

- RX Redundancy: 12 chips / FE link

TX Redundancy: Groups of 12 modules form a ‘redundancy loop’ whereby a module can be configured to receive the TX stream from the neighbouring module.

<table>
<thead>
<tr>
<th>Use of Optical Link Redundancy</th>
<th>Links</th>
<th>End Run1</th>
<th>Today</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX Redundancy</td>
<td>4088</td>
<td>14 (up to 240)</td>
<td>27</td>
</tr>
<tr>
<td>RX Redundancy</td>
<td>8176</td>
<td>132</td>
<td>147</td>
</tr>
</tbody>
</table>

VERTEX2016  D Robinson
SCT DAQ Bottlenecks

128 S-links (90 before LS1): 32bit wide transfer at 40MHz = 1.28Gbps

8176 FE optical links, 6 chips per link
Redundancy option: 12 chips/link
Data transmitted at 40 Mbps
SCT Bandwidth in Run1 (8TeV, 50ns)

**Pileup Limits for Run1 and Run2 extrapolation**

<table>
<thead>
<tr>
<th></th>
<th>8TeV 50ns 70kHz</th>
<th>14TeV 25ns 100kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE Links</td>
<td>&gt;120</td>
<td>87</td>
</tr>
<tr>
<td>Slinks</td>
<td>77</td>
<td>30</td>
</tr>
</tbody>
</table>

Expansion of SCT DAQ in LS1 (90→128 RODs/BOCs)

48→36 modules / ROD, smaller fragment size
SCT Bandwidth in Run2
13 TeV, 25ns, expanded DAQ
SCT Bandwidth in Run2
13 TeV, 25ns, expanded DAQ

Pileup limit at 100kHz is ~55
Assumes we disable some chips on links using RX redundancy
~60 chips, ~0.1% of detector

Limit is more pessimistic than 8TeV extrapolations
Presence of IBL
Non-linear extrapolation due to trigger bias
Data stream differences
Radiation Effects

Leak current at 0 °C [μA/cm²]

Year

2011 2012 2013 2014 2015

7 TeV 8 TeV 13 TeV

Sensor temperature

Int. luminosity delivered

Layer Data Model prediction
Barrel 3 ⋅ ± 1 σ
Barrel 4 ▲ ± 1 σ
Barrel 5 ▲ ± 1 σ
Barrel 6 ▼ ± 1 σ

Hamburg-Dortmund Model

ATLAS SCT Preliminary

VERTEX2016 D Robinson
SCT Long Term Projections

Models for a plausible LHC performance scenario

Peaks by 2024:
- Depletion ~200V
- Leakage current ~1.3 mA
19.6% of endcap sensors are a fundamentally different design and different manufacturer
- But same specification

Unstable leakage currents with collisions
More pronounced on module sides facing large volumes
- Ionization effects?
Mitigated by reducing HV during non-physics periods and reducing HV below nominal to depletion level
Mean Noise and Gain evolution during Run1

145 V < HV < 155 V

ATLAS Preliminary

Integrated luminosity delivered:
- × 1
- × 10
- × 100

Noise

Gain

Legend:
- Inner barrels <111>
- Outer barrels <111>
- Inner barrels <100>
- Outer barrels <100>
- Inner endcaps (Hamamatsu)
- Inner endcaps (CIS)
- Middle short (CIS)
- Middle endcaps (Hamamatsu)
- Middle endcaps (CIS)
- Outer endcaps
Link averaged noise history to today

ATLAS SCT Preliminary

145V < HV < 155V

VERTEX2016 D Robinson
Single Event Upsets

- Desynchronisation of module due to energy deposition in ipin diode
- Chip high occupancy or no hits, due to bit flips in chip config registers

Effective recovery in place:
- Module reconfiguration on the fly following desynchronisation (within 1 minute)
- Global reconfiguration (entire SCT) every 30 minutes to recover chips
Calibration

Calibration performed every 2-3 weeks: to impose a 1fC threshold across all chips to ensure low noise (<5x10^{-4}) and high hit efficiency

*Common 8-bit discriminator threshold for each chip*

*4-bit trim DAC per channel to correct for channel threshold variations*

‘Noisy strip’ means occupancy > 1.5% in empty bunch crossings
Pixel Upgrades during LS1

Complete extraction and re-insertion to accommodate installation of new Service Quarter Panels (nSQPs)

April-Dec 2013: Pixel on the surface
Jan-April 2014: Electrical and service reconnection
The new Service Quarter Panels

Primary motivation to replace old SQPs which were a significant source of module defects.

Additional improvements:
- On-detector opto-transceivers (optoboards) moved outside of ID enclosure (accessibility)
- Extra readout fibres to double layer-1 readout bandwidth to 160MB/s
Impact of nSQPs and repairs to all accessible defects

Active module count
95% (End of Run1)
98.3% (Start of Run2)
LS1 Pixel Readout Upgrades

- Focus on improving bandwidth from cavern to Readout Drivers in USA15 (Counting Room), made possible by nSQPs
- Plan replacement of RODs (by newly developed IBL RODs), at least for Layer 2, early in Run2
  - More CPU, more input channels and output bandwidth

<table>
<thead>
<tr>
<th>Layer</th>
<th>Run1</th>
<th>Post-LS1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>160 MB/s</td>
<td>160 MB/s (2x80)</td>
</tr>
<tr>
<td>1</td>
<td>80 MB/s</td>
<td>Up to 160 MB/s (2x80)</td>
</tr>
<tr>
<td>2</td>
<td>40 MB/s</td>
<td>80 MB/s</td>
</tr>
</tbody>
</table>
New Pixel Readout for Run2

IBL RODs and BOCs were installed end of 2015 for layer 2 readout
- fully exploits the 80Mbps FE bandwidth implemented in LS1
- multiple S-links for improved Slink bandwidth
- same upgrade planned for Layer 1 end of 2016

B-Layer readout (old ROD/BOC hardware) problematic in 2016
- B-layer should cope with factor 2-3 beyond current occupancy
- high pileup and rate exposed ROD processing issues...

Decision in 2016 to replace all readout to one common system
Pixel DAQ Optimisation Strategy

**Reduction of B-layer occupancy** to mitigate B-layer ROD issues

**Firmware developments** continually evolving for both new IBL RODs and old Si RODs

**Recovery mechanisms** implemented mid-2016 for SEU-induced desynchronisation and BUSY

**DAQ efficiency significantly improved during 2016**
Summary & Outlook

• The ATLAS tracker is now operating with luminosities and pileup that are well beyond design limits, and continues to deliver excellent tracking performance with >99% DQ efficiency after meeting numerous challenges
• DAQ and bandwidth limitations are the dominant issues so far in Run2
  – Further increases in luminosity and pileup will be extremely challenging
• Radiation damage effects follow expectations
  – With some curious anomalies which have not impacted significantly on operations
• Numerous technical challenges have been overcome and we have gained enormous operations experience and understanding of our tracking detectors
• The biggest challenge by far is retaining and/or nurturing expertise in these very complex and mature systems
Backup
SCT Timing and impact of 25ns trains

• Binary Readout
  – Hit or no hit

• 3 time bins of 25ns (LHC clock) around trigger
  – Charge>threshold=hit

• 3 different readout modes
  – XXX: no requirement
  – X1X: hit in bin 1 required
  – 01X: hit in bin 1 required and no hit in bin 0

01X is required for 25ns beams to veto hits from previous BC
→ Suppress ‘ghost tracks’
Leads to ~0.05% drop in hit efficiency for all except the first bunch in train
→ Drop is function of bunch intensity
Pixel Calibration

FE records **Time-over-Threshold** as proxy for deposited charge - counted in units of BC
Used for **tracking** (NN cluster seed and improving residuals), dE/dx etc

- Tuned to 30BC @ 20ke
  - Typical threshold/noise ~ 3500e/170e
  - Preamplifier risetime can shift low ToT hits to next BC → **TimeWalk**
    - Recovered by “ToT doubling”
      - Copy low ToT hits to previous BC
The ASICs (ABCD Chips)

- 128 channel ASIC with binary architecture
- Radiation-hard DMILL technology
- 12 chips per module (6 each side)
- glued to hybrid (Cu/polyimide flex circuit)
- 40MHz (25ns) clock
- 20ns front end shaping time

![Diagram of ASIC components]

- Pipeline contains 3.3μs history of hit data
- 3 pipeline bins read out
- Timing optimised using pattern of hits in the 3 time bins (to 01X)
Optical Communication & Power Supplies

8 ROD crates (128 ROD/BOC pairs)

88 Power Supply Crates

8 ROD crates (128 ROD/BOC pairs)

88 Power Supply Crates

LV: - $V_{dd}$ - $V_{cc}$ - $V_{vcSEL}$ - $V_{pin}$

HV: - $V_{bias}$

DCS

P-I-N receives Timing, Trigger & Control
VCSEL* for each link (side) returns data

* VCSEL=Vertical Cavity Surface Emitting Laser

VERTEX2016  D Robinson
Detector elements - straws chambers filled with Xe or Ar based mixtures

Low Level threshold: tracking and dE/dX measurements

High Level threshold: TR measurements
TRT Tracking Properties

Average occupancy around track

<\mu> = 28

Accuracy of track position measurement in straw

Barrel

EC

Xe

Ar

2016 running conditions
On-Detector IPINs
Proxy for TX light intensity

ATLAS SCT Preliminary

Relative Change in $I_{PIN}$ [\% / fb$^{-1}$]

SCT Module Grouping
- Barrel layers
- DAQ Crates
- Endcap A Disks
- Endcap C Disks
- Endcap A Rings
- Endcap C Rings
- Quadrants

2015, Fit range [0.5, 4.0] fb$^{-1}$
2016, Fit range: [0.5, 29.0] fb$^{-1}$
The Thermo-siphon Project

Replacement for the compressor system for cooling the SCT (and pixels) using 90m drop of C$_3$F$_8$ feed from the surface to the cavern to provide pressure

3 independent cooling circuits, no moving parts in the primary (detector) circuit