A Prototype of a New Generation Readout ASIC in 65nm CMOS for Pixel Detectors at HL-LHC

E. Monteil1,2, L. Pacher1,2, A. Paterno1,2, S. Marconi3,19, F. Loddo2, N. Demaria1, L. Gaiolivi1,10, F. De Caniol1,10, G. Magazzu7, G. Traversi6,10, A. Rivetti11, M. Da Rocha Rolo1, G. Dellecasa1, G. Mazzia1, C. Marzoccai,8, F. Licciulli,5, F. Cicirellio5,9, V. Re10,1, L. Ratti10,1, P. Placidi4,11, A. Stabile11, S. Mattiazzo12, C. Verti14

Motivation

Pixel detectors for HL-LHC experiments require the development of a new generation front-end chip to stand unprecedented radiation levels, very high hit rates and increased pixel granularity.

The main requirements for the HL-LHC detectors:
- Small chips: 50x50 μm
- Large chips: 2x2 cm²
- Trigger up to 1 MHz with 12.8 μs latency (100x in both buffering and readout)
- For innermost layer:
  - Pixel hit rate up to 3 GHz/cm²
  - Radiation: 1 Grad in 10 years
  - Data readout up to 4-5 Gb/s

CHIPIX65 project

Approved by INFN in fall 2013, with the goals of:
- Developing a CHIP for Pixel detectors using the 65nm CMOS technology for the first time in HEP experiments
- Propagate the use of the 65nm technology inside INFN
- 8 sections involved (Bari, Lecce, Milano, Padova, Pavia/Bergamo, Perugia, Pisa, Torino)
- Funding members of the CERN RD53 collaboration

CHIPIX65 demonstrator

Dimensions: 3.5 mm x 5.1 mm

Pixel region:
- Focused on a centralised fully shared latency buffer
- 4x4 pixel region
  - Allows better sharing of resources like trigger matching
  - Number of memory locations/pixel should scale by a factor of about 2

Digital architecture

The region digital logic is composed of:
- Hit mapper/writer – manages the pixel interfaces and drives the latency buffer
- Latency buffers
- Trigger matcher
- Output FSM/MUX – implements the column drain protocol

Bias and monitoring

- 16 current DACs
- Current mirrored from DACs to les cells
- Compatible with a matrix of 40x800 pixels
- Offset compensation done with capacitors (no trimming needed)
- Fast ToT using the latch as a local oscillator (up to 800 MHz)

End of Column, Readout and I/O

SUMMARY OF THE ARCHITECTURE PERFORMANCES

LATENCY BUFFER

- The event inefficiency depends on the number of latency buffer locations: 16 locations have been used in the CHIPPIX65 demonstrator
determining inefficiency ≈ 0.1 %

Features
- Design a small and complex pixel matrix containing new solutions compatible with RDS53A
- 64x64 pixels (50x50 μm each)
- Two analog FEs (async and sync)
- A novel digital architecture
- Bias network and monitoring
- Chip configuration based on SPI protocol
- Usage of CERN I/O library
- Submitted in late June 2016

Design flow:
- Digital-On-Top chip assembly
- Top-down hierarchical flow
- Pixel matrix composed of 16x16 pixel regions (master and slave)
- A pixel region contains the digital architecture and the analog FEs

Bias network

- 10-bit current steering DAC – LSB = 10 nA
- 8-way segmented DAC (2 binary weighted + 8 unitary decided cells)
- Characterised in lab
- Irradiation tests at Padova X-ray machine showed no significant degradation

Chip configuration

- Configuration at 13.33 MHz using fully-differential synchronous SPI master/slave transactions
- 24-bit SPI words contain configuration commands and payload data

CONCLUSIONS

- CHIP66 is a INFN project with around 40 people and 8 institutes and is a very active part of the CERN RD53 collaboration
- Two analog chips have been designed, tested and irradiated
- Several IPs blocks have been developed, tested, and irradiated
- The chip contains a novel Pixel Region architecture with digital efficiency ≈ 0.5% in the HL-LHC rate (2 Gb/s/cm²) and providing 5-bit ToT information of 99.6% of hits
- The CHIP65 demonstrator, containing a matrix of 40x800 pixels, is an intermediate step towards the RD53A prototype
- The chip has been submitted at the end of June 2016