C. Deplano
On behalf of the ALICE Collaboration

ALICE ITS

OPERATIONAL EXPERIENCE
Outline

- ALICE Experiment

- The Inner Tracking System (ITS)
  - Description of the Detectors
  - Trigger Performance
  - Highlights from RUN2 Operation

- ITS Physics Performance
  - Tracking
  - Particle Identification
  - Vertexing

- Summary & Conclusion
ALICE → A Large Ion Collider Experiment at LHC

- Conceived to study the **physics** of **strongly interacting matter** and the **properties** of the **Quark-Gluon Plasma** produced in **ultra-relativistic heavy-ions** collisions

- **Program for pp and p-Pb collisions**

**ALICE Central Barrel:**

- **Pseudo-rapidity** range $|\eta| < 0.9$
- **Tracking** in high density collision
  - Up to 150 points along the track
  - $dN/d\eta = 2000$
    - (0-5% Pb-Pb @ $\sqrt{s} = 5$ TeV)

**Particle Identification**

- based on: $dE/dx$, time of flight, transition and Cherenkov radiation, calorimetry and topological reconstruction

**Transverse momentum**

- range: $(0.1 \div 100)$ GeV/c
- Low material budget (10% $X_0$ for ITS+TPC)
- Moderate solenoidal magnetic field of $B = 0.5$ T
Central Barrel Tracking

ALICE Central Barrel Global Tracking and PID

- **Inner Tracking System (ITS)**
- **Time-Projection Chamber (TPC)**
- **Transition Radiation Detector (TRD)**
- **Time-Of-Flight (TOF)**
ALICE Inner Tracking System

**INNER TRACKING SYSTEM**

- Improve primary vertex reconstruction, momentum and angular resolution of tracks from outer detectors
- Reconstruct Secondary vertex with high resolution
- Tracking and PID of low $p_T$ particles, also in stand-alone
  - Analogue information for the 4 outermost layers $\rightarrow$ PID via d$E$/dx
- Measurement of charged particles pseudo-rapidity distribution
- Pileup rejection
- Prompt trigger capability ($<$ 800 ns latency) $\rightarrow$ contribution to ALICE Level-0 trigger

**ITS Detectors**

- 6 layers instrumented with 3 different technologies
  - **SPD**: Silicon Pixel Detector for the two inner layers
  - **SDD**: Silicon Drift Detector for the two central layers
  - **SSD**: Silicon double-sided Strip Detector for the two outer layers
### More Detector Features

- **Good spatial precision**
- **Radial Coverage**
  - Inwards $\rightarrow$ **Beam pipe** constraint
  - Outwards $\rightarrow$ Inner **TPC vessel** and **TPC track matching** requirements
- **Material Budget** per layer is $\sim 1\% X_0$ for straight track perpendicular to the surface

### Table: ALICE Inner Tracking System

<table>
<thead>
<tr>
<th>Layer</th>
<th>Det.</th>
<th>Radius (cm)</th>
<th>Length (cm)</th>
<th>Surface (m²)</th>
<th>Chan.</th>
<th>Spatial precision $r\phi$ (μm)</th>
<th>z (μm)</th>
<th>Cell (μm²)</th>
<th>Max occupancy Pb-Pb (%)</th>
<th>Power dissipation (W)</th>
<th>Material Budget X/X₀</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>SPD</td>
<td>3.9</td>
<td>28.2</td>
<td>0.21</td>
<td>9.8M</td>
<td>12</td>
<td>100</td>
<td>50x425</td>
<td>2.1</td>
<td>1.35k</td>
<td>1.14</td>
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<tr>
<td>2</td>
<td></td>
<td>7.6</td>
<td>28.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.6</td>
<td></td>
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<tr>
<td>3</td>
<td>SDD</td>
<td>15.0</td>
<td>44.4</td>
<td>1.31</td>
<td>133k</td>
<td>35</td>
<td>25</td>
<td>202x294</td>
<td>2.5</td>
<td>1.05k</td>
<td>1.13</td>
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<tr>
<td>4</td>
<td></td>
<td>23.9</td>
<td>59.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.0</td>
<td>1.26</td>
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<tr>
<td>5</td>
<td>SSD</td>
<td>38.0</td>
<td>86.2</td>
<td>5.0</td>
<td>2.6M</td>
<td>20</td>
<td>830</td>
<td>95x40000</td>
<td>4.0</td>
<td>850</td>
<td>0.83</td>
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<tr>
<td>6</td>
<td></td>
<td>43.0</td>
<td>97.8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.3</td>
<td>0.86</td>
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</table>
Silicon Pixel Detector – SPD

- 120 **Half-Staves modules grouped in two half barrels**
  - Each semi-barrel divided in 10 **semi-sectors** containing 6 **Half-Staves**
    - 2 HS in the **Inner Layer** (ITS layer1) and 4 HS in the **Outer Layer** (ITS layer2)
  - Each Half-Stave containing 2 **ladders**
    - Each ladder containing 1 **sensor** (200 μm thick) and 5 **readout** chips (150 μm)
    - Hybrid pixel detector with a binary output
    - p+n reverse biased (50 V) sensor with pixel size 425x50 μm² [z x rϕ]

- **Evaporative C₄F₁₀ cooling** system
Current Status:

- 6 Module recovered during Long Shutdown 1 (LS1)
- 4 modules excluded during RUN1
- 1 Hot module
- 1 Data Wrongly formatted
- 1 Multi Event Buffer Problem
- 1 Data not sent
The SPD contributes to the **First Trigger Level** with the **Fast-OR** signals
- Fast-Or bit per pixel chip @ 10 MHz \(\rightarrow\) signals if at least 1/8192 pixel is fired
- **Hits** and **Fast-OR** are both recorded in the data using 4-Events deep **Multi-Event Buffer**
- The read-out strobes on the two separate lines must be matched in time (unit of 100 ns delays)

**RUN2 L0 trigger classes** including the **SPD Trigger** (**pp collisions**)
- Online **Background** Estimator (2015)
- **High multiplicity** (2015)
- **Double Gap Diffractive** (2016)
High Multiplicity Trigger

- SPD: Fast-Or signals (100 ns time window)
- High Beam **Background** Signal in Layer_1
  - Online Beam **Background Mitigation** with forward rapidity detectors
  - Online **Past-Future Protection**: events are accepted only if no other collisions are present in a time window of \( \pm 7 \) Bunch Crossing
- Collected Events \( \rightarrow 140 \times 10^6 \)

SPD Algorithm

- \( Fired\_Layer1 \geq 0 \)
- \( Fired\_Layer2 \geq 70 \)
L0 Trigger – Double Gap Diffractive

Double Gap Diffractive Trigger

- **Low multiplicity** events (2 to 4 tracks)
- Looking for **double gaps @ forward rapidity**
  - Veto with forward rapidity detectors
- Looking for **events @ mid-rapidity → SPD**
  - Fast-Or signals

SPD Algorithm

- **Correlated tracklets** in the 2 SPD layers
  - Based on *pixel chips in a cone*
  - *rϕ* correlation
- **Topological Trigger** with programmable acceptance
  - **Opening angle** between two tracklets
  - **Min** and **Max number** of tracklets

![Diagram of SPD layers and tracklets](image)
Silicon Drift Detector – SDD

- 260 silicon drift modules (300 μm thick)
  - Inner layer (ITS layer 3) → 14 ladders (with 6 modules)
  - Outer layer (ITS layer 4) → 22 ladders (with 8 modules)
    - 512 collection anodes with a pitch (z) of 294 μm
    - Drift HV: 1.8 kV
    - Drift velocity ~ 6.7 μm/ns

- Leak-less water cooling system

Central Cathode @ -HV

Voltage Divider

Anodes

FE electronics CMOS 0.25 μm
PASCAL + AMBRA ASICs

87.6 mm
75.3 mm
72.5 mm
70.2 mm

SDD Barrel Outer Layer

collection anodes
MOS injectors

Sensitive region
Drift cathodes
Guard region

Higher voltage cathode
MOS injectors

Data

Commands

Trigger

LV supply

HV supply

E_{drift}

v_{d}(e^-)

E_{drift}

v_{d}(e^-)

Caterina Deplano

VERTEX 2016 – La Biodola, Isola d’Elba, Italy

25-30 September 2016

12/23
SDD – Operational Performance

<table>
<thead>
<tr>
<th>SDD</th>
<th>Availability in Data Taking</th>
<th>Acceptance [# of modules]</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN1</td>
<td>92%</td>
<td>87%</td>
</tr>
<tr>
<td>RUN2</td>
<td>98.4%</td>
<td>82.8%</td>
</tr>
</tbody>
</table>

- **Bad modules** excluded for:
  - Front End Electronics (HV/noise/shorts/disconnected)

- **Drift speed** is stable
  - Measured at the **beginning** of each fill with MOS injectors implanted on the detector surface
  - 0.1% precision on drift speed is needed to reach the nominal resolution of 25 μm along the drift region
2016 → Recovery Time Improved

- SuperCarlosRX Readout board (LS1) → FPGA (Xilinx Virtex5) firmware modified to improve the recovery if one or more Front-End chips lose the configuration (like baseline, threshold, masks)
  → caused by SEU

- **Automatic procedure** implemented to detect noisy chips and eventually reload the configuration event by event
  - Configuration lost → 1 Noisy Chip → 64 anodes
  - Event size of JTAG reload ~600kB

- **No need to stop** and restart the run
  → recovery time ~ 800 μs

- Since September 2016 the information related to the reconfigured chip is encoded in the Data Header
Silicon Strip Detector – SSD

- **1698 silicon strip modules** (300μm thick)
  - **Inner** layer (ITS layer 5)
    - 34 ladders (22 modules each)
  - **Outer** layer (ITS layer 6)
    - 38 ladders (25 modules each)
  - **768 double-sided strip** sensors per module
    - Strip: **pitch** (rφ): 95 μm; **length** (z): 40 mm
    - Stereo angle: 35 mrad
      - ✓ position resolution bending direction
  - p+n reverse bias optimized for each half ladder (20V ÷ 80V)
  - Outputs pure analog signals

- **Leak-less water cooling** system + air dryer system
**Current Status:**

- 6 Half Ladders excluded since RUN1
- 1 Half Ladder recovered during LS1 (problem related to the water cooling)
- 1 Half Ladder excluded during RUN2 commissioning due to disconnected JTAG signals

<table>
<thead>
<tr>
<th>SSD</th>
<th>Availability in Data Taking</th>
<th>Acceptance [# of Modules]</th>
</tr>
</thead>
<tbody>
<tr>
<td>RUN1</td>
<td>96%</td>
<td>91%</td>
</tr>
<tr>
<td>RUN2</td>
<td>98.6%</td>
<td>91%</td>
</tr>
</tbody>
</table>
SSD Front End Read Out Module electronics:

- A side crates → located in the cavern just outside the L3 magnet
  - Analog Data Digitization and Time tagging
  - Offset correction and zero-suppression
  - Xilinx SRAM FPGA → 224 FPGA
    - 8 * 1 Link module boards: 8 * 1 FPGA XC2V1000FG456 (VIRTEX II)
    - 8 * 9 AD module boards: 9 * 3 FPGA XC2S50EPQ208 (SPARTAN II)
  - Xilinx Rad Hard PROM → (2 every 28 FPGAs)
    - 8 Link Module boards → 8 * 2 PROM XQR18V04CC44M

- Exposed to radiations (simulation 10 year data taking)
  - TID 4 \(10^{-4}\) Gray
  - Fluences \([p/cm^2]\) above 20 MeV: \((p, \pi \rightarrow 2.5 \times 10^5)\) \((n \rightarrow 3.5 \times 10^6)\)

**Subjected to Single Event Upset Mitigations** by Design:

- Data Parity Check
- JTAG used for FPGA reconfiguration
- Poly switch fuses to protect power supply from latch-up
**Issues – SSD SEU**

**Suspected SEU (SRAM FPGA):**

- **Run1** → **4** in pp collisions + **3** in p-Pb collisions
- **LS1** – **Mitigations added:**
  - Radiation Tolerant PROM
  - Firmware upgrade to allow a faster FPGA reload

- **Run2_2015** → **8** in pp collisions
  - ALICE Integrated Luminosity 7.1 pb\(^{-1}\)
  - Mitigations added in Run2:
    - Optimization of the operational procedure to minimize the Data Tacking stopping time

- **Run2_2016** (till 13 Sept) → **10** in pp collisions
  - ALICE Integrated Luminosity 11.35 pb\(^{-1}\)

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*Mean SEU rate looks about 1 SEU/pb\(^{-1}\)*
Issues – SSD SEU

**SEU Signature:**
- **Error** appears under the beam presence
- **High** data size not correlated with the occupancy and **not recoverable** with a pedestal runs
- **Error** on the data transmitted via optical link
  - **firmware reload** needed

**SEU @ RUN2 versus Time**
- **SEU** looks **correlated** to the ALICE integrated **luminosity** and the **fluence** on RadMon12
  - **Low Statistic** to make predictions
  - Currently **→ Improve** the **recovery time** during the data acquisition
    - 2015 → 20 min
    - 2016 → 5 min
ITS Physics Performance

**Tracking Performance**
- Very good track matching between ITS and TPC

**Transverse Momentum Resolution**
- ITS extends the $p_T$ range down to 80÷100 MeV/c
Particle Identification

- **PID combined with standalone tracking**
  - K-π separation in the range $\rightarrow (0.1 \div 0.45)$ GeV/c
  - K-p separation in the range $\rightarrow (0.1 \div 1)$ GeV/c
Impact parameter resolution

- **Weak dependence** on the colliding system and very good **MC description**
- **Very good impact parameter** resolution
  - $\sigma_d = 60 \, \mu m \, @ \, p_T = 1 \, GeV/c$
  - Allows reconstruction of **secondary vertices**
    - $D^+ (ct \sim 312 \, mm)$
    - $D^0 (ct \sim 123 \, mm)$
    - $D_s (ct \sim 150 \, mm)$

Summary & Conclusion

- **ALICE Inner Tracking System** has been in operation during **RUN1** and since the beginning of **RUN2**
  - Participation to pp, p-Pb and Pb-Pb **data taking** with **high efficiency**
  - SPD, SDD, and SSD **perform** remarkably **well** and **according** to the **specifications**
  - **New procedures** developed to **minimize** the **recovery** time related to SEU
  - The **SPD** contributes to the **L0** trigger with **new algorithms**

- **Performance** in agreement with the design requirements and **stable** with time
  - **Standalone** capability allows to **track** and **identify charged particles** with **momenta** down to 100 MeV/c
  - **PID** performance allows for **separation** of **pions, kaons and protons** down to very **low** $p_T$
  - **Impact parameter resolution** of about 60 μm or better for tracks with $p_T \geq 1$ GeV/c allows the reconstruction of charmed **secondary vertices**

Stay tuned:

… the **upgrade is coming** !!!

- “**The Upgrade of the ALICE ITS**” by Stefania Beolè (Tuesday morning)
- “**Tracking in High-multiplicity Events**” by Maximiliano Puccio (Friday morning)

Thank you for Your Attention!
Backup
ALICE Global tracking strategy

1. Vertex with SPD
2. Seeds in outer part of TPC (lowest track density)
3. Inward tracking from the outer to the inner TPC wall
4. Matching the outer SSD layer and tracking in the ITS
5. Outward tracking from ITS to outer detectors (TRD, TOF)
6. Inward refitting to ITS
7. Refining vertex with optimal resolution
- Expected increase of dead areas
- Switching on and off HV => thermal cycles that in turn cause the detaching of the readout chips from the sensor
- Dead pixels are due to missing bump bondings at the 4 corners of the chip. Other contributions are from
  - Dead pixel from construction
  - Inefficient pixels
- Inefficient and dead pixel in hs in DAQ:
  - Run 1 (2013) 2%
  - Run 2 (2015) 4.5%

From A. Mastroserio @ Pixel 2016
Silicon Pixel Detector – SPD

- The SPD contributes to the First Trigger Level with the Fast-OR signals
  - **Hits** and **Fast-OR** are both recorded in the data using 4 deep Multi-Event Buffer
  - The read-out strobes on the two separate lines must be matched in time (unit of 100 ns delays)

![Diagram of Silicon Pixel Detector](image)

- **Hits to Routers**

- At beginning of RUN2 the Level0-Level1 trigger latency has been changed in the Central Trigger Processor from 6.5 μs to 7 μs
After the L0-L1 latency change, 100 ns needed be compensated in the Hits links to align them with respect to the FastOR links:

- Compensated in the pixel internal register \textit{misc}
- The \textit{misc} register only get two values corresponding to 0 and 100 ns delay
- During Run1 it was configured with 0 ns delay

With this setting in the \textit{misc} register a time mismatch between Hits and Fast-OR data has been observed for all chips:

- Reconstructed Hits are assigned to the wrong event
- The time mismatch changes cyclically by step of 100 ns: from 100 ns to 300 ns, it recovers and then restart with 100 ns mismatch
- The same pattern is repeated along the run
- The problem seems to be related to a faulty behavior of the delay register \textit{“misc”}

Solution

\rightarrow the needed delay has been compensated in the off-detector read-out electronics
**L0 Trigger – Background Estimator**

- **Bunch-bunch** collisions:
  - Same number of fired pixel in both SPD layers
  - Distribution of the difference of fired pixels (Layer2 – Layer1) peaked in zero

- **Bunch-gas** collisions:
  - Large difference in the number of fired pixels in the two SPD layers

- **SPD Algorithm OSX2**:
  - Fired\_Layer1 – Fired\_Layer2 > Threshold

- **Background Separation** proven with LHC Transfer Line Test (2015):
  - Beam quenched on the TDI
    - only background
  - Fired\_Layer1 – Fired\_Layer2 > 20
  - Background reduction of 40 %
  - Correlation found among OSX2 and BLM
- **Injector Events** used to calculate the drift speed

- Drift speed measured with **MOS Injectors** implanted on the detector surface during standalone runs

- **0.1% precision** on drift speed is needed to reach the **nominal resolution** of 25 μm along the drift region
Run2 Issues – Ventilation Machine

Issue spotted on June 2015 ⇒ increasing leakage current of some SSD modules

- High current for a long time can lead to permanent sensors damage
  ⇒ detector switched OFF

- Problem related to increasing air humidity from the DESSICA ventilation machine
  - Series of interventions allowed to take the conditions under control until end 2015
  - Difficult to get the spares of some key components; not reliable
  - Planned to install a new ventilation machine during the YETS 2015 ⇒ SAMP machine

Requirements:
Surface Absolute Humidity $\text{AH} \sim 1.35 \text{ g/kgas}$ ($\Rightarrow \text{RH} = 10\% @ T=19 \text{ deg C}$)
Relative Humidity inside SSD $\Rightarrow 10\% < \text{RH} < 15\% (@ T = 20 \text{ deg C})$
Run2 Issues – Ventilation Machine

- **Absolute Humidity** AH adjustable in the range 1 to 1.5 g/kgas
- **Air quality**: Class 1000 (ISO6) filtering stage at the output of the machine
- **Fixed flow** of 350 m$^3$/h (100 m$^3$/h to SSD)
- Installed during YETS and commissioned on Mars/April 2016
- Several T and RH **sensors monitored** from the SSD DCS interface
AH is **inside** the **requested range**

Bigger amplitude wrt DESSICA (winter) but we are in summer

2\textsuperscript{nd} SAMP machine validation from the company done in July 2016