Development and construction of the Belle II DEPFET pixel vertex detector


B. Schwenker for the DEPFET collaboration
Outline

- SuperKEKB and Belle II experiment
- The Belle II vertex detector
- Test results from final ASIC generation
  - Using small scale test demonstrator
- Results from VXD beam test
  - Large scale demonstrator / prev. ASIC generation
- Summary and outlook
The DEPFET collaboration

- Original collaboration: DEPFET pixel detector @ ILC (since 2002)
- Now: design, deliver and operate PXD for Belle II

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University of Bonn (J. Dingfelder)
University of Hamburg (C. Hagner)
University of Heidelberg (P. Fischer)
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University of Göttingen (A. Frey)
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University of Mainz (C. Sfienti)
MPG Semiconductor Laboratory, Munich (J. Ninkovic)
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MPI for Physics, Munich (H.-G. Moser)
Technical University, Munich (S. Paul, A.Knoll)
Struct. Biol.Research Center, KEK (S. Wakatsuki)
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University of Tabuk, Saudi Arabia (R. Ayad)

DEPFET@Belle II

Management

Project Leader
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Technical Coord.
L. Andricek (HLL)

IB- Board
Chair: J. Dingfelder (Bonn)

Integration Coordinator
Shuji Tanaka (KEK)
SuperKEKB and the Belle II experiment

- SuperKEKB: Asymmetric e+e- collider @ \( E_{cm} = 10.58 \text{GeV} = m(Y(4S)) \)
- Peak luminosity \( L = 8 \times 10^{35} \text{ cm}^{-2} \text{ s}^{-1} \), 40 times higher than KEKB machine
- Nano beam schema: Beam size reduction and higher currents
The BELLE II detector

- Detector requirements
  - Vertexing capability
  - Particle identification
  - E.M. calorimetry
  - $K^0_L$ and muon ID
  - Data handling capabilities
The Belle II pixel vertex detector
Belle II vertexing requirements

<table>
<thead>
<tr>
<th></th>
<th>Belle II PXD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radiation</td>
<td>2 Mrad/year</td>
</tr>
<tr>
<td></td>
<td>$2 \cdot 10^{12}$ 1 MeV $n_{eq}$ per year</td>
</tr>
<tr>
<td>Duty cycle</td>
<td>1</td>
</tr>
<tr>
<td>Frame time</td>
<td>20 $\mu$s</td>
</tr>
<tr>
<td>Momentum range</td>
<td>50 MeV $&lt;$ p $&lt;$ multi GeV</td>
</tr>
<tr>
<td>Acceptance</td>
<td>17$^\circ$-155$^\circ$</td>
</tr>
<tr>
<td>Material budget</td>
<td>0.2% $X_0$</td>
</tr>
</tbody>
</table>

- Modest impact parameter resolution (15 μm), dominated by multiple scattering → pixel size (50 x 75 μm$^2$)
- Lowest possible material budget (0.2% $X$)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services
The Belle II vertex detector

- 2 DEPFET layers (PXD)
- 4 Double Sided Si-Strip Detector layers (SVD)
- **PXD + SVD integration**
  - Nov. 2017

<table>
<thead>
<tr>
<th></th>
<th>DEPFET PXD</th>
<th>L1</th>
<th>L2</th>
</tr>
</thead>
<tbody>
<tr>
<td># ladders</td>
<td>8</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Distance from IP (cm)</td>
<td>1.4</td>
<td>2.2</td>
<td></td>
</tr>
<tr>
<td>Sensitive thickness (μm)</td>
<td>75</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td>#pixels/module</td>
<td>768x250</td>
<td>768x250</td>
<td></td>
</tr>
<tr>
<td>Total no. of pixels</td>
<td>3.072x10⁶</td>
<td>4.608x10⁶</td>
<td></td>
</tr>
<tr>
<td>Pixel size (μm²)</td>
<td>55x50</td>
<td>60x50</td>
<td>70x50</td>
</tr>
<tr>
<td>Frame/row rate</td>
<td>50kHz/10MHz</td>
<td>50kHz/10MHz</td>
<td></td>
</tr>
<tr>
<td>Total sensitive Area (cm²)</td>
<td>89.6</td>
<td>176.9</td>
<td></td>
</tr>
</tbody>
</table>

**Total 0.2% X₀**
VXD Phase 2 hardware (Beast)

- Machine commissioning
- Radiation safe environment for the VXD
- 2 PXD and 4 SVD ladders
- +X direction, highest sensitivity to backgrounds

Integration of the phase 2 hardware (incl. other radiation monitors): November 2016 @ DESY
Installation at KEK: July 2017
The PXD module: Readout electronics

**SwitcherB - Row Control**
- Gate and Clear signal
- Rad. hard proved (36 Mrad)

**DCDB - Drain Current Digitizer**
Amplification and digitization of DEPFET signals.
- 256 input channels
- 8-bit ADC per channel
- 92 ns sampling time
- Rad. hard proved (10 Mrad)

**DHP - Data Handling Processor**
- Common mode and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Rad. Hard proved (100 Mrad)
PXD9: Belle II DEPFET Sensors

- Small matrices 80x32 pixels
  → Small test systems

- Final size modules 768x250 pixels
  → VXD test beam
  → Phase II
  → full Belle II PXD

- Small matrices 80x32 pixels
  → Small test systems
Hybrid 5: Small scale detector demonstrator

- Small PXD9 Belle II matrix
  - Pixel pitch: 50x55 μm²
  - Thinned to 75 μm
  - Gate length: 5 μm
  - Thin gate oxide (rad. hard.)
  - 32x64 pixels readout

- Final readout chain
  - SwitcherB
  - DCDB
  - DHPT
  - DHH

- All measurements at nominal speed
ASIC performance

- After optimization, all 256 DCD channels perform within specs
  - Operation at nominal speed (92ns sampling time)
  - Measure ADC curve using external current source

INLpp < 8 ADU
Median = 4.5
Noise < 0.55 ADU
Spread < 0.08 ADU
Homogeneous gain
Min to max variation
~10%
DCD noise and pedestals compression

without pedestal compression

min-max pedestal = 217 ADU

noise mean = 1.41 ADU

with pedestal compression

2bit DAC corr.

Switchable current sources at DCD inputs

min-max pedestal = 111 ADU

noise mean = 0.83 ADU
Sr90 Spectrum

**DCD4.2**
(final DCD version)

MPV = 31.75 ADU

SNR ~ 38

gate length 5µm

$g_q \sim 700 \text{ pA/e}$
PXD9: Belle II DEPFET Sensors

• ALL results are satisfactory, as expected by design and also according to simulations:
  
  ASICs performance: Noise, speed, ...
  Sensor: Charge collection, signal-to-noise, gain, ...

→ Not mentioned here: Irradiation campaigns, stability tests, other test vehicles…
Combined VXD test beam

- VXD common test beam in April 2016
- Small sector of the full Belle II VXD
  2 PXD + 4 SVD layers
- Complete VXD readout chain: HLT, monitoring, event building, PocketDAQ
- CO₂ cooling, slow control, environmental sensors
- Illumination with (up to) 6 GeV e⁻ under solenoid magnetic field (PCMAG)
- Alignment, tracking algorithms, ROI

**Goal:** System integration and Phase 2 Commissioning
Test beam setup
PXD on the SCB
SVD Cartridge
Integration into PCMAG
VXD test beam DAQ structure
PXD hit maps

Threshold = 5ADU (~1200 electrons)

Both detectors fully functional. Only a few ø(20) pixels masked
Trigger on 4 scintillators Collimated beam No magnetic field
Event display: PXD + SVD integration

Online (HLT) extrapolation to PXD → define region of interest

Track passing all SVD layers
Efficiency study in PXD

Track selection cuts:
- B-field 1T, 5GeV electron beam
- using only single track events
- select high momentum $p > 1\text{GeV}$
- $p$-value $> 0.001$

Layer 1

Layer 2

Run w/o beam

Run w/o beam
Closer look to efficiencies

:- MPV cluster signal drops for certain readout channels

:- At those places, threshold too high

→ efficiency drops

:- Need to work on gain Homogeneity

:- Head room for improvements

→ New ASICs
→ better tuning
PXD residuals

Residuals for perpendicular incident MIPs
- 14 μm (50 μm pitch)
- 18 μm (60 μm pitch)
- Measured residuals very close to digital resolution
- Spatial resolution of perp. tracks is worst case
- (small charge sharing → small clusters)
Summary and outlook

• Combined PXD-SVD beam test @ DESY
  – 2 PXD half-ladders fully operational
  – Sensors with homogeneous response
  – Hit maps, SNR OK
  – PXD residuals as expected
  – VXD correlations (mapping and timing)
  – PXD efficiency >95%, average > 98%
  – Operation with CO2 cooling (@ -27°C)
Summary and outlook

- **Belle II PXD takes shape**
  - Integration of the Phase II PXD (2 ladders) at DESY in November 2016
  - Installation of Phase II detector at KEK in summer 2017
  - Production of the Phase III detector (full 2 layer PXD) is ongoing.
  - Start integration of PXD half-shells @ DESY in spring 2017
  - Transport of PXD to KEK October 2017

Further reading: Cern Courier September 2016
Thanks
DEPFET's in a nutshell

- fully depleted sensitive volume
  - fast signal rise time (~ns), small cluster size
- In-house fabrication at MPS Semiconductor Lab
  - Wafer scale devices possible
  - Thinning to (almost) any desired thickness
  - no stitching, 100% fill factor
- no charge transfer needed
  - faster read out
  - better radiation tolerance
- Charge collection in "off" state, read out on demand
  - potentially low power device
- internal amplification
  - charge-to-current conversion
  - r/o cap. independent of sensor thickness
  - Good S/N for thin devices $\sim 40\text{nA/}\mu\text{m}$ for mip

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Current receiver, ADC chip
Commissioning schedule
ASIC performance

- DHPT1.2: Proper data transmission after 10 m Infiniband cable

![Eye diagram with 237 mV signal level](image-url)
Closer look at noise occupancy

Noise occupancy ($<10^{-6}$) from a long run w/o beam

Noise hits appear to cluster in groups of adjacent physical columns.

Always groups of 8 very noisy columns, i.e. same column pair in DCD ASIC.
In-house MPG HLL DEPFET Sensor Production

- Starting material SOI wafer: 75µm top, 450µm support
- Production in three phases, 19 lithography steps
  - 9 implantations, 2 poly-silicon layers
  - 2 aluminum layers
  - last metal copper and thinning of sensitive area
## PXD production wafer level QA tests

### Percentage of live pixels

<table>
<thead>
<tr>
<th></th>
<th>Pilot run</th>
<th>Pre-production</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>W30</td>
<td>W35</td>
</tr>
<tr>
<td>IF</td>
<td>0*</td>
<td>98.44</td>
</tr>
<tr>
<td>OF1</td>
<td>100.00</td>
<td>98.44</td>
</tr>
<tr>
<td>OF2</td>
<td>99.48</td>
<td>98.96</td>
</tr>
<tr>
<td>OB1</td>
<td>97.72</td>
<td>99.40*</td>
</tr>
<tr>
<td>OB2</td>
<td>99.48</td>
<td>0</td>
</tr>
<tr>
<td>IB</td>
<td>97.92</td>
<td>0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>83.3%</strong></td>
<td><strong>66.6%</strong></td>
</tr>
</tbody>
</table>

- 34/42 (80.1%) working sensors
- 25/42 (59.5%) prime grade sensors (>99% pixels)
- 9/42 (21.4%) second grade sensors

*Failure due to operator error during testing*
SuperKEKB Injection Scheme – Need of Electronic Shutter

- Continuous injection → ~ 400 revolutions with two noisy bunches (100ns apart) every 20 ms
- DEPFET integrates two trains, these noisy bunches would blank the frames → 20% loss of data

- The best solution: gate the DEPFET during the passage of the noisy bunches
- ~100ns gate, with some rise and fall times, twice per frame → 2x2µs of 20 µs blind
- Assuming 4 ms relaxation time (not clear), ~200 consecutive frames with gate cycles

- DEPFET operation mode during gating: DEPFET off, Clear active (Vgs=3 .. 5V, Vclear=16 .. 20V)
DEPFET Gated Mode Operation

Switching to gated mode:

» DHE receives signal from acc., sends "veto" DHPT switches to gated sequence controls Switcher
» DCD operation mode remains untouched

Normal charge collection

» Vgs=4V, Vclear=5V
» all signal charge collected in internal gate

Gated mode

» Vgs=4V, Vclear=20V
» all signal charge dumped to Clear

Challenge: switch all Clear contacts in the matrix from ~5V ~20V shown on small matrix, but as expected, it’s more difficult on large modules
VXD Cooling System

**Requirements**

- **PXD:** Sensor < 25 °C to minimize shot noise due to leakage current; ASICs < 50 °C to avoid risk of electro-migration
- **SVD:** APV25 readout chips surface@~0 °C for SNR improvement
- **Power consumption:** PXD 360W; SVD 700W, together with the heat load through 9m of vacuum isolated flex lines; required cooling capacity of 2-3kW
- **VXD needs to be thermally isolated against CDC and beam pipe. Room temperature at the inner surface of CDC is required for stable calibration and dE/dx performance**
- **IBBelle CO2 cooling plant in collaboration with CERN (currently shipped to Japan)**
- 75µm thin Si-substrates with Belle II geometry
- Glued at the narrow edge + ceramic insert to get ladders
- Resistors integrated on Si-substrates to simulate the power distribution
- Additional power of 25 W is given on the kapton cables to simulate their power dissipation
- Thermal mock-up consist of 2-layer PXD and 4-layer SVD (half of L.6 cooling pipes are under preparation)
Temperature on PXD

- Thermal and mechanical measurements to PXD have been finished. Maximum temperature along the sensor is around **20 °C in VXD volume**


Figure 5: The temperature distribution of PXD ladders along the z-direction. BW(FW) is on the left(right) side. The gray areas indicate the regions of DCD/DHP, while the 75μm thick sensitive area is shown in the center. The thick solid line indicates the averaged temperature along z-direction measured from the Pt100s. Different markers show the average temperature in y-direction at certain position along z-axis, the error bar on the marker represents the temperature range in x-direction. Thin solid lines show the temperature distribution measured by the IR camera on selected ladders.
- TIA gain adjustable by combination of feedback resistors of 26k (En30), 13k (En60) and 19k (En90)

<table>
<thead>
<tr>
<th>Rf [kOhm]</th>
<th>gain [nA/ADC]</th>
<th>range [uA]</th>
<th>range (+-100 ADC) [uA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>26 (En30)</td>
<td>75</td>
<td>19</td>
<td>15</td>
</tr>
<tr>
<td>19 (En90)</td>
<td>96</td>
<td>25</td>
<td>19</td>
</tr>
<tr>
<td>13 (En60)</td>
<td>144</td>
<td>36</td>
<td>29</td>
</tr>
<tr>
<td>8.7 (En30+En60)</td>
<td>171</td>
<td>44</td>
<td>34</td>
</tr>
<tr>
<td>7.7 (En60+En90)</td>
<td>217</td>
<td>61</td>
<td>48</td>
</tr>
<tr>
<td>6.0 (all)</td>
<td>313</td>
<td>80</td>
<td>63</td>
</tr>
</tbody>
</table>

measured with H5.0.26 with DCD4.2 by Bonn