Operational experience with the NA62 Gigatracker

Massimiliano Fiorini
(Università di Ferrara and INFN Ferrara)

On behalf of the NA62 Gigatracker Working Group:
CERN, INFN Ferrara, INFN Torino, UCL Louvain

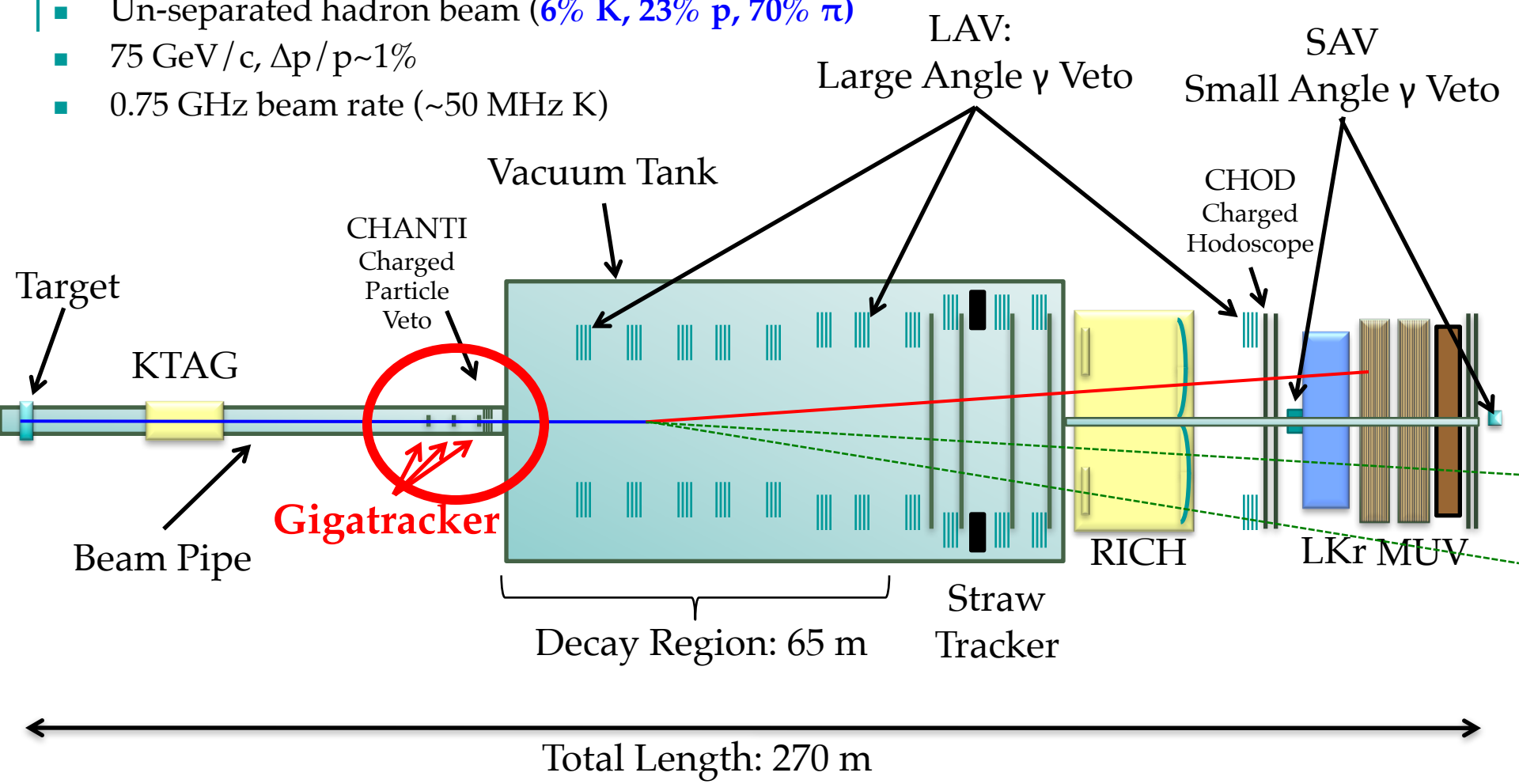
The 25th International Workshop on Vertex Detectors
La Biodola, 25-30 September 2016

Outline

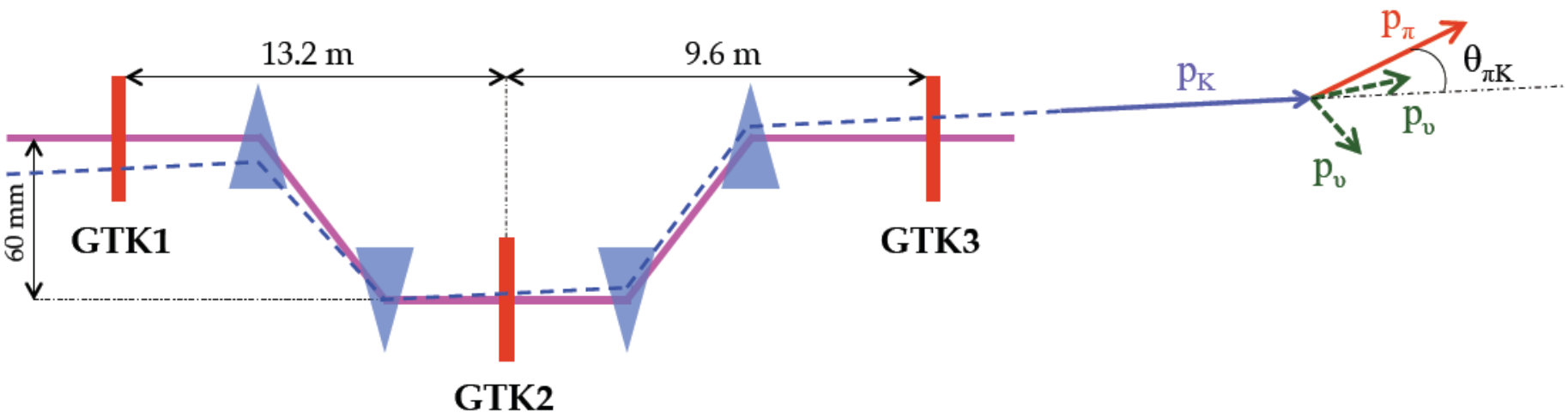
- The NA62 experiment
- Gigatracker detector system
  - Requirements from the experiment
  - Sensor technology
  - The TDCpix front-end ASIC
  - Micro-channel cooling system
- Detector performance
  - Prototype detector
  - Detector commissioning in NA62
  - Detector performance in 2015/2016 runs
- Conclusions

NA62 experiment

- Measurement of $K^+ \rightarrow \pi^+ \upsilon \bar{\upsilon}$ at the CERN SPS
- Un-separated hadron beam (**6% K, 23% p, 70% π**)
- 75 GeV/c, Δp/p~1%
- 0.75 GHz beam rate (~50 MHz K)



The GigaTracKer (GTK)

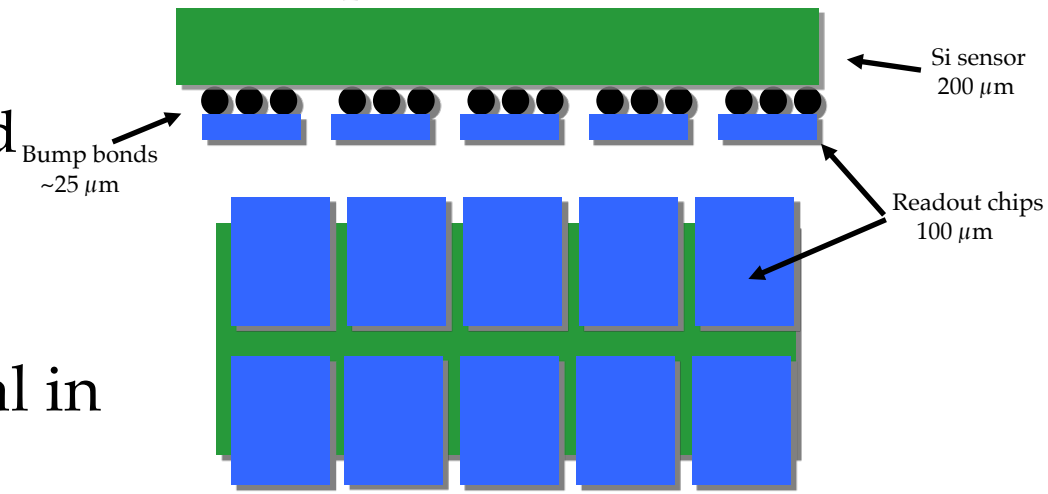


- Beam spectrometer
  - Provides momentum, time and angular measurements on all beam tracks
  - Sustains high and non-uniform rate (~150 MHz/cm^2 in the center, 0.75 GHz total)
  - Reduces multiple scattering and beam hadronic interactions

- X/X_0 ~0.5% per station
- $\sigma(p_K)/p_K$ ~0.2%
- $\sigma(\theta_K)$ ~16 μrad
- 300 μm × 300 μm pixel size
- **200 ps time resolution on single hits**

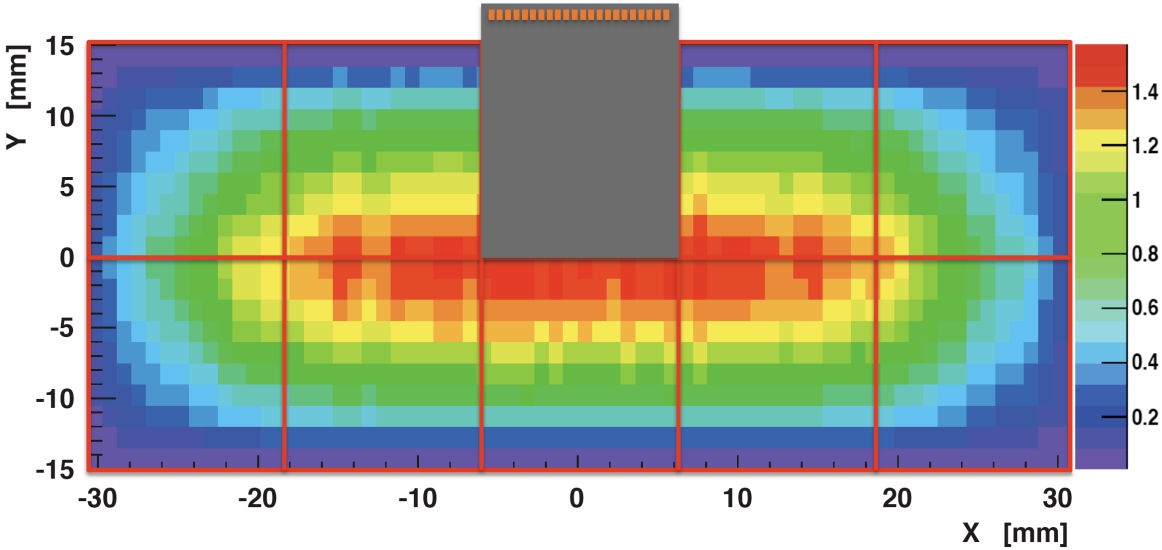
Gigatracker assembly

- Hybrid pixel detector
  - **300 μm × 300 μm** pixels
  - 1 sensor (~6×3 cm^2) bump-bonded to 10 read-out chips
- Material budget:
  - 200 μm sensor + 100 μm read-out chip → ~0.32% X_0
  - Bump bonds ~0.01% X_0
  - Mechanical support and cooling ~0.15% X_0
  - **Total** **< 0.5% X_0**
- Minimization of material in active beam area
  - Beam profile adapted: two rows of read-out chips
  - Wire connections to R/O chip outside active area



Operating environment

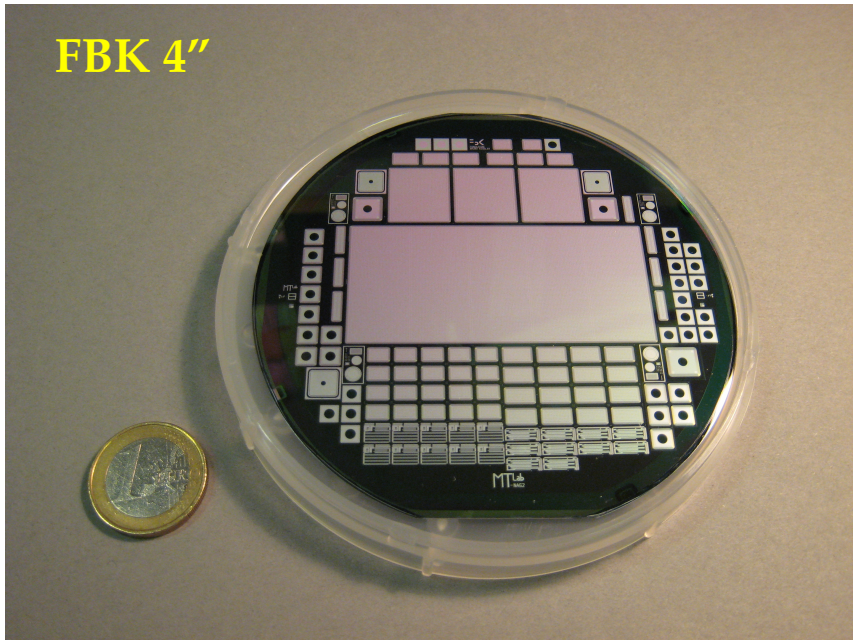
- GTK stations installed in **vacuum**
- High and non-uniform radiation levels
  - Expected fluence is **~2 × 10^{14} 1 MeV n_{eq}/cm^2** during one year of operation (~100 days) in the sensor center
- Efficient cooling necessary for stable detector operation
  - **35 W** per station
  - Very low material budget (**~0.15% X_0**) in the active beam area

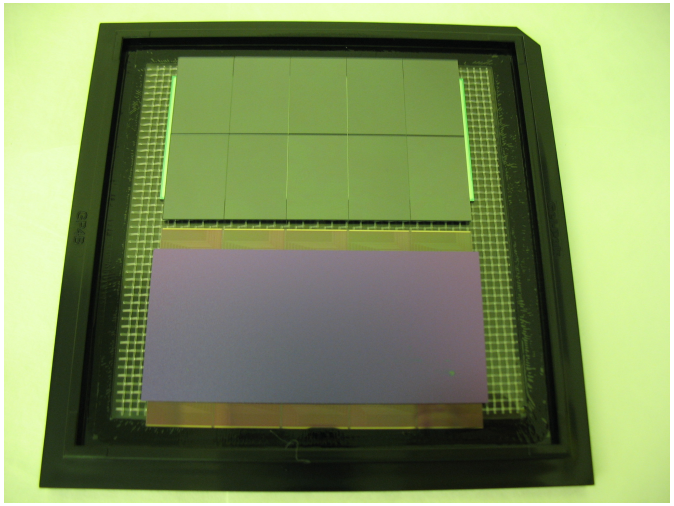


- Micro-channel cooling plate chosen by the NA62 collaboration

Sensors and bump-bonding

- 200 μm thick p-in-n and n-in-p planar sensors (FBK, CiS)
- Over-depleted operation of the detector required to achieve target time resolution (300 V over-bias)
  - Fast charge collection
- Irradiation of test structures
  - Annealing study following expected run scenario





- Flip-chip bonding and read-out wafer thinning (100 μm) done at IZM
  - Benzocyclobutene (BCB) deposition

Read-out specifications

Pixels per chip	40 columns × 45 pixels = 1800
Chip size	12 mm × 20.4 mm
Dissipated power	3.5 W
Dynamic range	3600 – 60000 e^- (0.6 – 10 fC)
Total dose in 1 year	~10^5 Gy
Time resolution	< 200 ps
Peaking time	5 ns
TDC bin size	100 ps
Efficiency per station	> 99%
Particle rate per (central) pixel	~140 kHz
Particle rate per chip	~150 MHz
Data bandwidth	4 × 3.2 Gb/s

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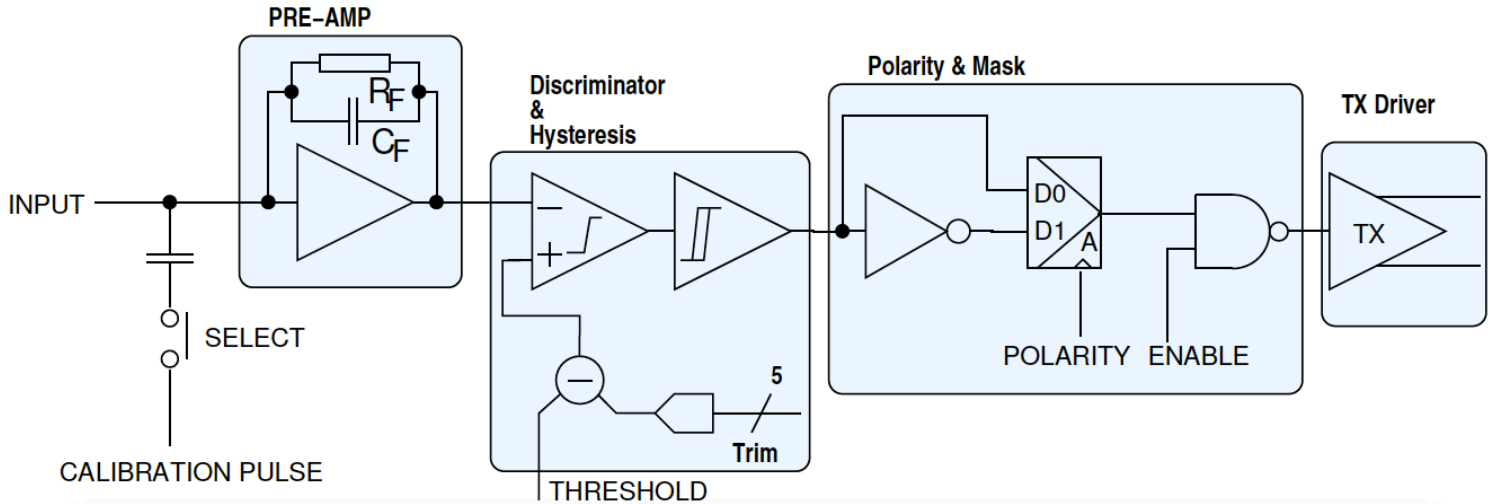
Talk by M. Noy on "Chip Development for High Time Resolution Silicon Detectors"

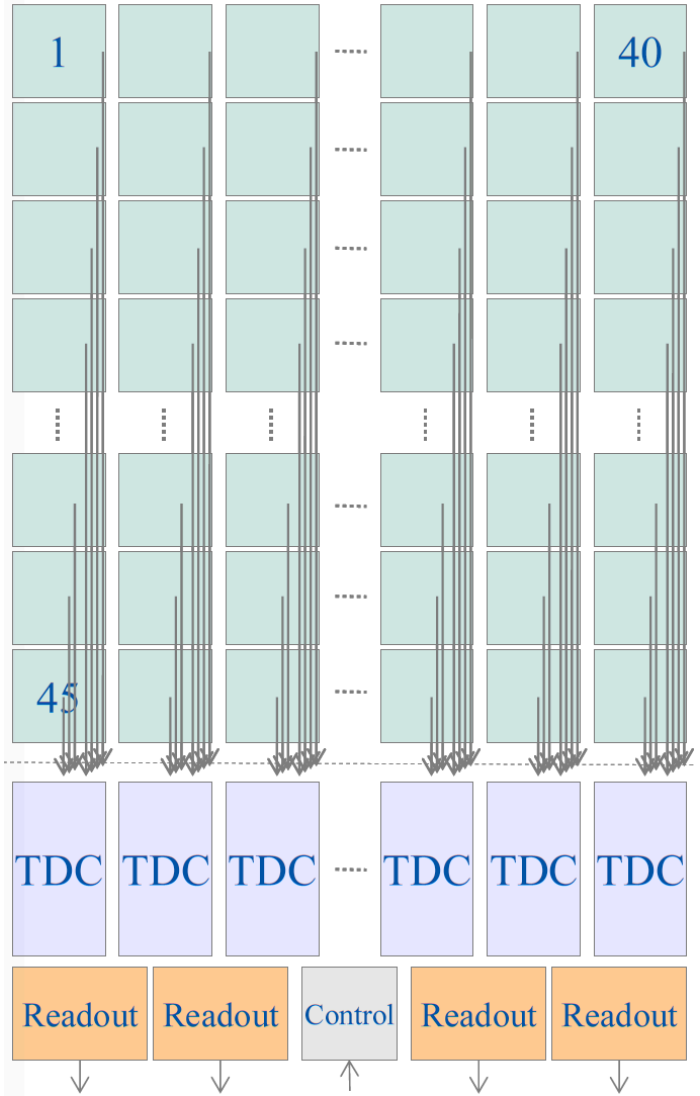
Simplified pixel architecture



- IBM 130 nm CMOS technology
- On-pixel fast preamplifier and discriminator
  - 65 mV/fC gain, 5 ns peaking time
- Asynchronous transmission lines from pixels
- Data driven architecture
- ENC ~210 e^- (170 e^- with no sensor)
- 5 bit DAC thresh. trim
- Polarity control
- Pixel mask
- TX with pre-emphasis

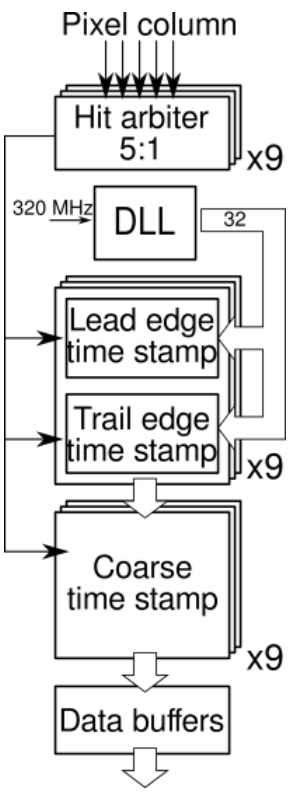
TDCpix architecture

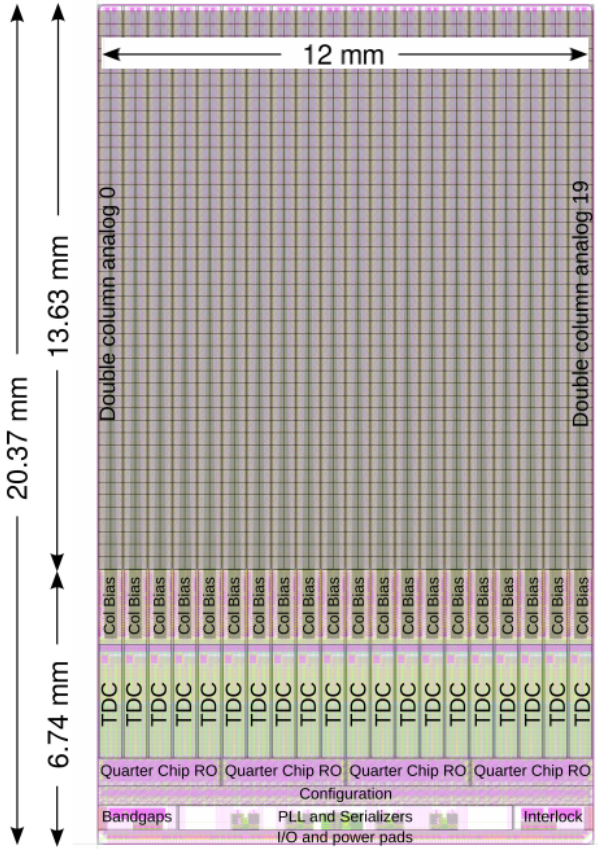
- 1800 pixels (40 × 45), 300 × 300 μm^2
  - Asynchronous
- End-of-Column (EoC)
  - Per-pixel hit signal to EoC
- 360 dual TDC channels
  - TDC Bin size 98 ps
- Self-triggered operation
  - 210 MHits/s rate
  - 4 × 3.2 Gb/s serializers
- SEU protection
  - Triplicated digital logic
- No digital activity in the matrix



Time-to-digital converter

- Digital signal from 5 pixels in a column (45 pixels) are sent to a "hit arbiter"
- A TDC pair is connected to each "hit arbiter" to measure leading and trailing edge
  - 360 TDC pairs/chip
  - 9 TDC channels per column
    - Dual edge stamping
      - Time Over Threshold
- Delay Locked Loop
  - 320 MHz reference
    - 32 bins of ~98 ps
  - Shared between two TDCs



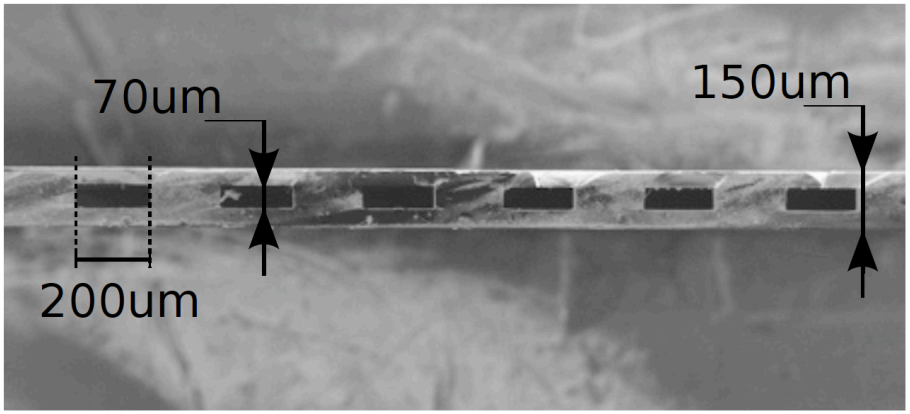


Cooling system

- Constraints
  - Material budget minimization (<0.5% X_0)
  - Detector in vacuum
  - 35 W power dissipated per station
- Micro-channel cooling matches the constraints
  - Etch channels (+ openings for inlets/outlets) in a 140 μm (210-280) thick plate glued to bump-bonded assembly
  - Circulate coolant (C_6F_{14}) in micro-channels
    - 3.5 bars pressure, 3 g/s flow
    - Two cooling circuits
    - Temperature down to -25 °C
- First application of this technique to a HEP experiment

Micro-channel cooling

- Fabricated by CEA Leti
- 200μm × 70μm channels



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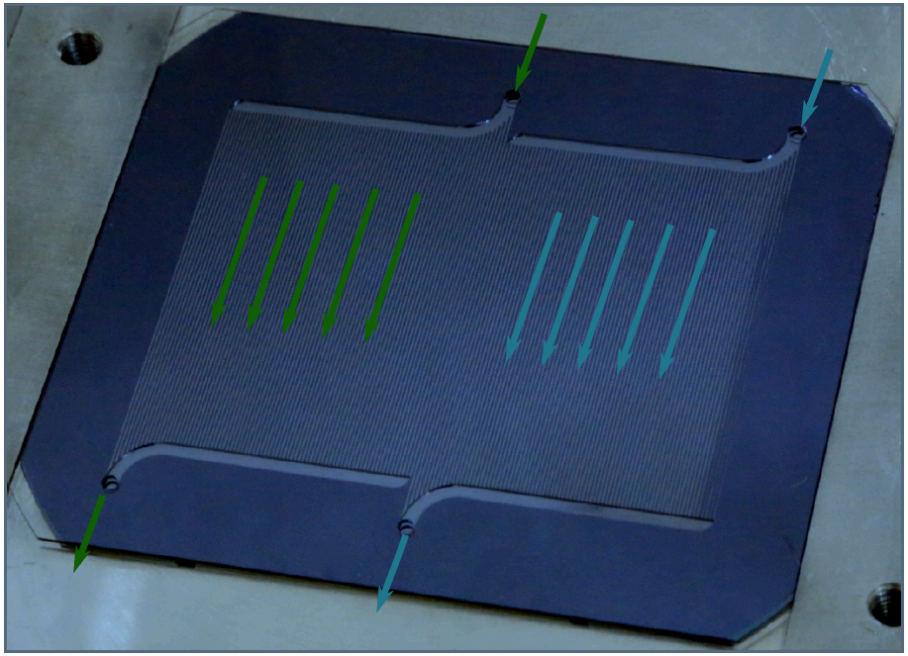
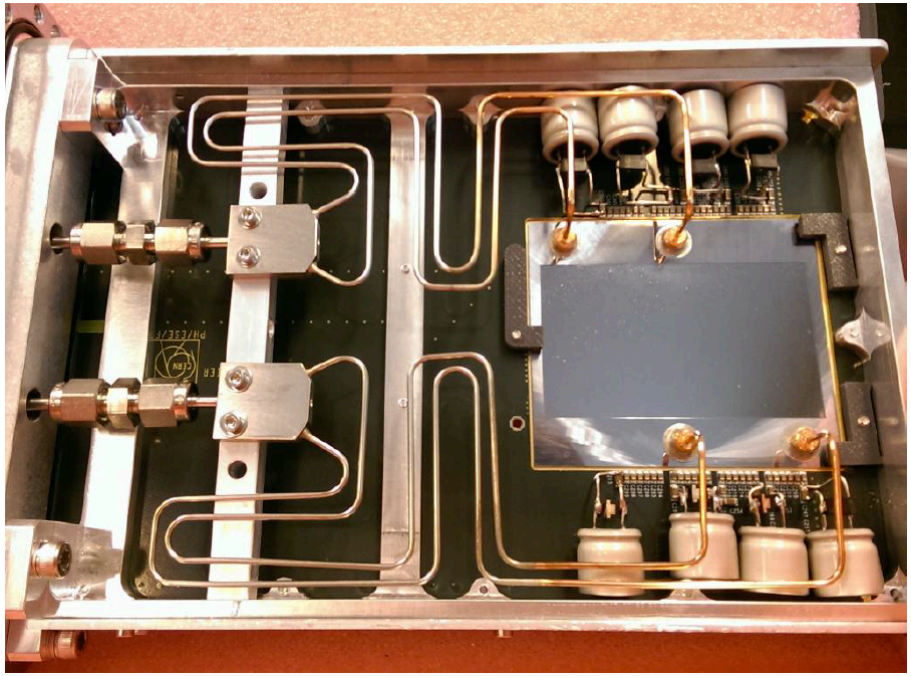


Micro-channel cooling

- Fabricated by CEA Leti
- 200μm × 70μm channels
- Two cooling circuits
- Fluid brought in with capillaries
- Kovar connectors soldered onto cooling plate



Micro-channel cooling

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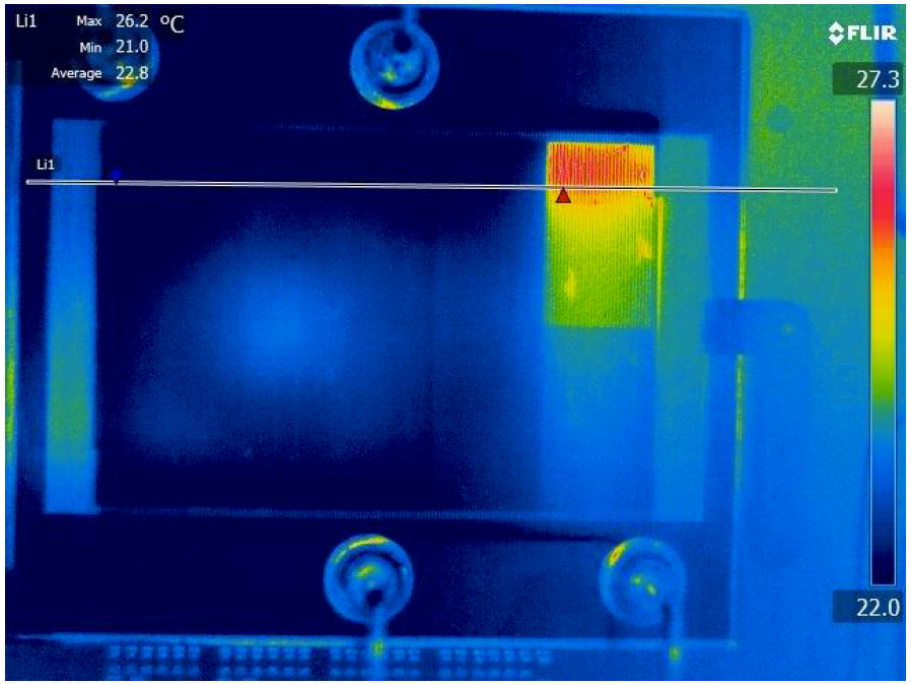
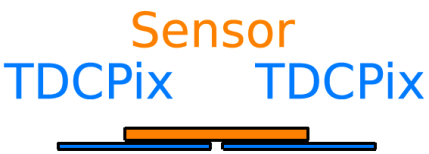
- Kovar connectors soldered onto cooling plate
- Infra-red picture



Electro/mechanical integration

- Detector glued on 150 μm (210 μm) cooling plate



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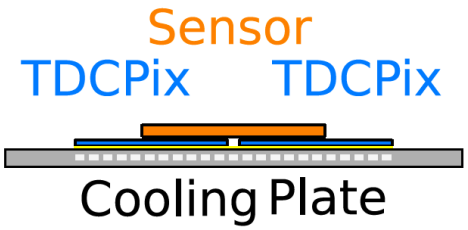
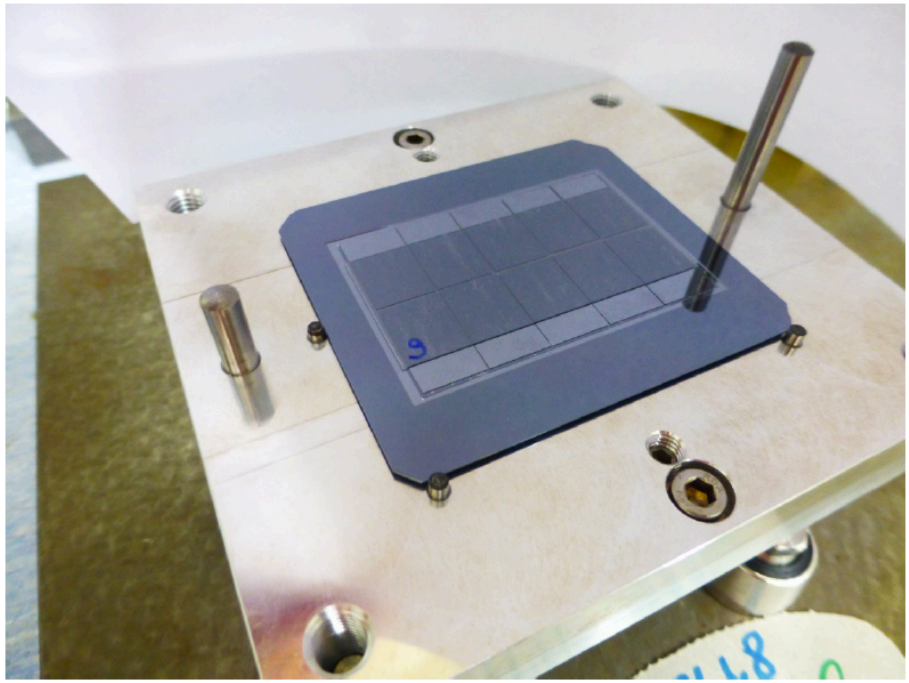
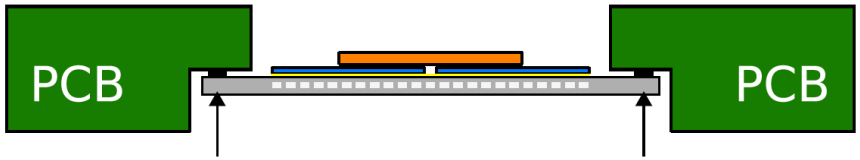




Electro/mechanical integration

- Detector glued on 150 μm (210 μm) cooling plate
- Cooling plate clamped on PCB, then TDCPix wired bonded to PCB (14 layers)
  - Serving power, clock, config. and receiving data
  - 40 differential 3.2 Gb/s signals over 30 cm
  - 73 μm bonding pitch on chip



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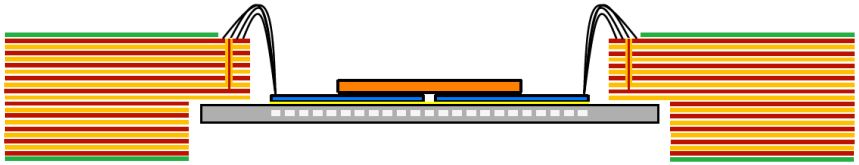

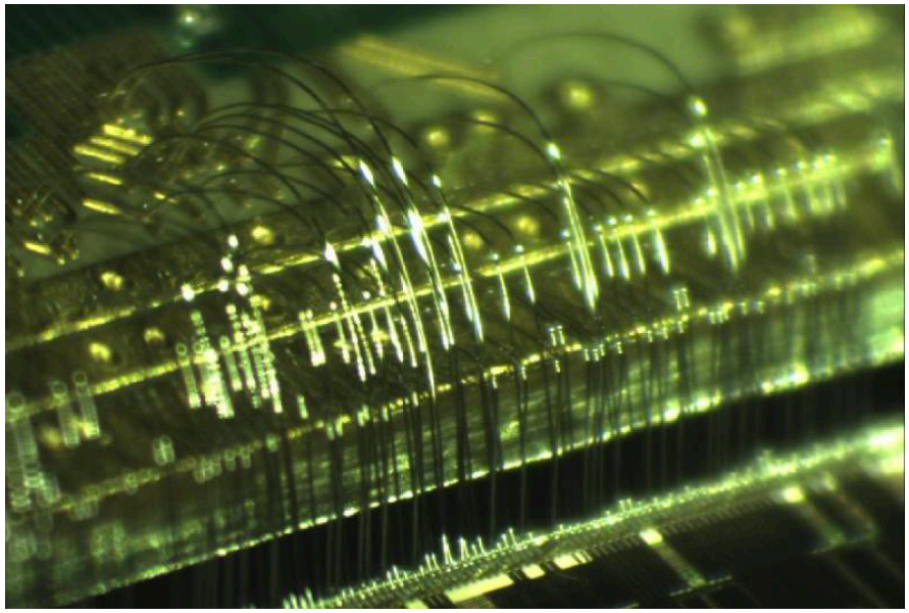

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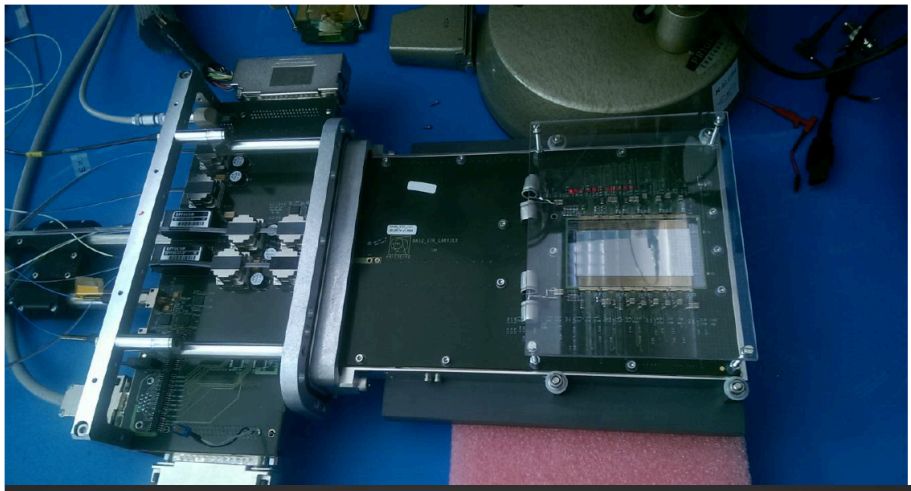
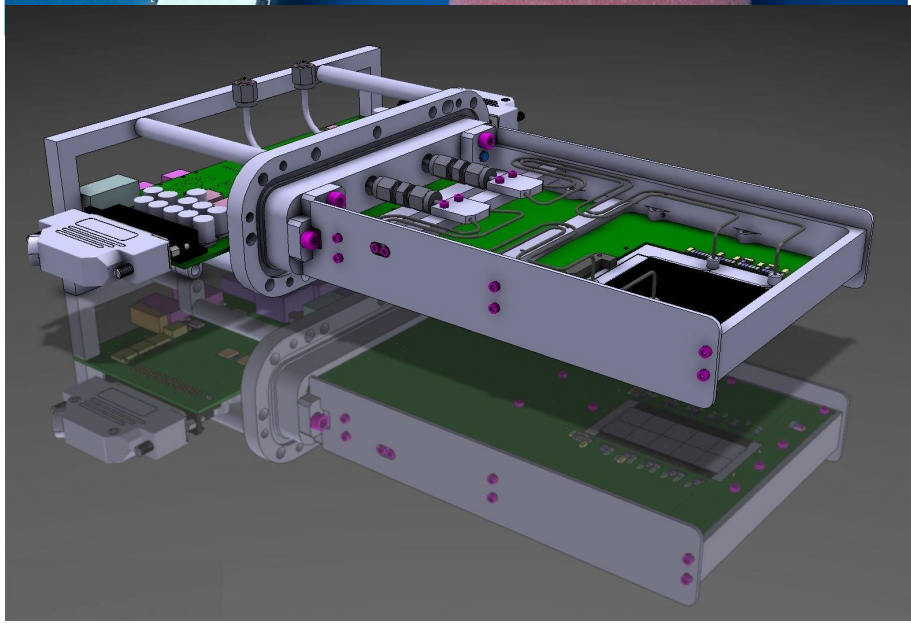
- PCB glued on frame + flange





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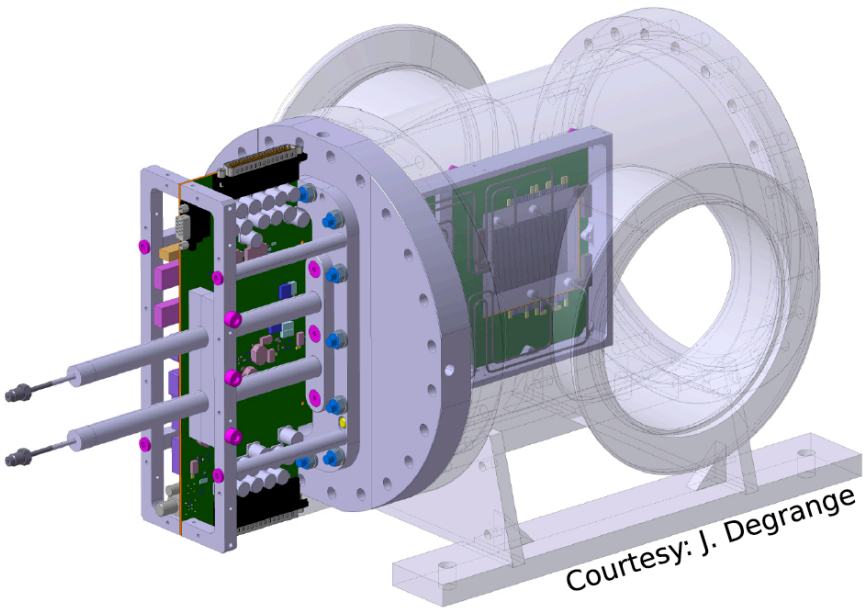
  - Serving power, clock, config. and receiving data
  - 40 differential 3.2 Gb/s signals over 30 cm
  - 73 μm bonding pitch on chip
- PCB glued on frame + flange
- Flange closes the vacuum
- Easy access for interventions

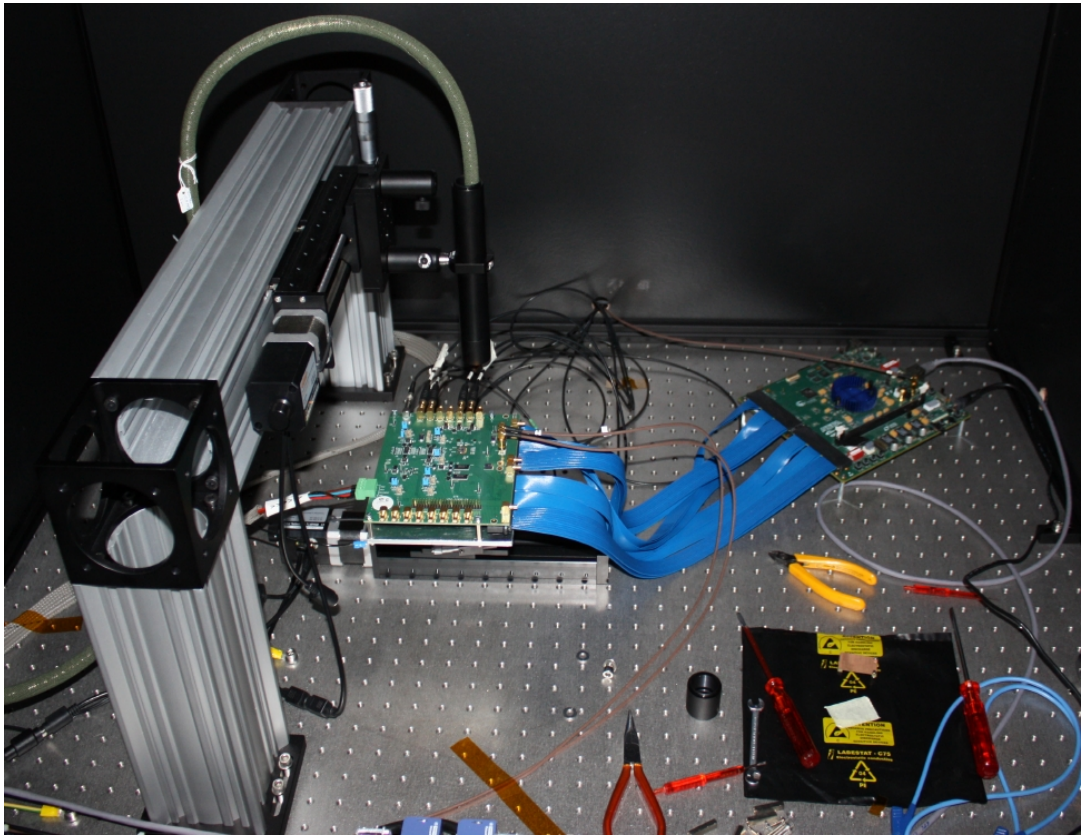


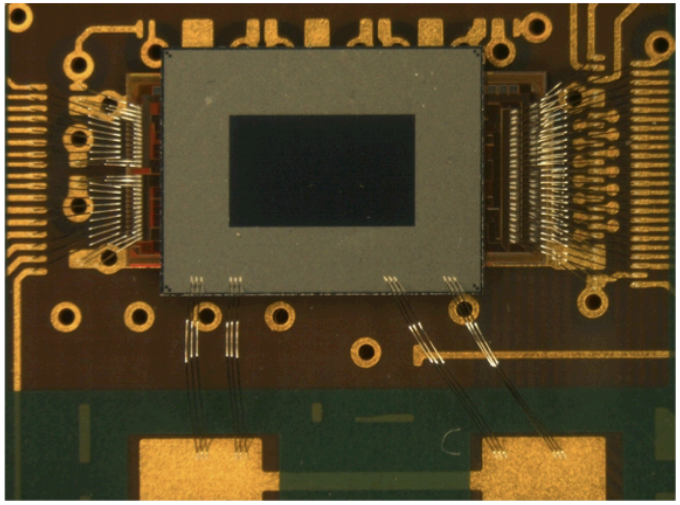
GTK back-end Read-Out

- TDCpix sends out every hit: trigger matching needed
- GTK-RO built using FPGA (Altera Stratix GX110)
- Each GTK-RO made of two decked cards: daughter card handles interface with TTC
- Each TDCpix is connected to one GTK-RO through 4 optical links (one per 3.2 Gb/s serializer) plus 1 configuration link
  - Trigger matching efficiency measured splitting optical signal and reading trigger-less data concurrently (on few boards)
- GTK-RO board must:
  - Buffer data, waiting for level-0 trigger decision (maximum level-0 trigger latency is 1 ms)
  - Retrieve data in a 75 ns time window upon trigger request
  - Send data to the subdetector PC

Laser test setup

- IR light (1060 nm) to create charge carriers through silicon bulk
- Characterize GTK bump-bonded assemblies on laboratory bench

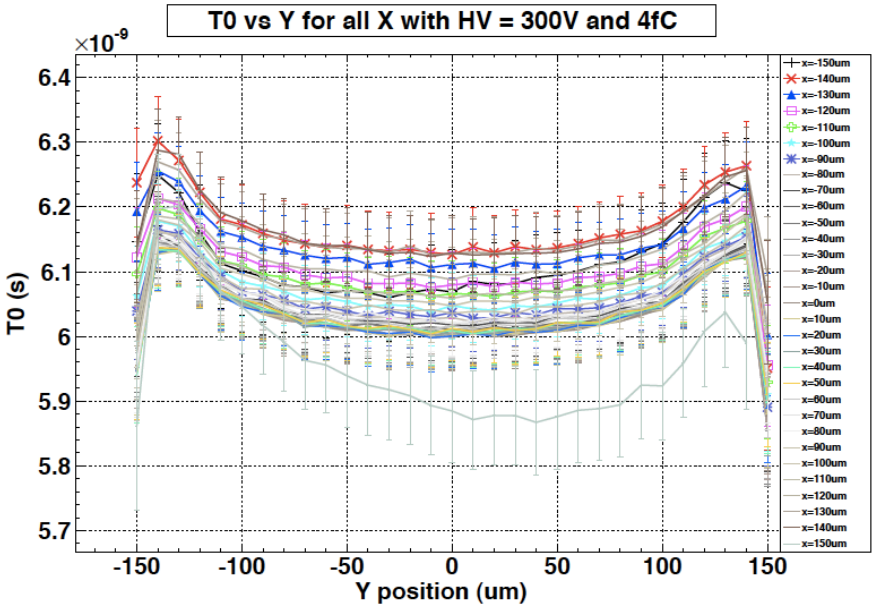


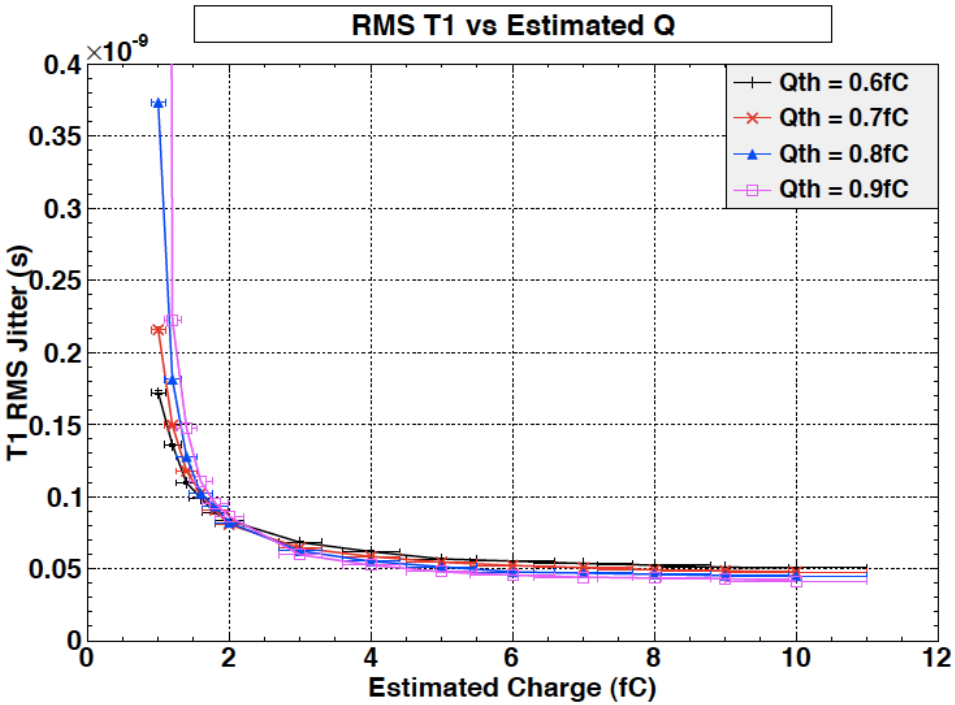


- 5 ps time precision
- Absolute calibration of injected charge
  - Radioactive sources (^{241}Am, ^{109}Cd)

Results from laser tests

- Time resolution of ~75 ps at 3 fC (average charge created by minimum ionizing particle)
  - Charge injected at the pixel center

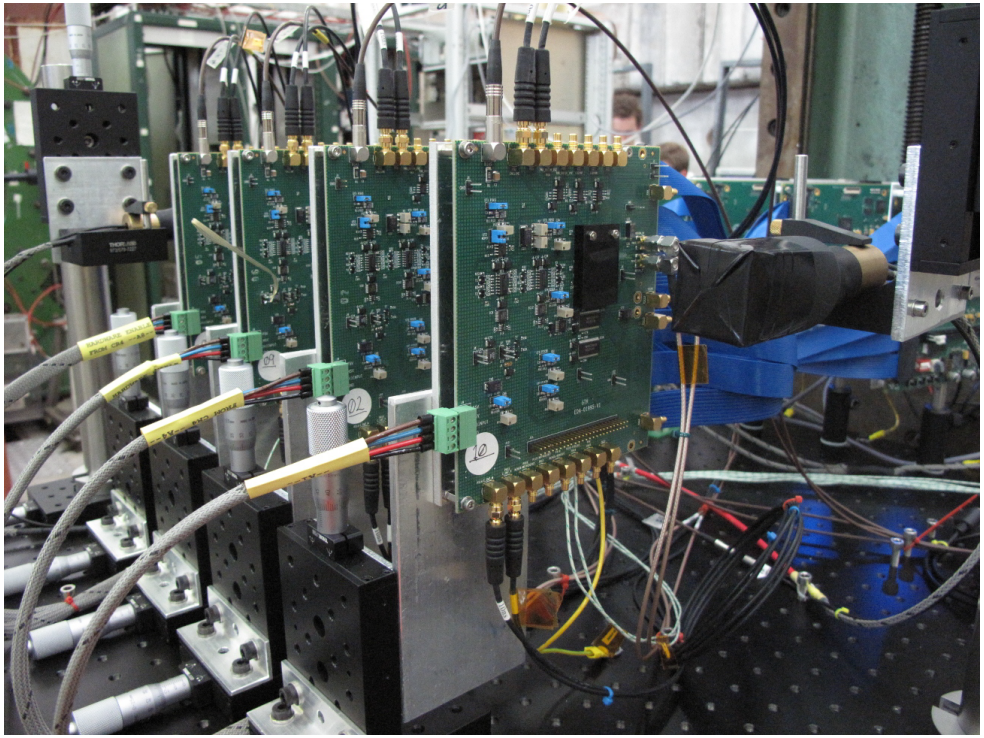




- X-Y position scan of pixel matrix
  - Variation of measured time with impact position inside pixel
  - Geometrical effect (weighting field)

Test-beam at CERN

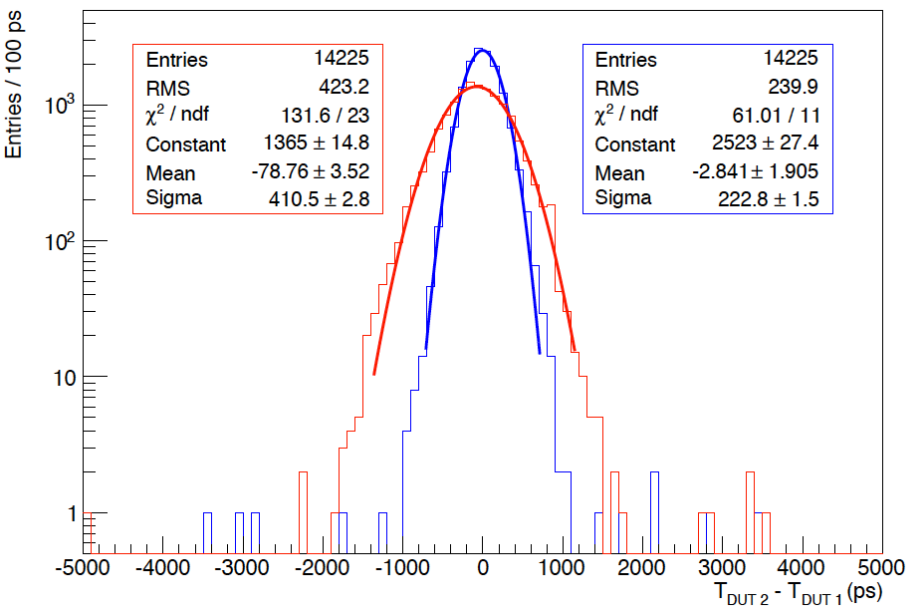
- Test-beam at the T9 beam-line (CERN PS East Hall)
  - 10 GeV/c π^+ and p
- 4 consecutive **prototype** detector planes
- Fast scintillators used for timing reference
  - Synchronized 25 ps TDC independent read-out

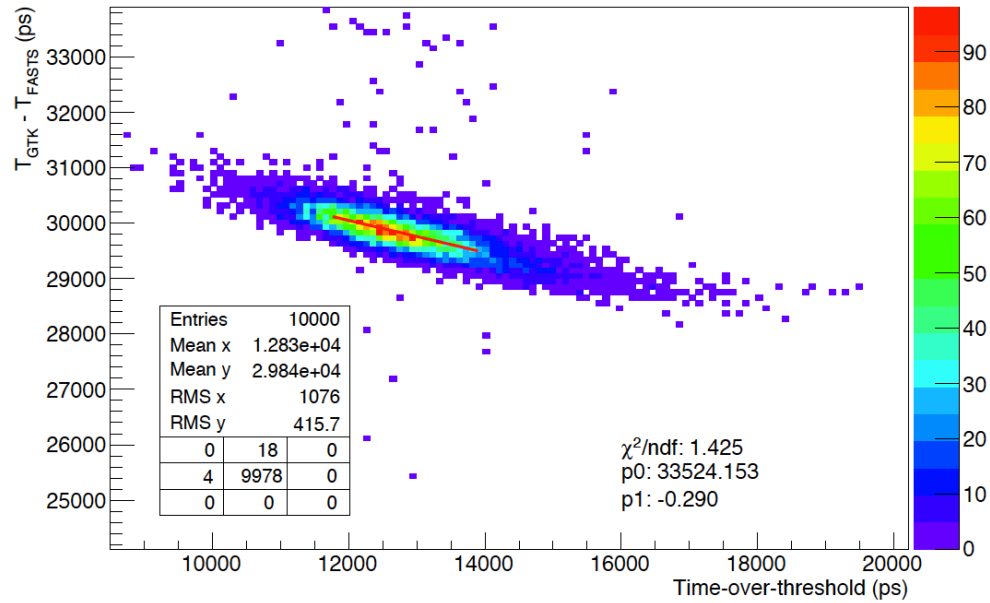


- Very precise mechanical supports and pre-alignment at the 150 μm level
- Operation in air (no cooling, no dry air circulation)
- Results published on JINST 10 P12016 (2015)

Time-walk correction

- Time-walk correction evaluated using fast scintillators for time reference and time-over-threshold information
  - Pol fit or look-up table

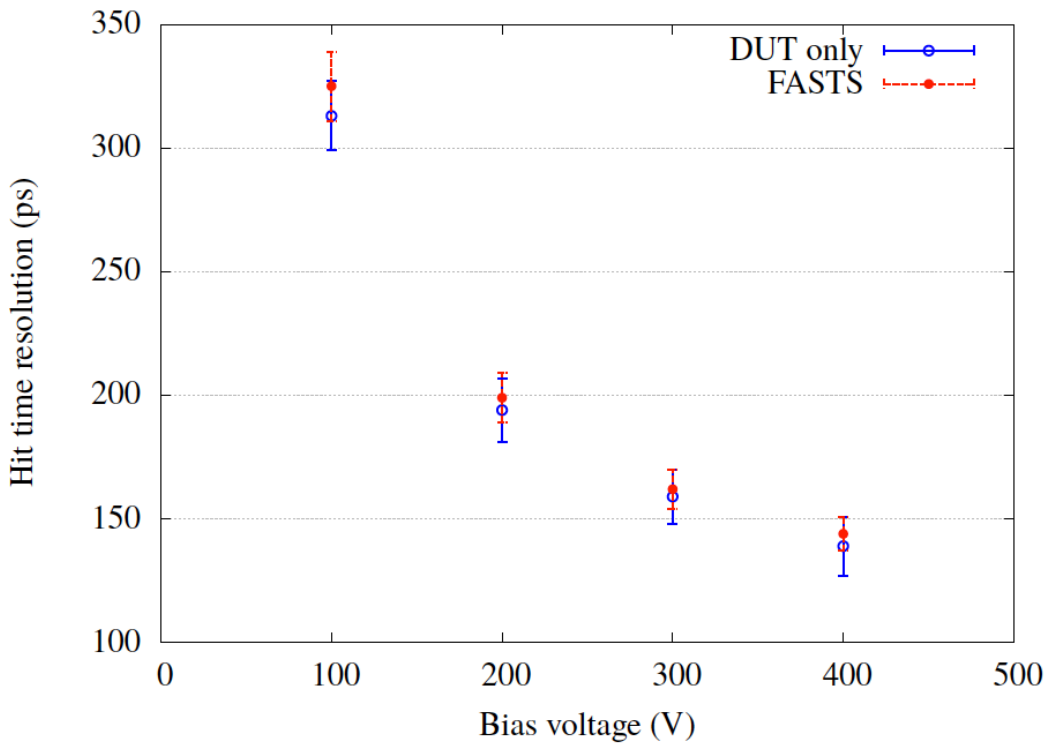




- Discriminator thresholds set by unique digital-to-analog converter for all pixels
  - (0.70±0.14) fC
- Time resolution after correction is ~160 ps (for 300 V bias)

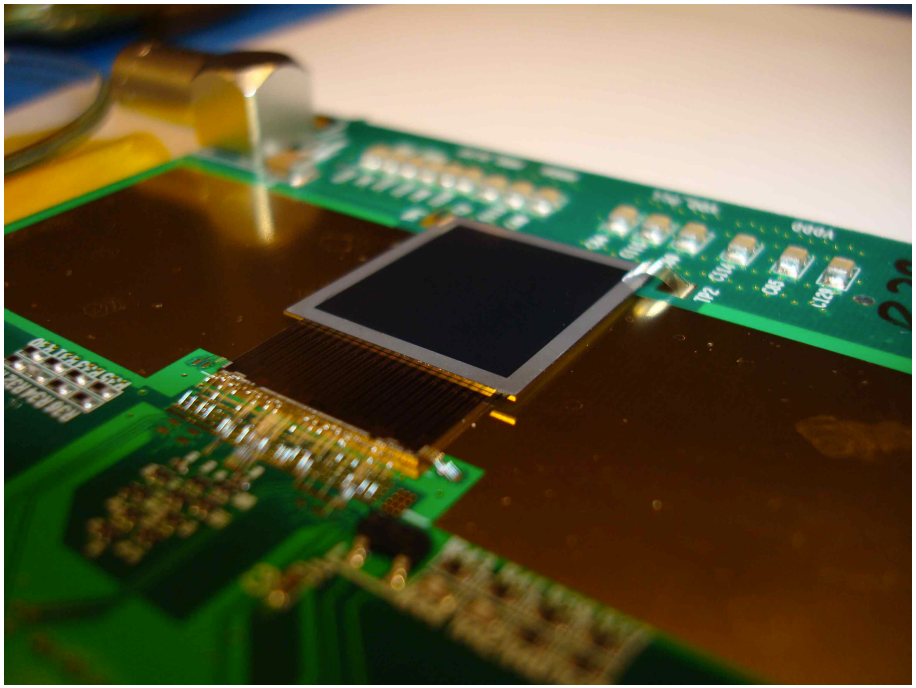
Bias voltage variation

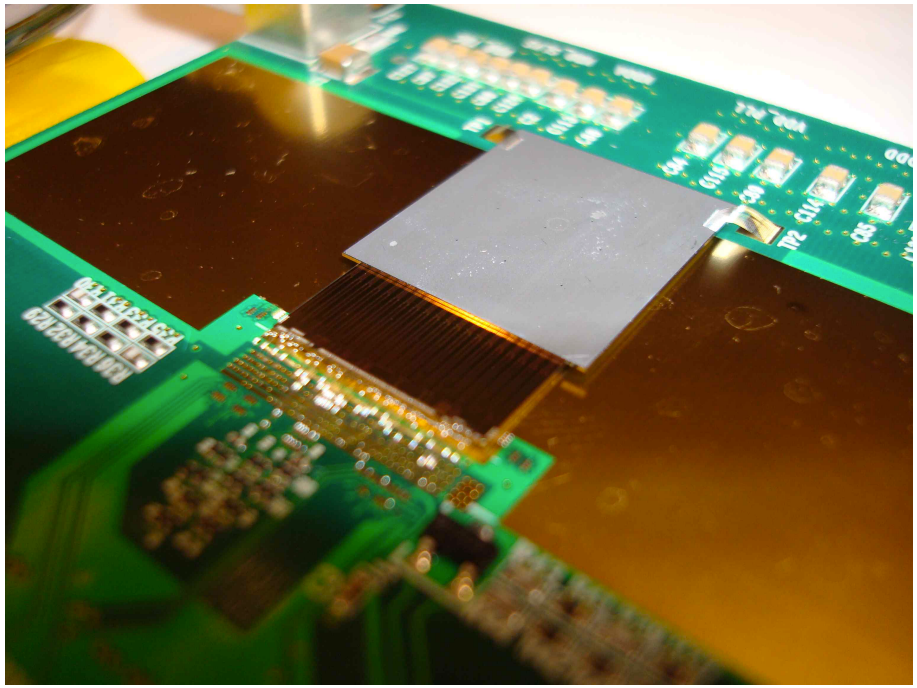
- Time resolution measured as a function of bias on **prototype detector**
- Better than **150 ps** at 400 V
  - Still room for improvement at higher voltages



TDCpix assemblies

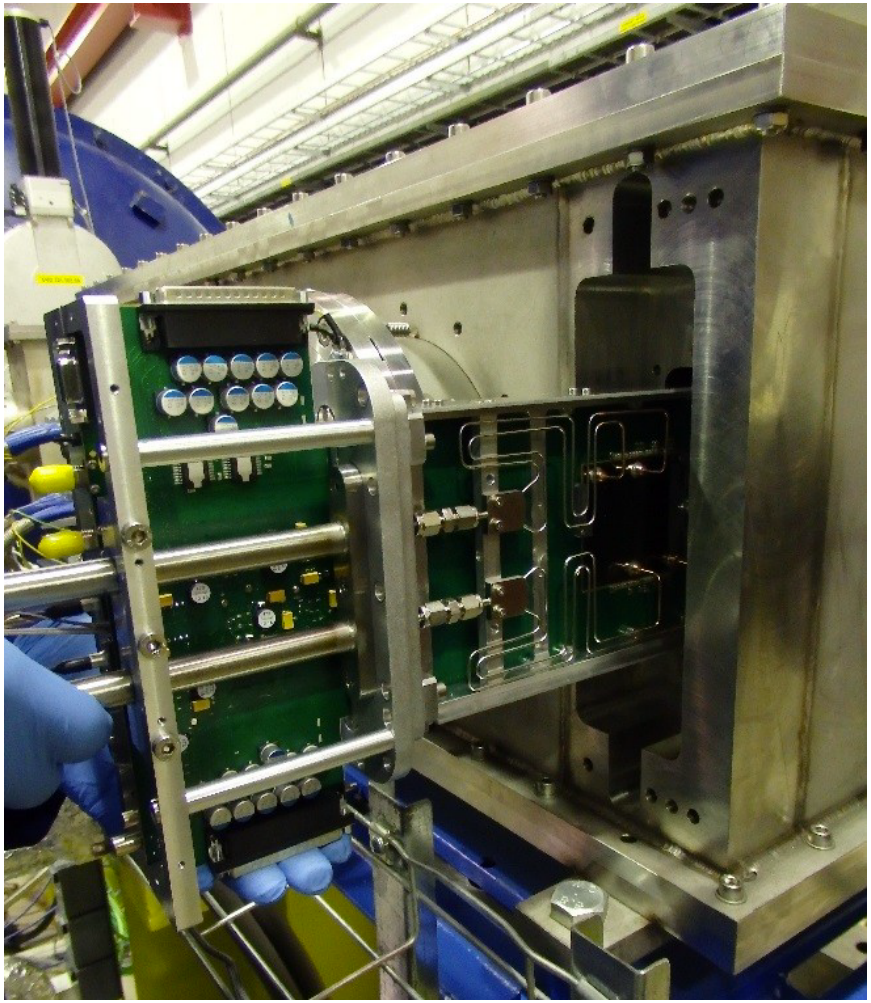
- Bump-bonded assemblies with final TDCpix ASIC
  - Full assemblies (1 large sensor + 10 read-out chips)
  - Single-chip assemblies opened and closed back-side metallization
    - For lab bench and laser tests



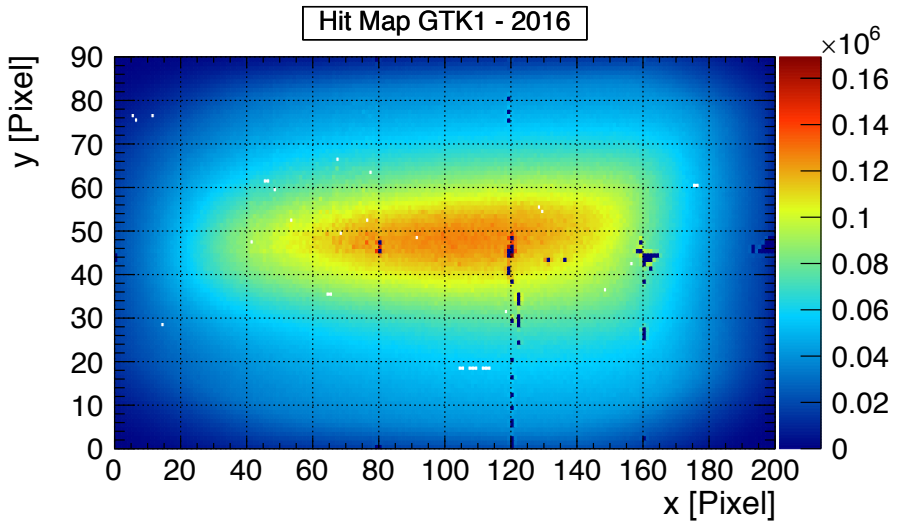


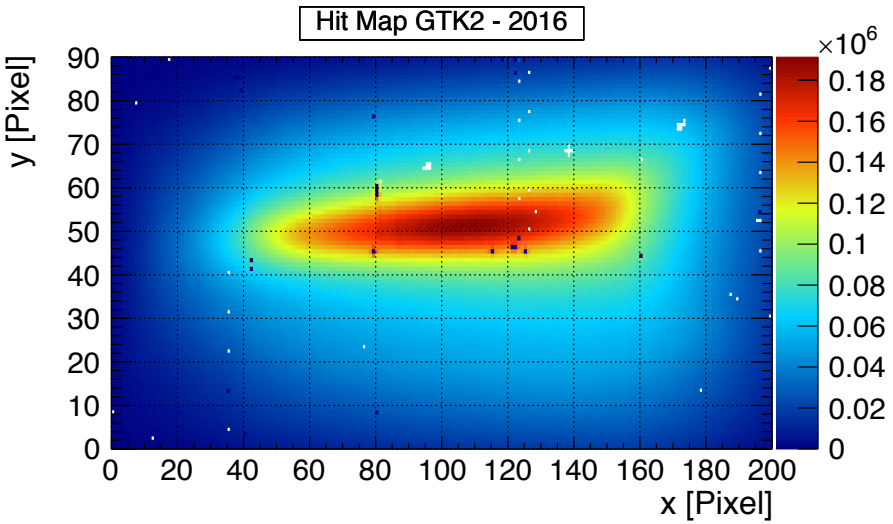
Installation in NA62 beamline

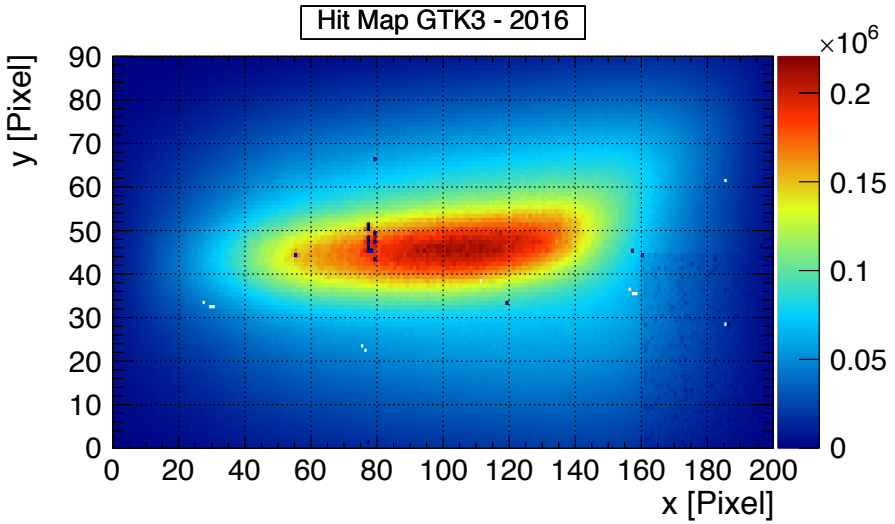
- All stations and infrastructure installed in 2014/2015
- Beam line commissioned up to nominal intensity
- Sub-detectors and trigger/DAQ up to 20% nominal intensity
- Gigatracker commissioned in 2014/2015
  - GTK cooled at 0 to -10 °C
  - Thresholds set to 0.7 fC
  - Bias voltage set to 100-300 V depending on running periods



Hit maps

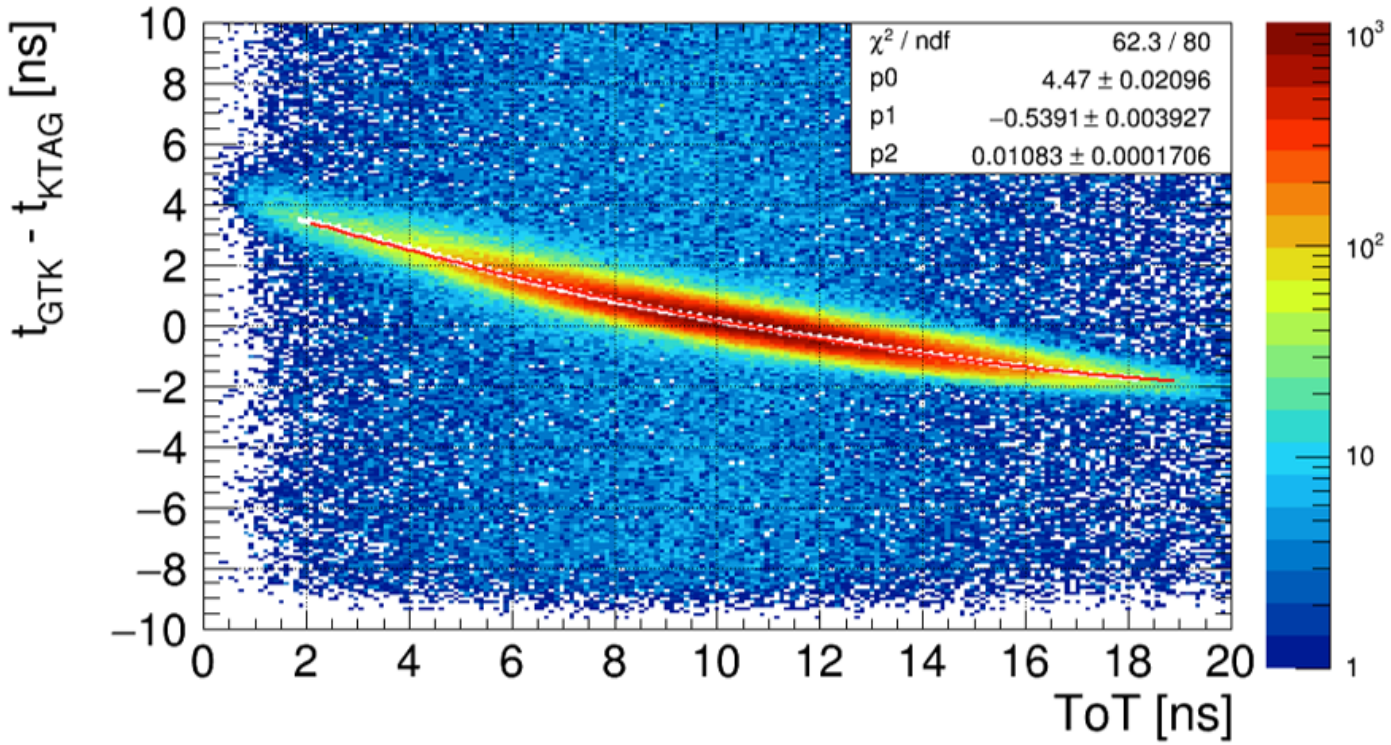

Hit Map GTK1 - 2016
y [Pixel]
x [Pixel]
×10^6
0.16
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0


Hit Map GTK2 - 2016
y [Pixel]
x [Pixel]
×10^6
0.18
0.16
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0


Hit Map GTK3 - 2016
y [Pixel]
x [Pixel]
×10^6
0.2
0.15
0.1
0.05
0

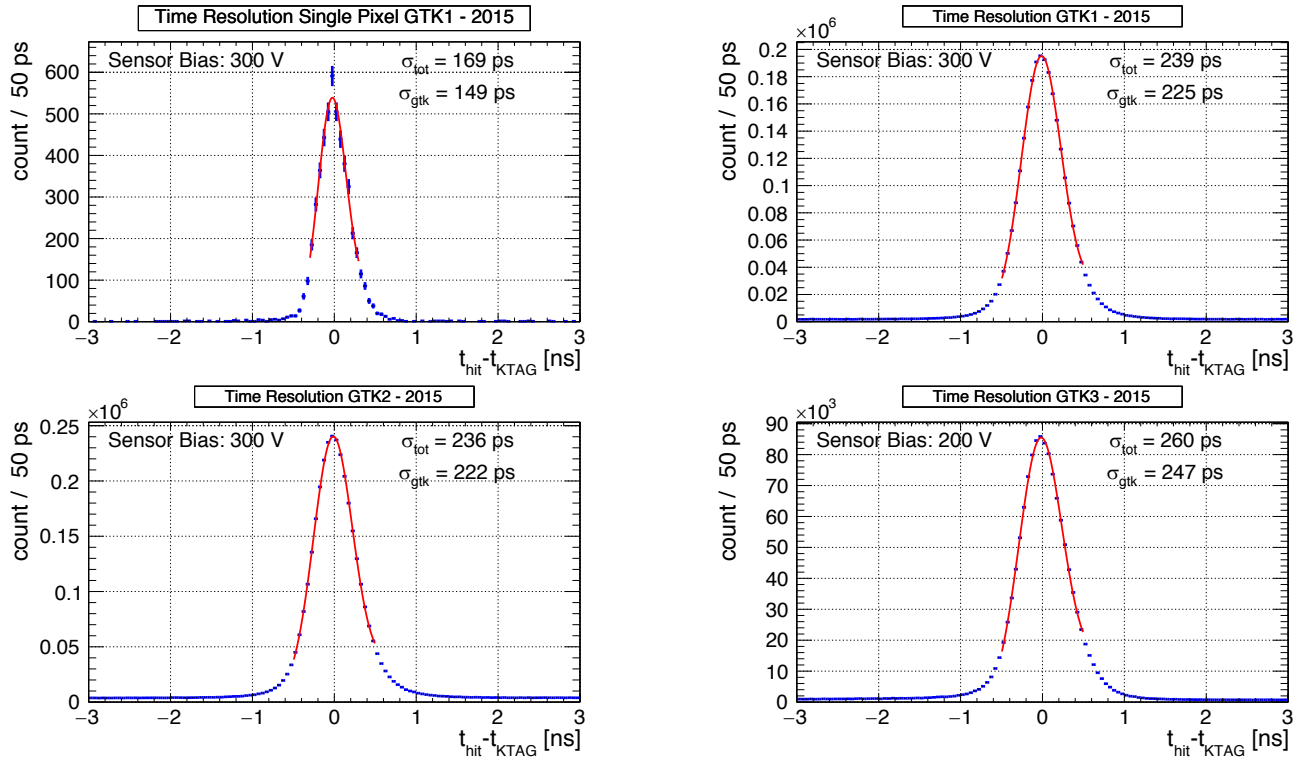
Time resolution (1)

- Preliminary results from 2015 data
  - Paper on NA62 detector and beam line performance is under preparation
- Time walk correction using KTAG as timing reference



Time resolution (2)

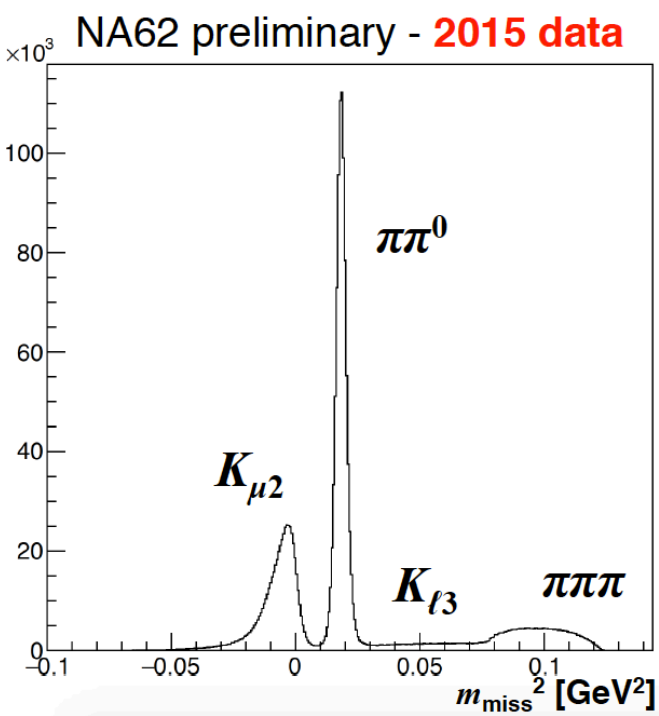
- Time resolution measured using 2015 data
  - 300 V bias except for GTK3 (200 V)

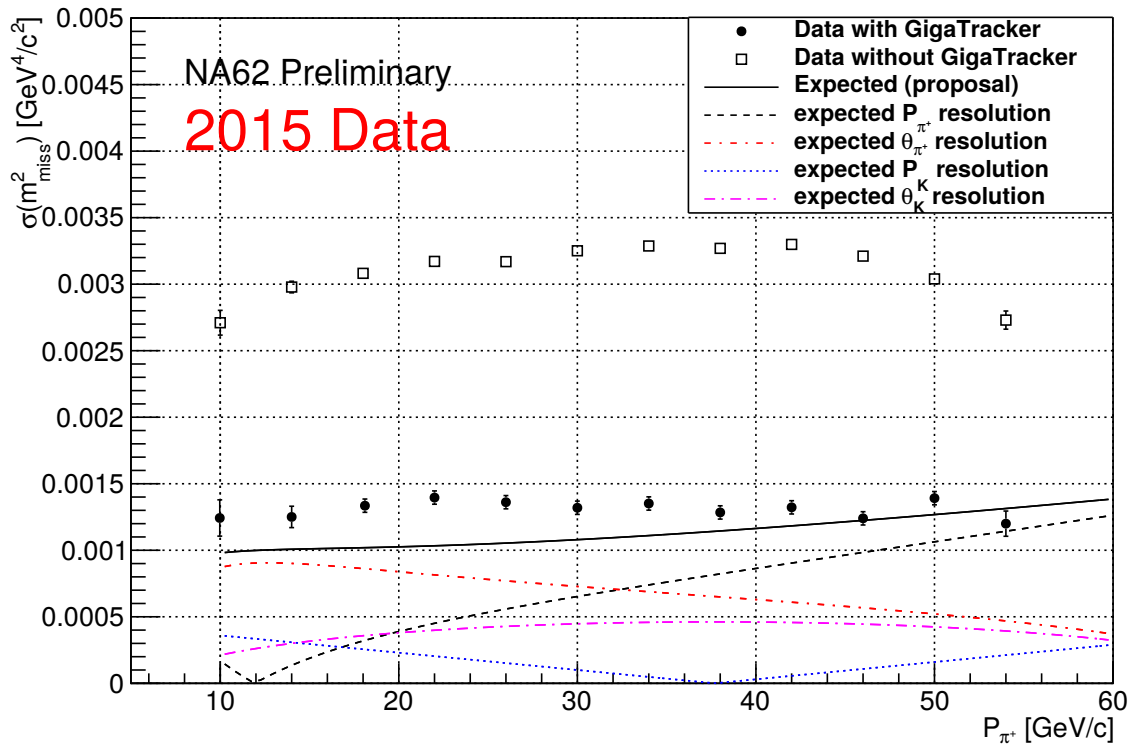


- Further calibrations and data analysis needed to exploit the full potential of the detector

m_{miss}^2 resolution

- Important contribution of the Gigatracker to improve missing mass resolution
  - Preliminary results from 2015 low intensity data





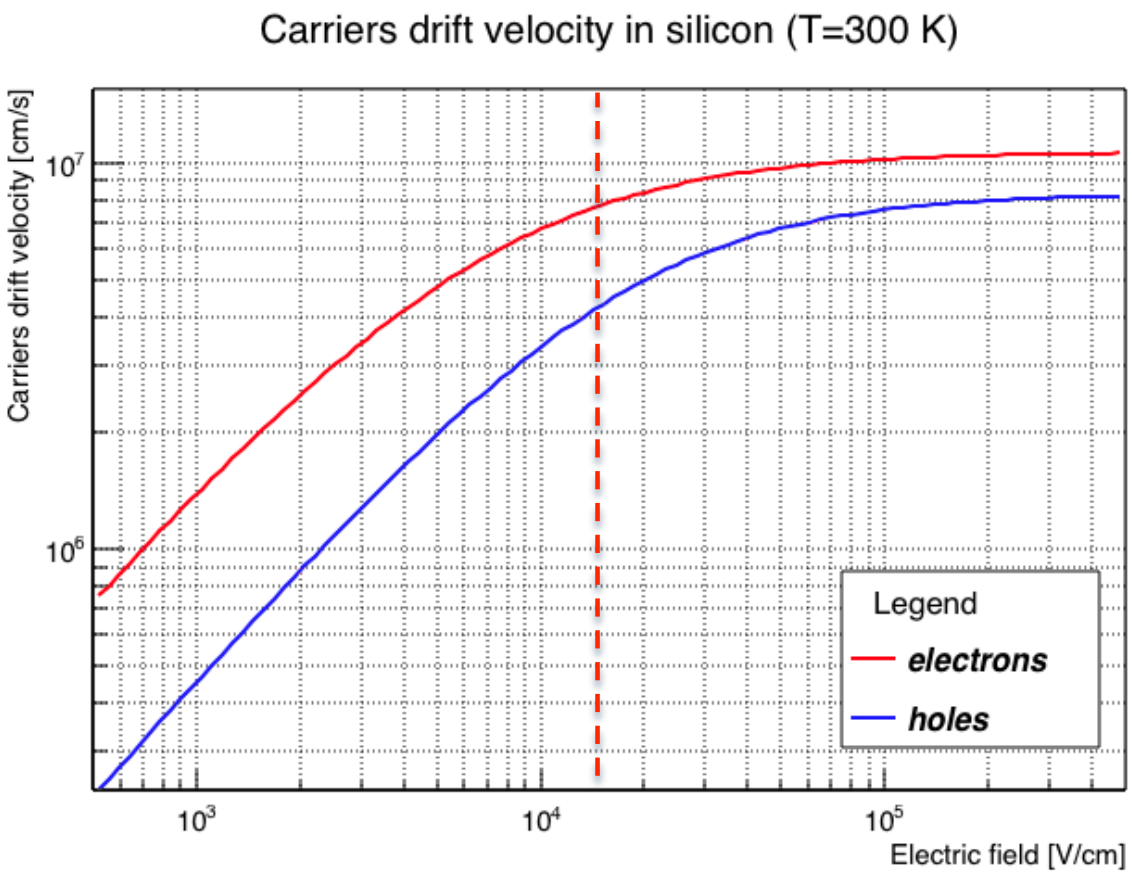
Conclusions

- The Gigatracker detector is essential to measure BR($K^+ \rightarrow \pi^+ \nu\bar{\nu}$) at NA62
- Detector fully commissioned
- Excellent timing performance measured on thin hybrid pixel detectors (200 μm planar sensors) with a very high density of channels (18000 per sensor) in vacuum
  - High over-depletion necessary
- Innovative and very-low mass cooling plate based on micro-channels
  - First implementation in HEP experiment
- Analysis of full 2015 and 2016 data sets is on-going
  - Monitoring radiation damage effects on performance

SPARES

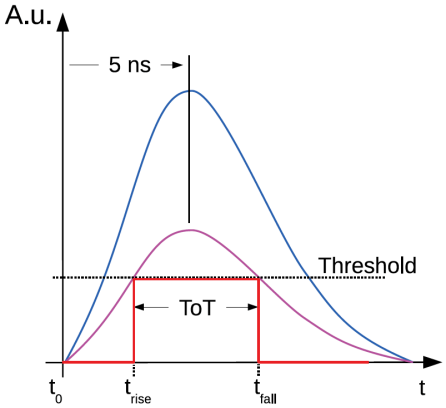
Carriers drift velocity

- In "nominal" conditions we apply 300 V over 200 μm
- Electric field 1.5×10^4 V/cm
- Close to saturation but still room for improvement



Timing detector

- In timing measurements the slope-to-noise ratio has to be optimized rather than the signal-to noise ratio alone
  - Very low r.m.s. noise σ_n
  - Very steep signal at threshold level $(dV/dt)_{thr}$
- Time resolution is given by the ratio: $\sigma_t = \dfrac{\sigma_n}{(dV/dt)_{thr}}$
- Many contributing factors to consider:
  - Need large signals, and fast "signal collection"
  - Reduce input capacitance, match amplifier bandwidth
  - Electric (weighting) field uniformity
  - Energy release (total, straggling, direction)
  - Time-walk correction
  - Digitization (e.g. TDC bin size and linearity)
  - …



Time-walk correction

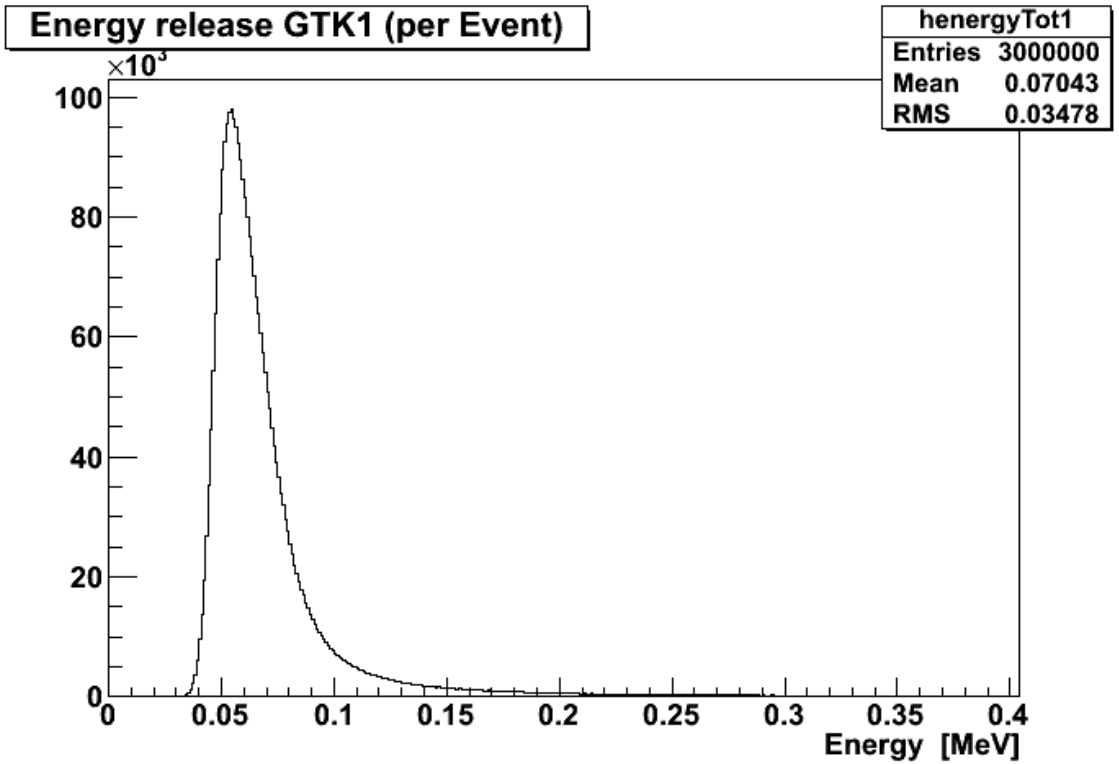
- To achieve excellent timing accuracy, a careful time-walk compensation has to be applied:

Some alternatives:

- Single threshold discriminator and Time over Threshold
  - Time-walk correction algorithm based on the signal time over threshold (pulse width), obtained by measuring leading and trailing edges of the pulse
  - Accurate calibration needed to define correction algorithm
- Use of a Constant Fraction Discriminator (CFD)
  - Analog signal processing technique of time information
  - Single time measurement, complicated analog design
- Digitizer
- Multiple thresholds discriminator

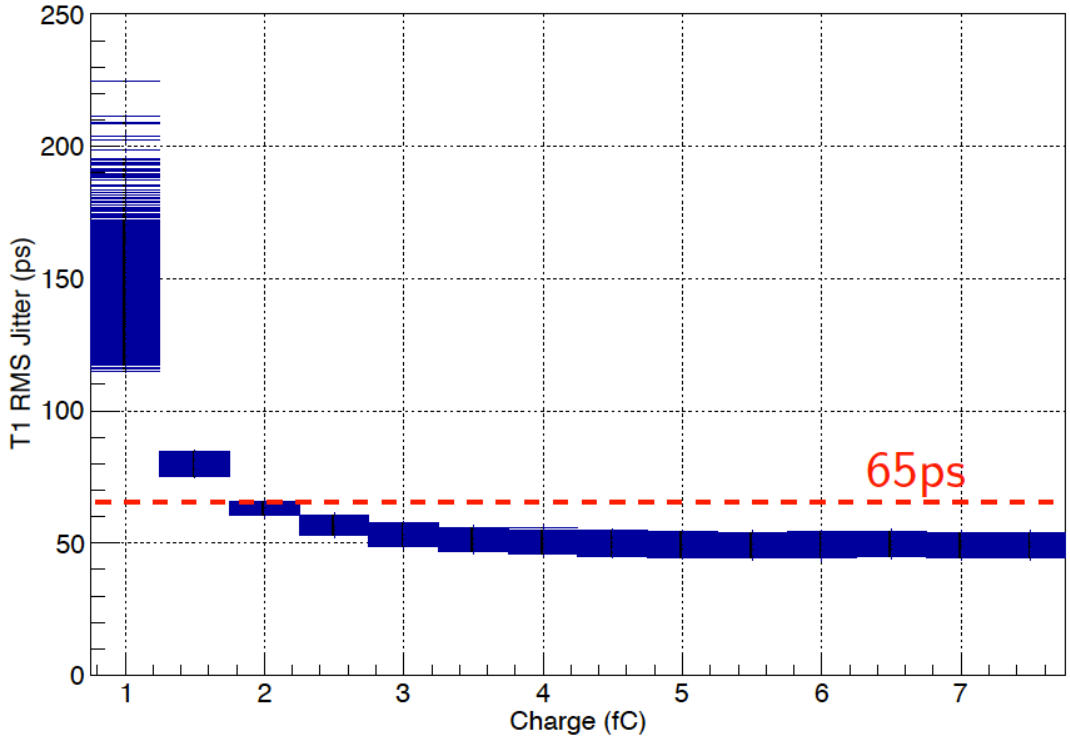
Sensor signal

- Simulation of energy deposited in 200 μm silicon
  - GEANT4
- Most probable energy: 54 keV
  - 15 k e^-h, 2.4 fC
- Mean energy: 72 keV
  - 20 k e^-h, 3.2 fC



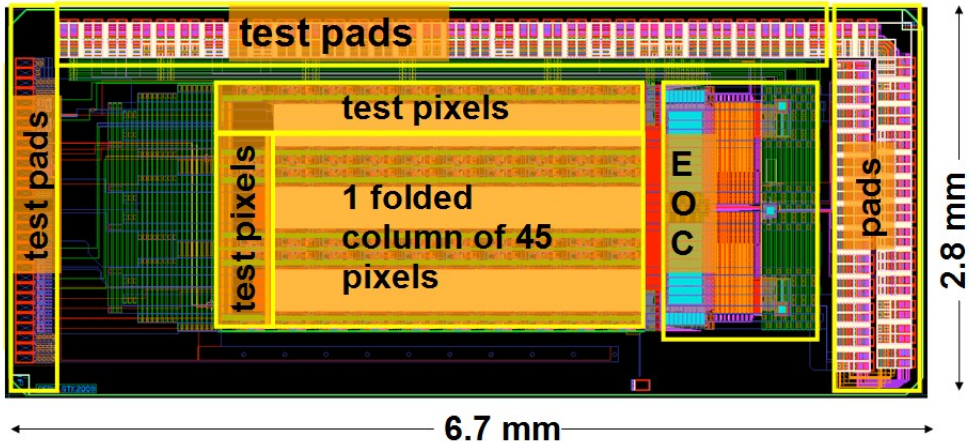
TDCpix full-chain resolution

- Complete electrical characterization of the full-chain (pixel → TDC → output)
  - Scan over the full clock period for each charge
  - Resolution better than 65 ps at 2 fC

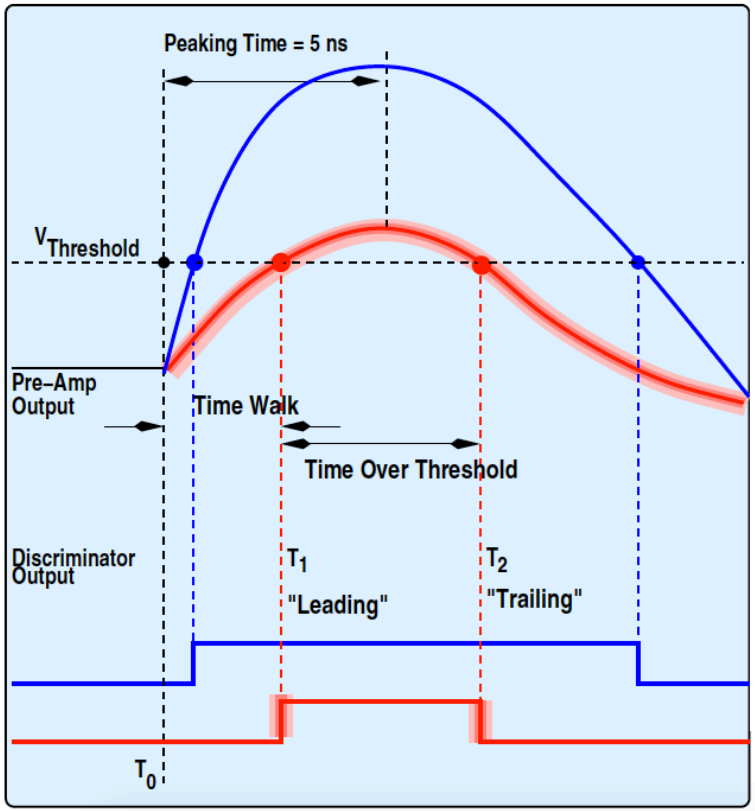


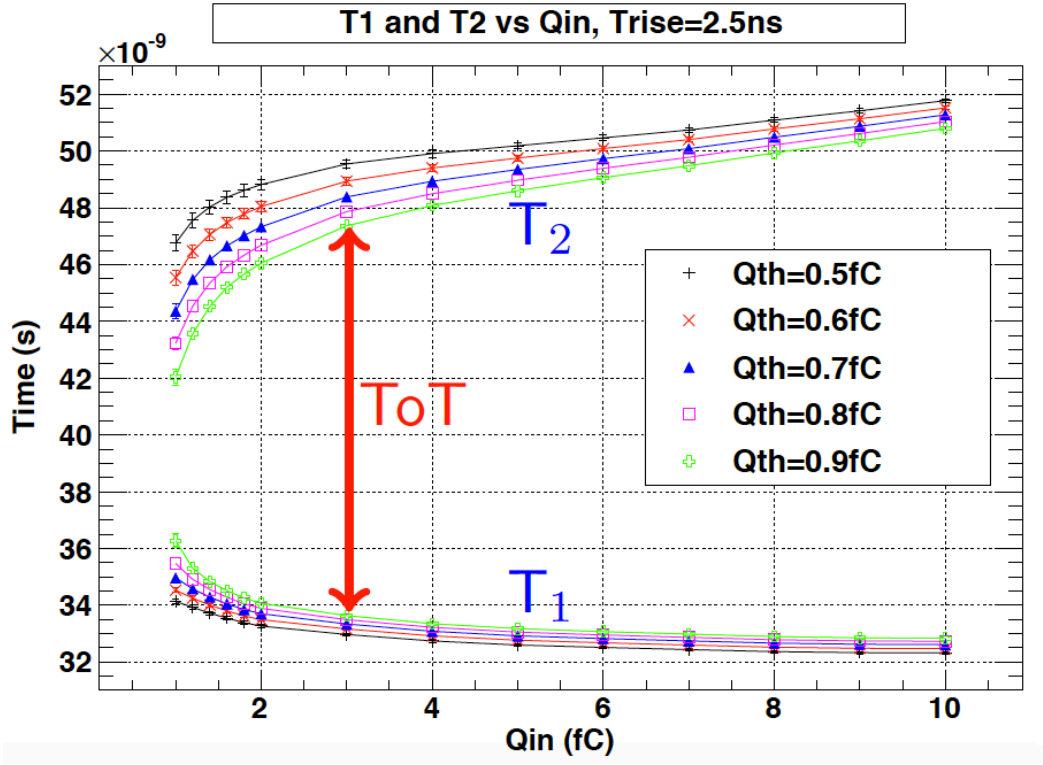
Prototype read-out ASIC

- IBM 130 nm, 2.8 mm × 6.7 mm total size
- 320 MHz reference clock
- 60 pixels divided into 3 groups
  - 45 pixels with 9 read-out blocks, each one serving the 5 pixels through the "hit arbiter" block
  - Small array: 9 pixels
  - Test column: 6 pixels with analog output
- Extensively characterized with electrical tests, laser and particle beams



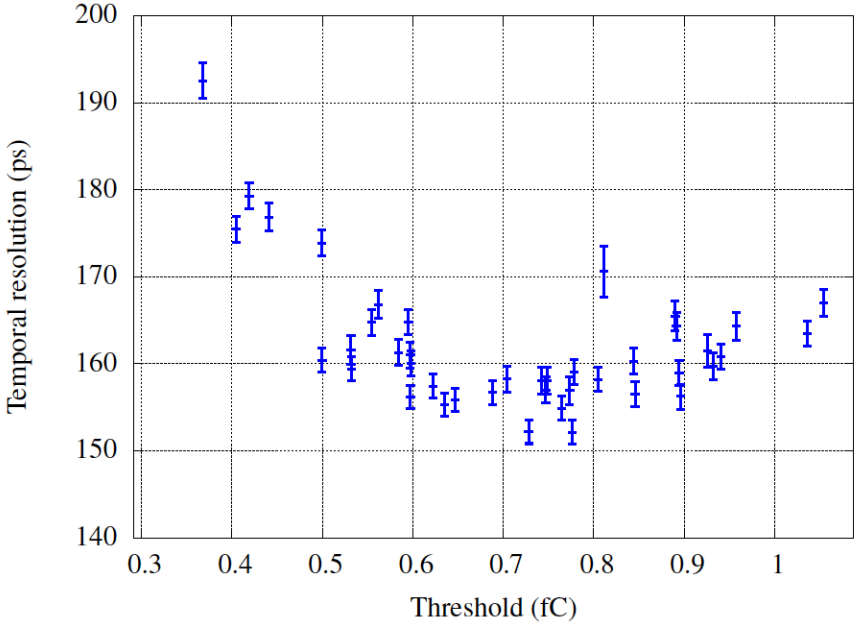
Time walk effect

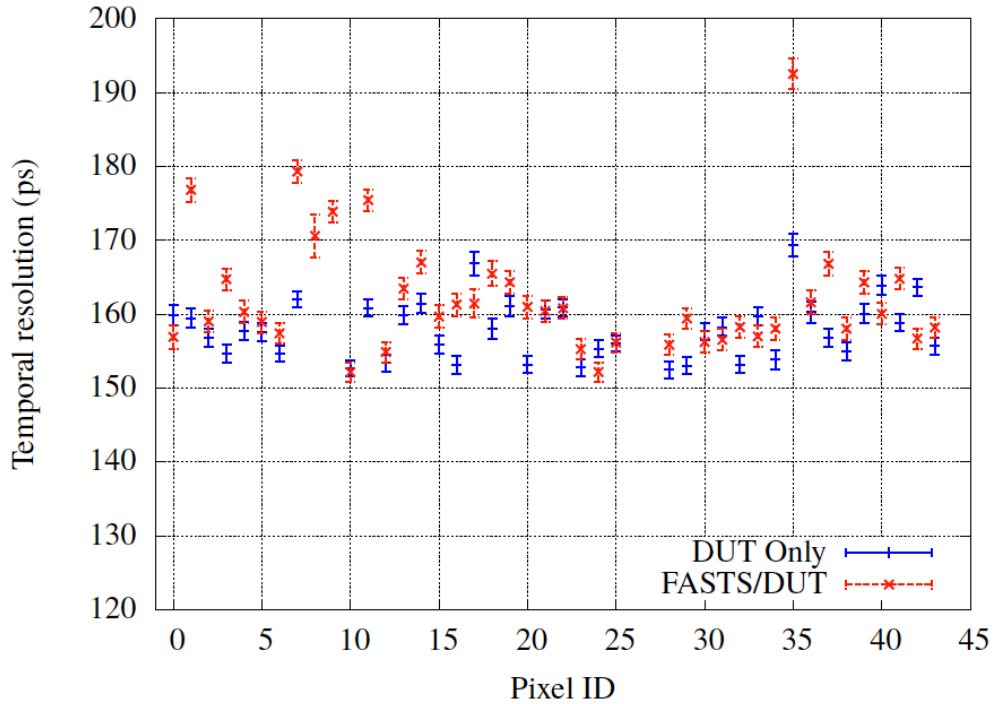




Prototype time resolution

- Time resolution measured for all 45 pixels per chip
  - Shown for 300 V bias
  - Variations mainly due to pixel-by-pixel threshold variation

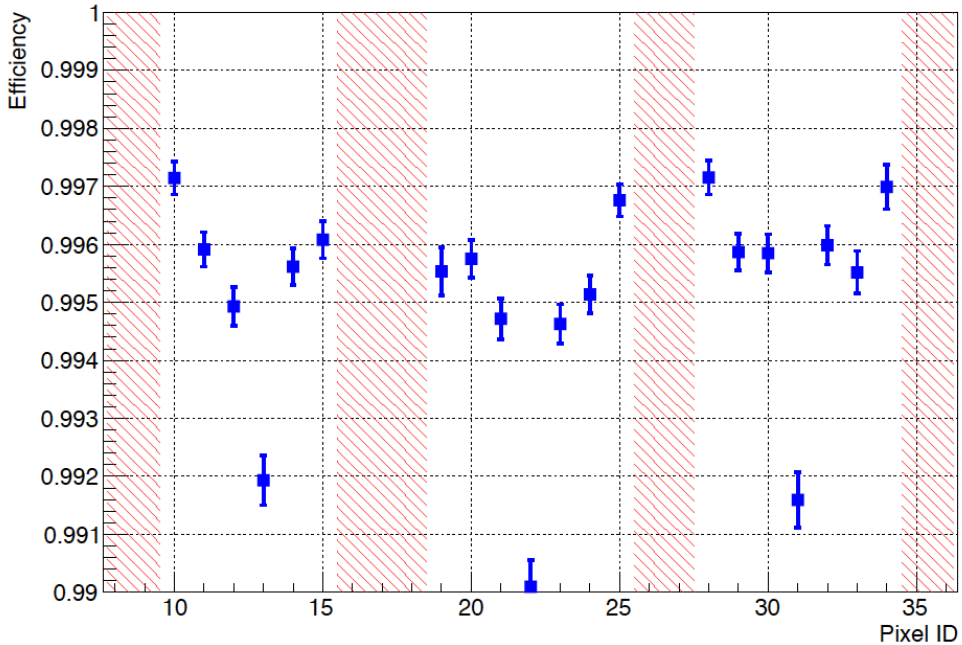




- Clear threshold dependence
  - Worse resolution for small threshold values (smaller signal slope)

Prototype efficiency

- Track fitting and extrapolated track impact position to the target detector calculated
- Very high efficiency (>99%)
  - Pixels in the outer region and dead pixels have been excluded (red hatched area)



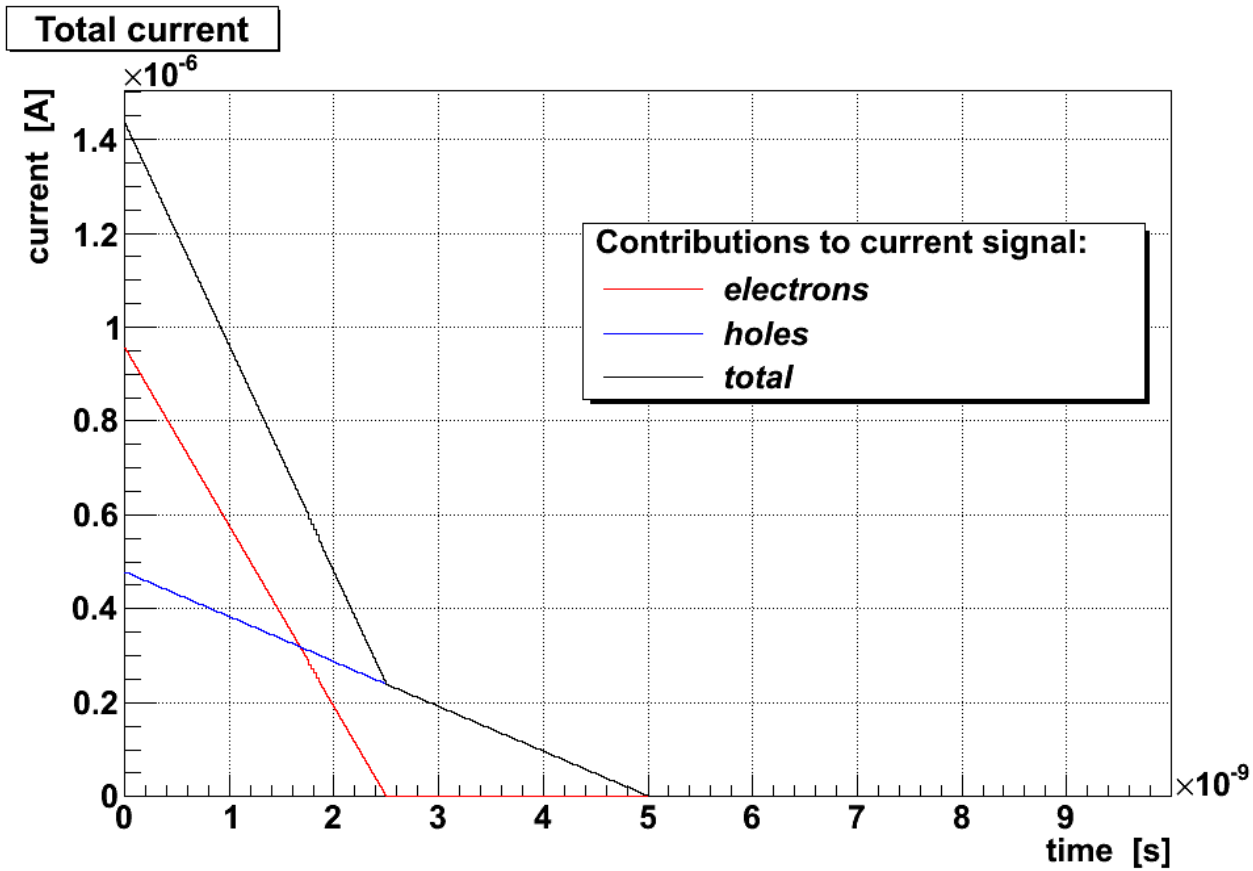
Contributions to σ_{time}

- Electronic noise from front-end chip
  - Measured ~210 e^- (ENC) with sensor
- Sensor bias voltage and threshold
  - Variation of charge collection time (signal slope at the discriminator threshold)
- Impact position on pixel sensor
  - Weighting field variation (geometrical effect)
- Total energy release
  - Variation of total energy released in sensor according to Landau/Vavilov distributions
- Energy straggling in the sensor bulk
  - Non-uniform energy release along track and delta rays

Sensor: signal formation

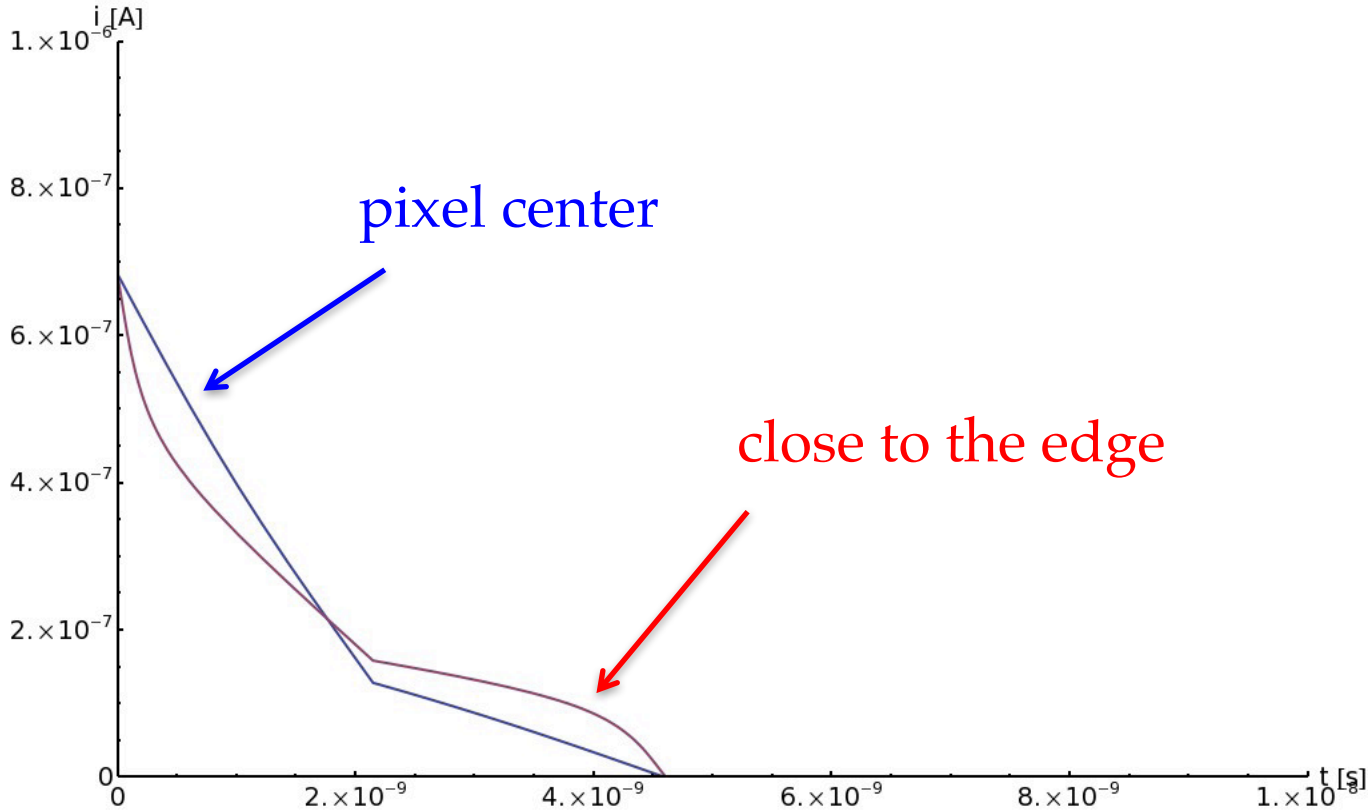
- Ramo-Shockley theorem
  - $i = q\,\mathbf{v} \bullet \mathbf{E_w}$

- Example: uniform release of 2.4 fC (MPV) along a 200 μm thick planar sensor
  - Assuming uniform weighting field



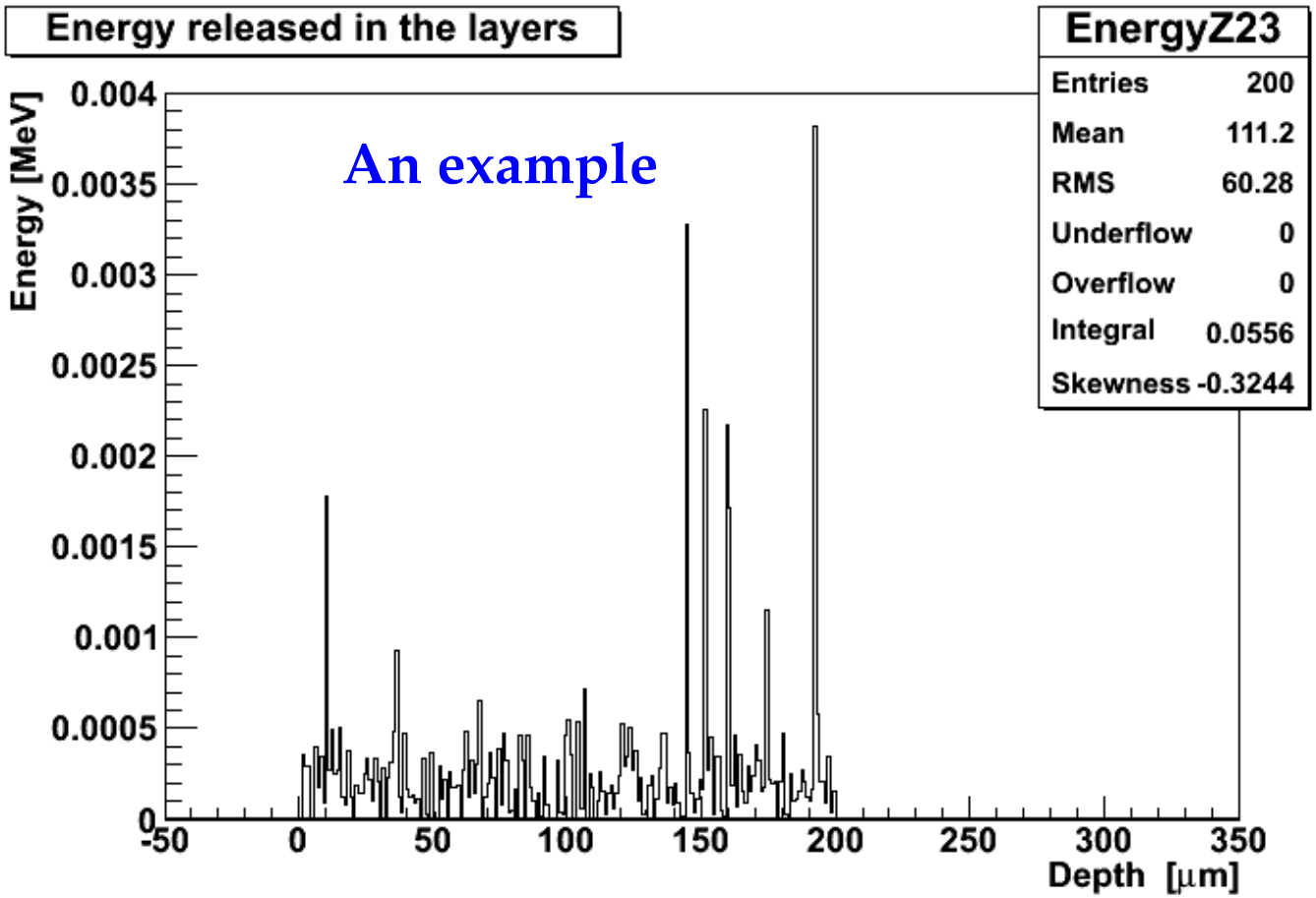
Sensor: weighting field effect

- Uniform charge release along the sensor thickness
- Charge injection at pixel center and close to the edge



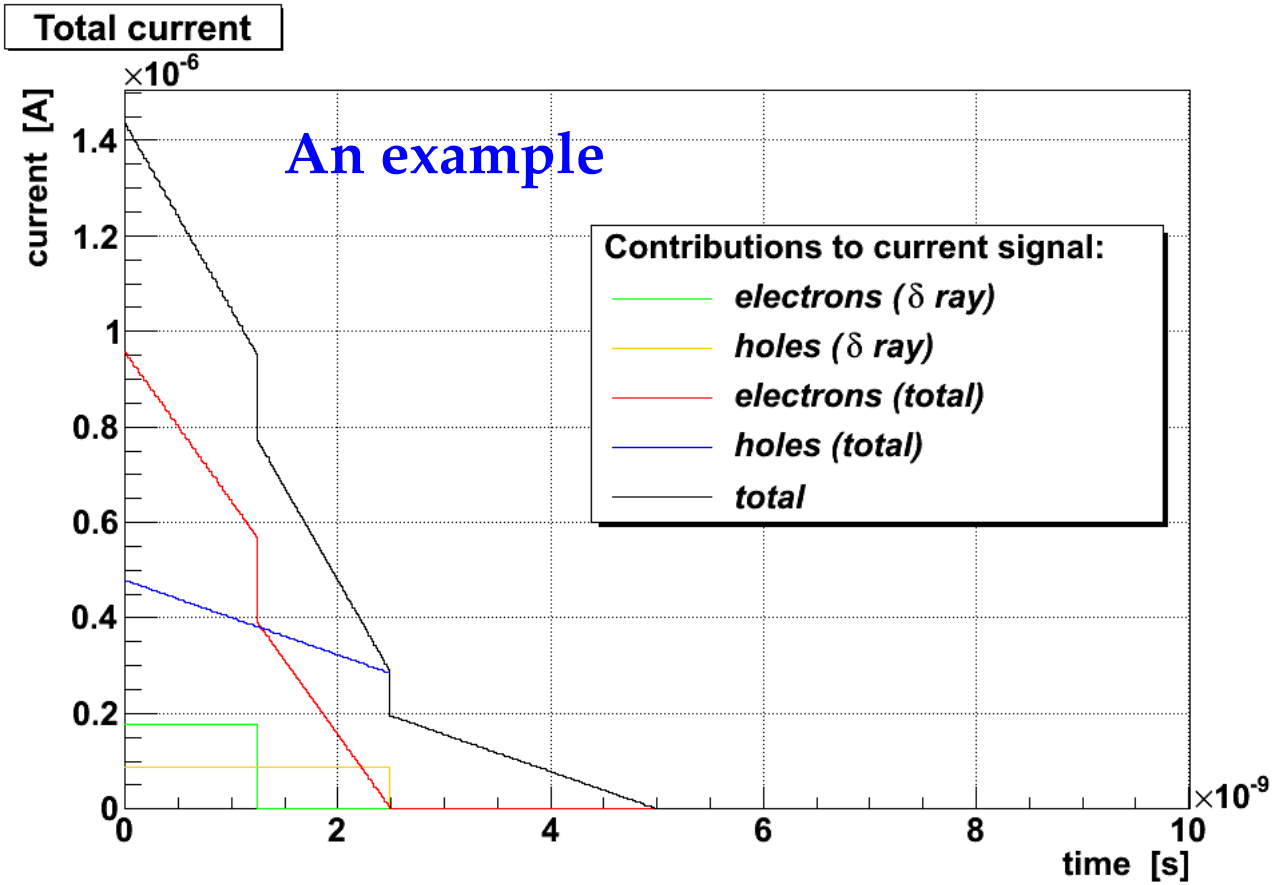
Sensor: energy straggling (1)

- Energy released as a function of depth in silicon
- 200 μm thick silicon divided in 200 layers (1 μm each)
  - GEANT4

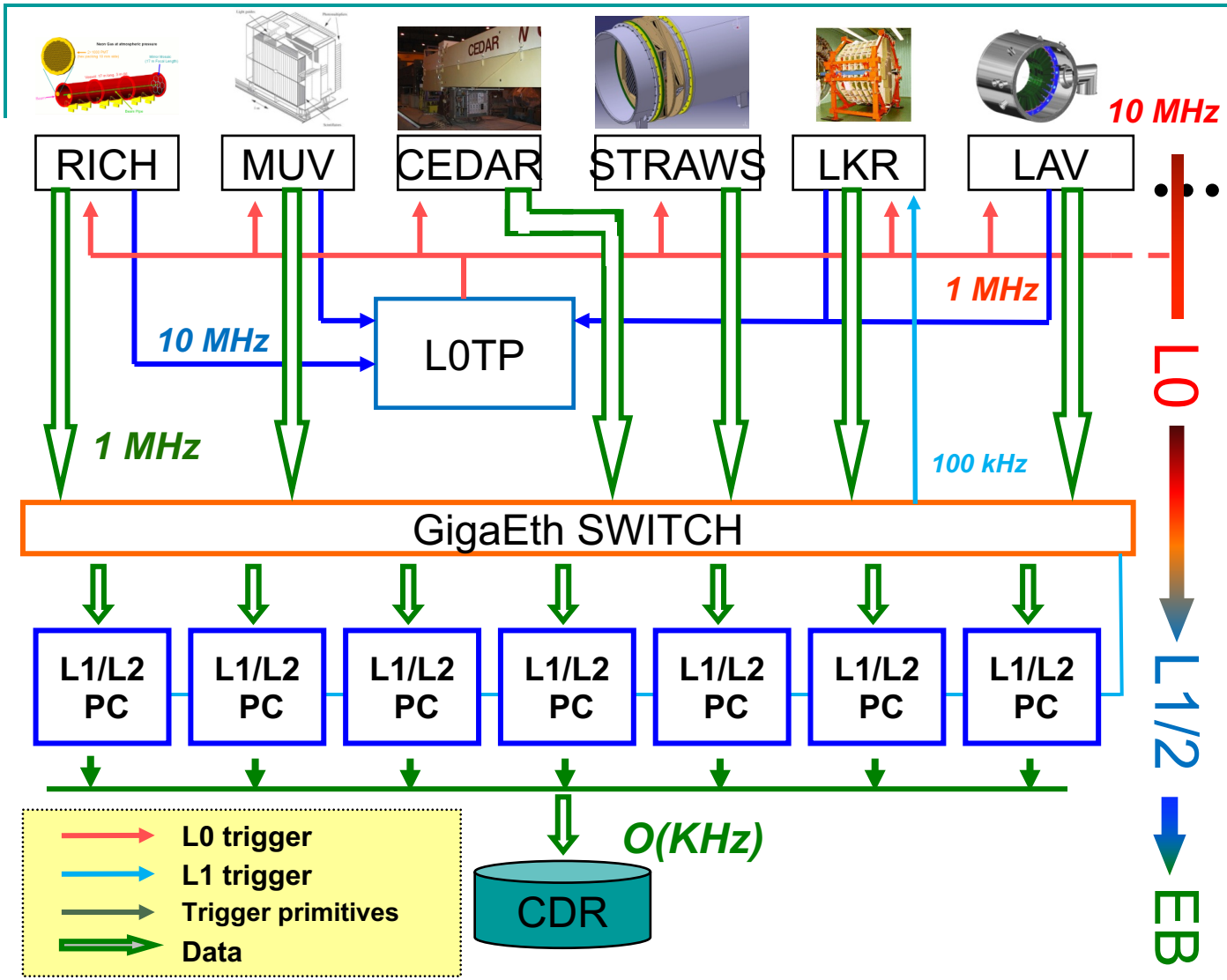


Sensor: energy straggling (2)

- Total charge release of 54 keV (2.4 fC)
- One δ ray emitted at 100 μm
- δ ray energy is 10 keV (~0.4 fC)

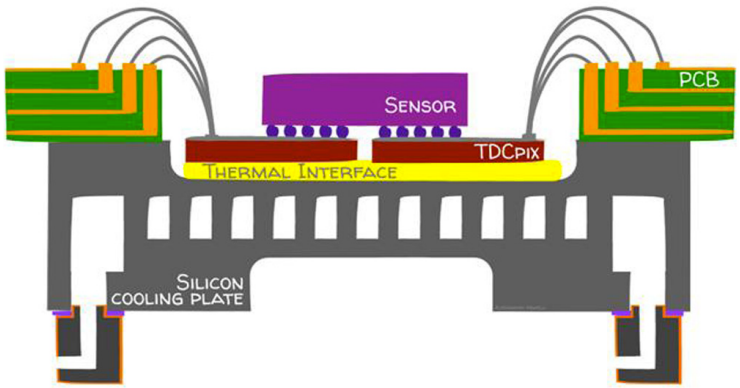


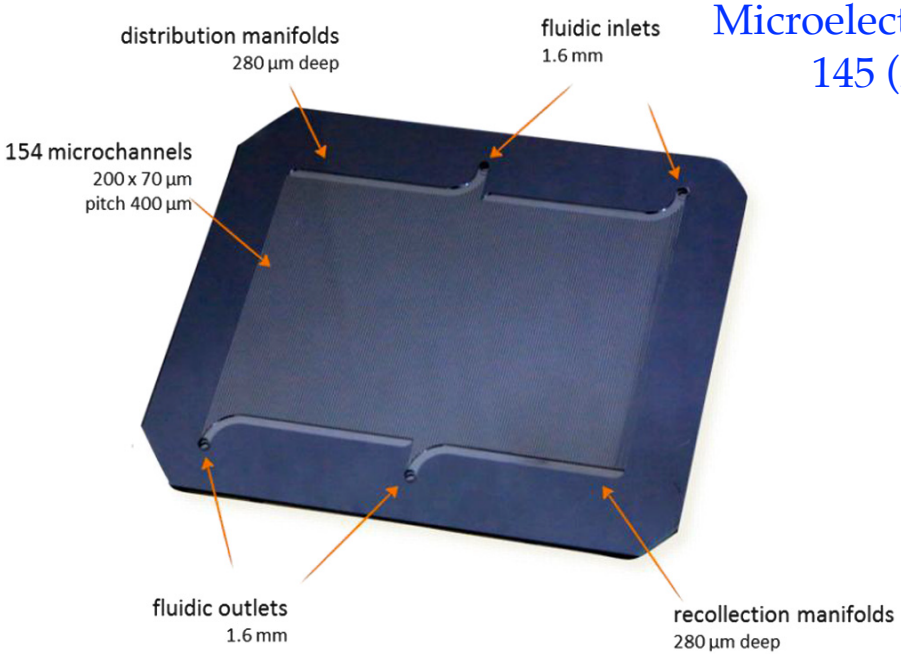
NA62 Trigger and DAQ



- **L0**: Hardware synchronous level
  - 10 MHz to 1 MHz, **1 ms max. latency**
  - Primitives (MUV, RICH, LAV, LKR)
- **L1**: Software level
  - "Single detector", 1 MHz to 100 kHz
- **L2**: Software level
  - "Complete information", 100 kHz to 10 kHz

Micro-channel cooling





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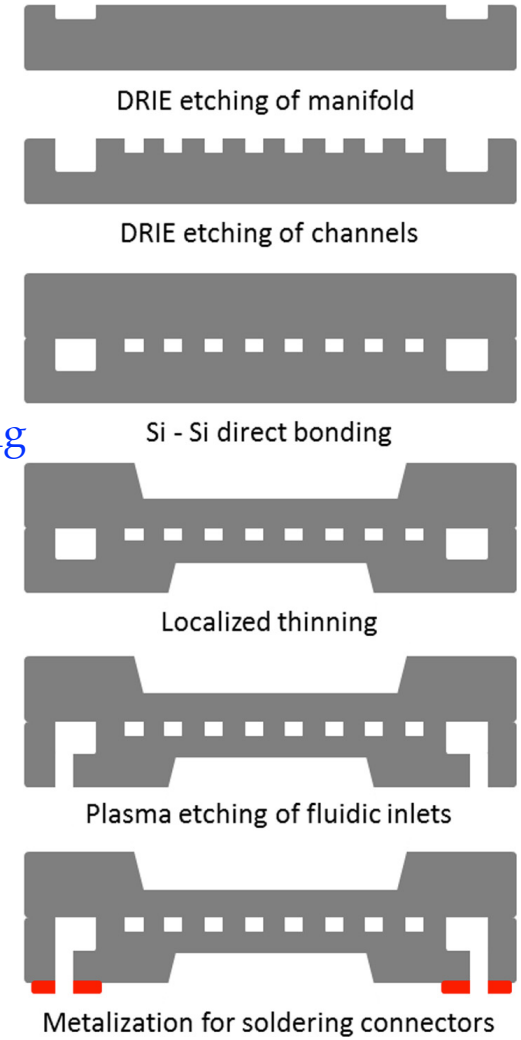
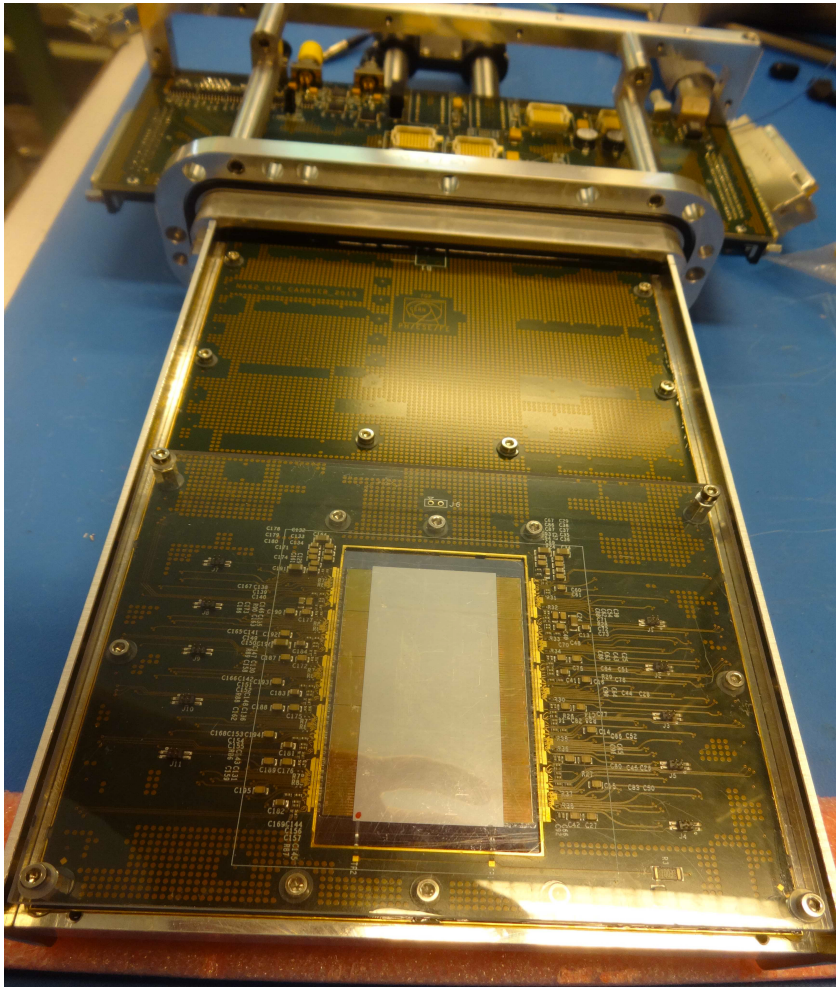
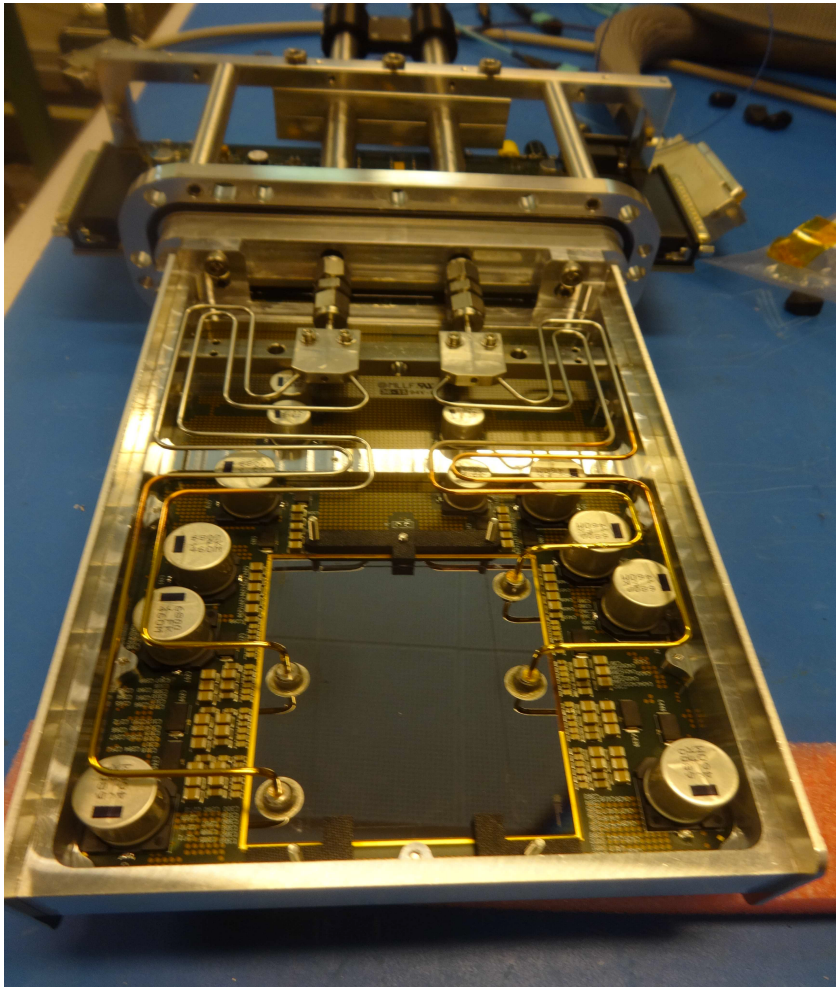


Gigatracker carrier card

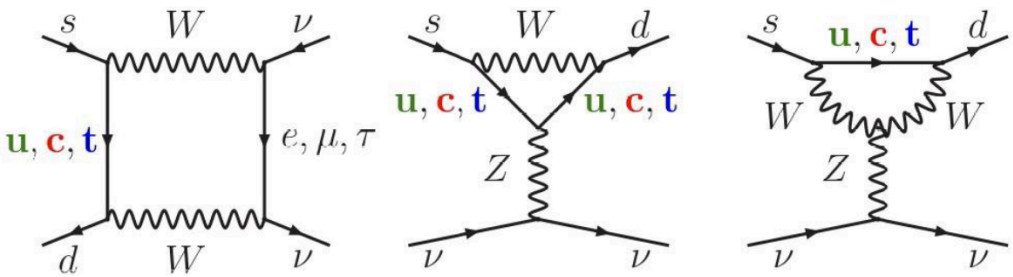




GTK-RO board

The $K^+ \to \pi^+ \nu\bar{\nu}$ decay

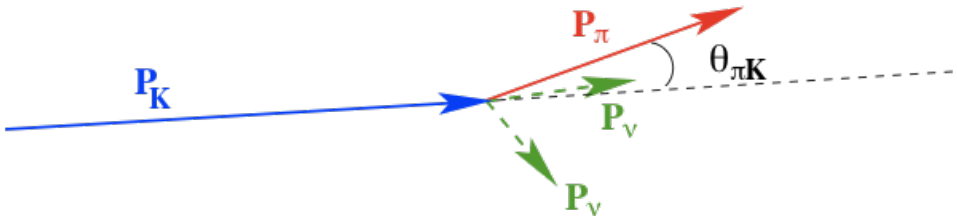
- FCNC loop process



- Ultra-rare decay:
  - BR($K^+ \to \pi^+ \nu\bar{\nu}$) = **$(8.4 \pm 1.0) \times 10^{-11}$** (SM prediction)
- Theoretically very clean: hadronic matrix element can be related to measured quantities
  - Sensitive to new physics
- Existing measurement based on 7 events (E787/E949)
  - BR = $(17.3\ ^{+11.5}_{-10.5}) \times 10^{-11}$
- The **NA62 Collaboration** aims to measure $\mathcal{O}(100)$ $K^+ \to \pi^+ \nu\bar{\nu}$ events with ~10% background at the CERN SPS in few years of data taking

Signal and background

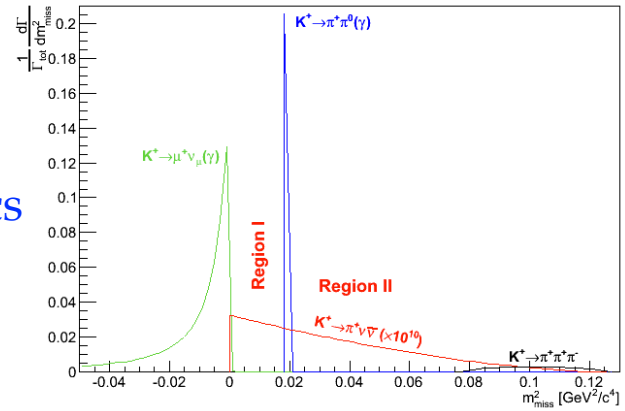
- Weak signal signature
  - K^+ track in, π^+ track out
- Backgrounds:
  - K^+ decay modes
  - Beam-gas and upstream interactions
- Experimental principles:
  - Kinematic reconstruction: $m_{miss}^2 = (P_K - P_\pi)^2$
    - Precise measurement of K and π momenta
    - Minimize multiple scattering
  - PID: K upstream, $e/\mu/\pi$ downstream
  - Hermetic γ detection
  - Sub-ns timing



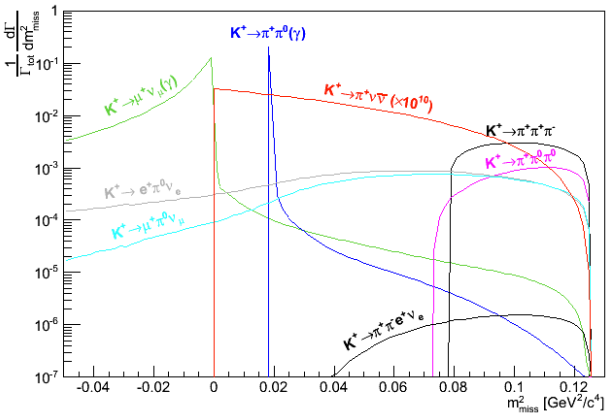
Scheme for analysis

- Signal selection
  - 1 track with 15 GeV/c < P_π < 35 GeV/c and π PID in RICH
  - No μ in MUVs; No γ in LAV, LKr, IRC, SAC
  - 1 beam particle in Gigatracker with K PID by KTAG
  - Z_{vtx} in 65 m fiducial volume

Closed kinematics 92%



Open kinematics 8%



- NA62 goal: 100 signal events with ~10% background
  - With ~10% acceptance (3% + 9%), need 10^{13} K^+ decays and about 10^{-12} background rejection