Vertical integration technologies for tracking detectors

Valerio Re

Università di Bergamo
Dipartimento di Ingegneria e Scienze Applicate

INFN
Sezione di Pavia

Outline

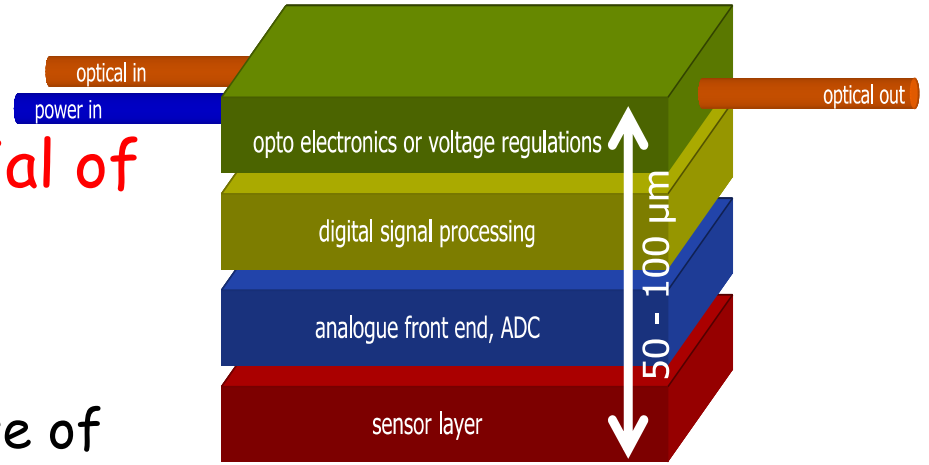
- Vertical (or 3D) integration aroused a lot of interest in view of the design of a new generation of silicon tracking detectors and readout electronics. Where are we today?

- Status and prospects of 3D integration for detectors and electronics in HEP and photon science: ideas, technologies, projects,…

This project has received funding from the European Union Horizon 2020 research and innovation program under grant agreement No. 654168

What is 3D integration?

- 3D electronics: "the vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers."[1]



- 3D electronics has the potential of being:
  - Denser (smaller form factor)
  - Faster (reduced delay because of shorter interconnects)
  - Lower power (smaller interconnect capacitance)
  - Lower cost (sizably less expensive than aggressive CMOS scaling)
  - Integration of dissimilar technologies (sensor, analog, digital, optical)

1) Philip Garrou, Christopher Bower, Peter Ramm, Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits,Wiley-VCH, 2008.

Advancing the state of the art of pixel sensors for a next generation of HEP experiments…

New demanding specifications for experiments at new machines (HL-LHC, Linear Colliders, FCC,…):

- **Improve resolution ⇒ shrink pixel size and pitch**, down to 20 μm or even less
- **Preserve or even increase pixel-level electronic functions**

  handling of high data rates (3 GHz/cm^2 hit rates), analog-to digital conversion, sparsification, intelligent data processing…: presently this also contributes to limiting the minimum size of pixel readout cells
- **Decrease amount of material ⇒ thin sensor and electronics** chips, "zero mass" cooling

  Necessary to reduce errors in track reconstruction due to multiple scatterings of particles in the detector system

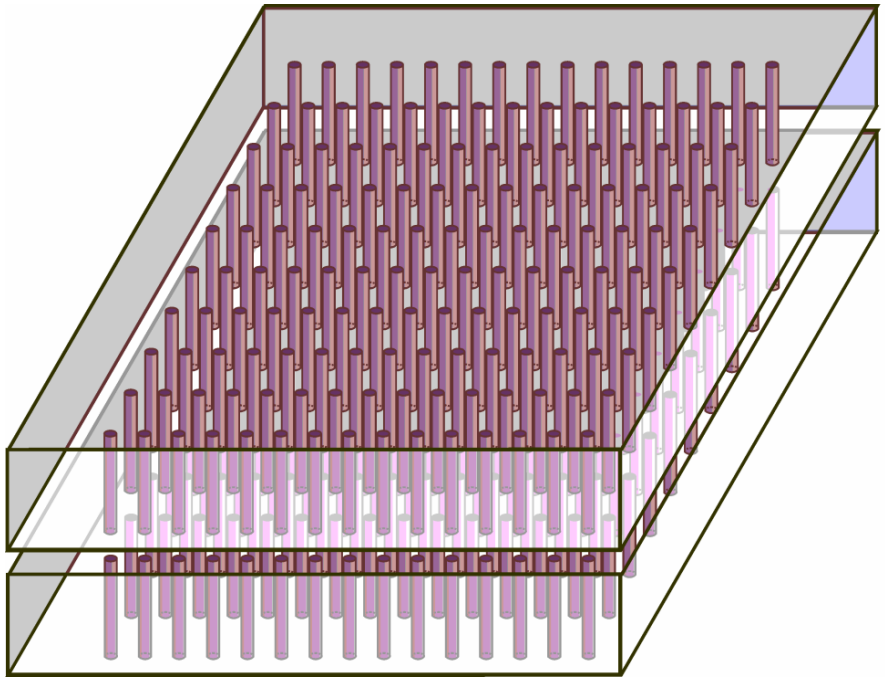
  50 -100 μm total thickness

…and photon science

Potential benefits of new microelectronic technologies to future detector systems for X-ray imaging at free electron laser facilities:

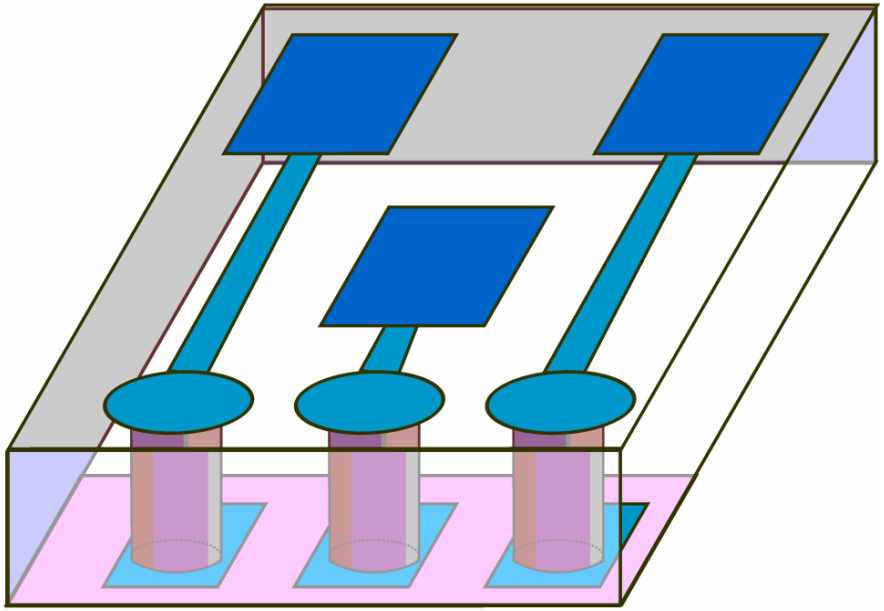
- Reduction of pixel size (100x100 μm^2 or even less), presently limited by the need of complex electronic functions in the pixel cell
- Larger memory capacity to store more images
- Advanced pixel-level processing (1 – 10000 photons dynamic range, 10-bit ADC, 5 MHz burst mode or 100 kHz continuous mode operation)
- 4-side buttable tiles for a large area detector with minimum or no dead area

3D integration: high-density multi-layer vs low-density



3D IC

- Small diameter (~1μm), shallow (<~10μm) and highly dense pitch (~2μm) Through Silicon Vias
- ASICs composed of multiple tiers that exchange signals through inter-tier bonding interfaces (dense and low C)



almost-3D IC

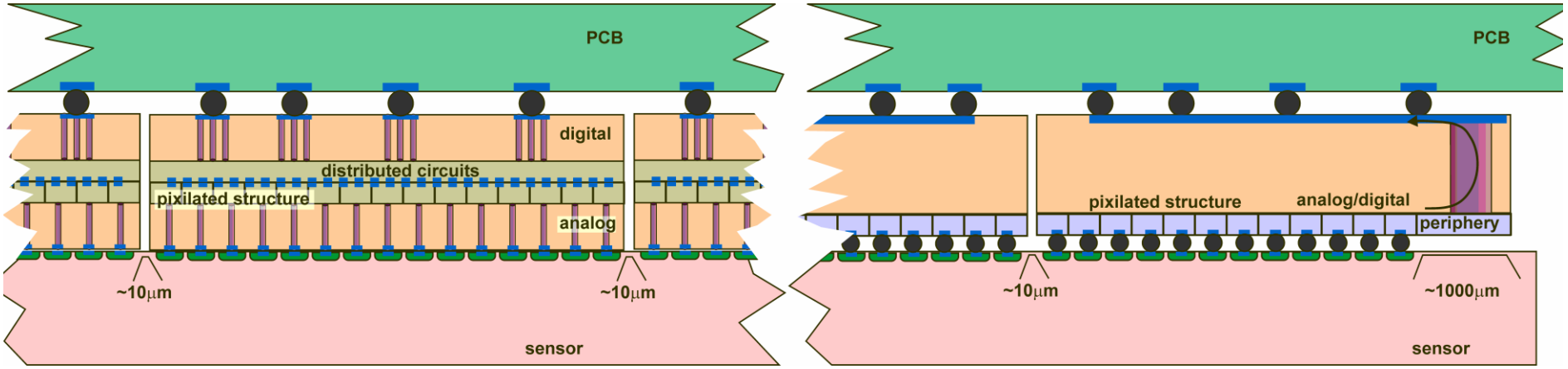
- Large diameter (~50μm), deep (~100μm) and coarse pitch or peripherally located Through Silicon Vias
- ASICs are single layer, and TSVs are used to carry I/Os from one side to another (few, high C)

Fermilab

Courtesy of G. Deptuch, FNAL

The potential of the two versions of 3D integration

pixel detectors



3D IC

- Unprecedented forms of pixel detectors are possible, i.e. seamlessly assembled on large area pixel sensor (or entirely edgeless, i.e. 4-side buttable)
- Separate functions of tiers: analog (pixilated) and digital (distributed circuits) tiers
- New technology ⇨ increased costs

almost- 3D IC

- Improved forms of pixel detectors with reduced dead zones, avoided wire-bonding and
- Rigid form of pixilated layout of processing analog/digital ASIC with I/O. control and other functions located on periphery/balcony
- Conservative technol. ⇨ moderate costs

Fermilab

Courtesy of G. Deptuch, FNAL

R&D on 3D integration: results, present work, plans for the future

- The pixel sensors community has been working with several companies providing 3D integration technologies (Through-Silicon Vias, low-mass bonding,…)

- There is a lot of obvious synergy between photon science and particle tracking in 3D integration projects for new pixel detectors

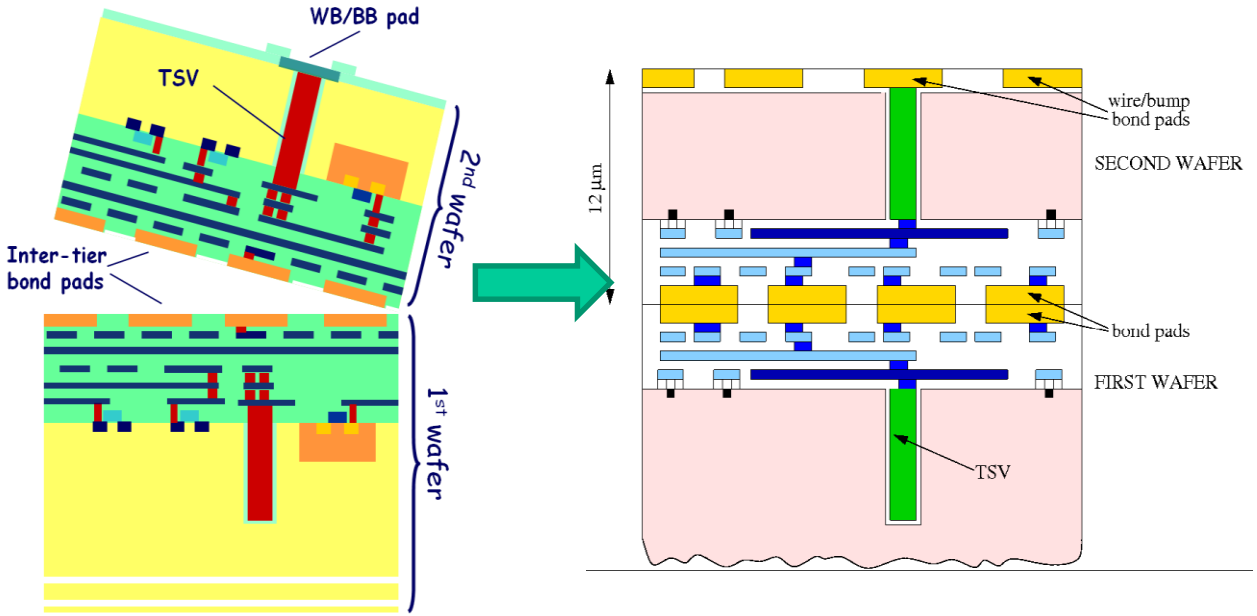
- Fermilab has been a major driving force in this field; groups in Japan and Europe have been also very active, forming consortia and collaborating in the frame of research networks (in Europe: AIDA WP3 and AIDA-2020 WP4)

- In this talk I cannot cover everything: I'll focus on some developments which, despite problems and setbacks, outline the great potential of the various flavors of 3D integration

Experience with "aggressive" 3D integration: the first run of the 3D-IC consortium

3D MPW run organized by Fermilab, collecting designs from various institutions in US and Europe – 2009

- Through-Silicon Vias (TSV) etched at early stages of a 130 nm CMOS process (after transistor fabrication) at the silicon foundry. High density vertical interconnections. High-density, low-mass bonding of CMOS layer by a Cu-Cu thermocompression process or by DBI bonding (reworkable, better alignment).



very small TSV: Φ_{via}=1.2 µm, $\Phi_{landing_pad}$=1.7 µm, d_{min}=2.5 µm

Wafer bonding pads are nominally on a 4 µm pitch

Low capacitance interconnects

Results of the first 3D-IC MPW run

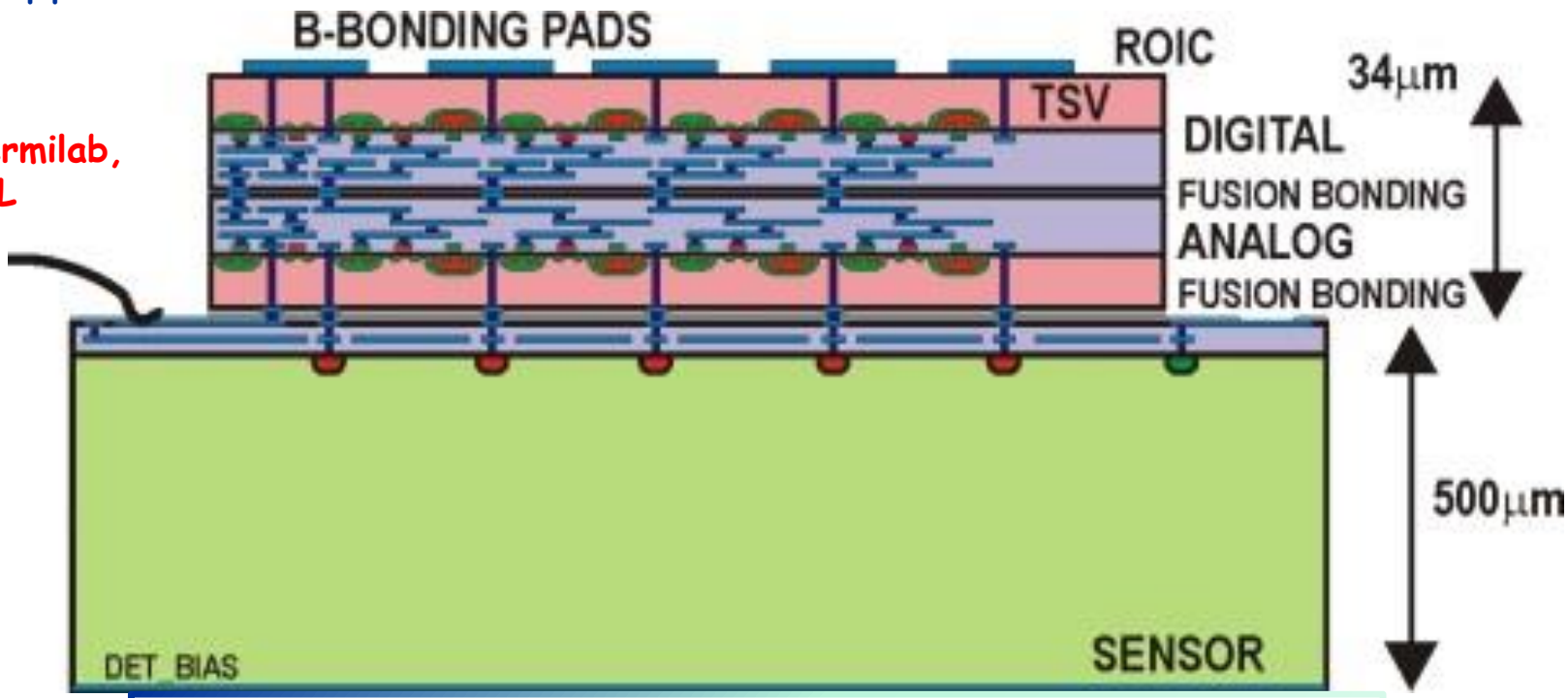
- Various large-scale chips were fabricated (2-layer CMOS readout chips and CMOS sensors).
- Despite well-known delays and problems, this run provided a proof of principle of the advantages and potential of 3D integration.
- Among these:

  - Performance of transistors and circuits is retained after 3D processing steps
  - The separation of analog and digital circuits in two different layers reduces digital-to analog interferences
  - 3D CMOS sensors with small pitch and complex pixel-level analog and digital functions can operate with high efficiency
  - Advanced digital readout architectures were devised, and thin assemblies of silicon sensors and front-end chips were fabricated and successfully tested

A demonstrator of 3D integration in the first MPW run: the VIPIC chip

Vertically Integrated Photon Imaging Chip (VIPIC)
detector: Si d=500 μm, pitch 80×80 μm², soft 8keV X-rays
application: XPCS

Collaborating institutions: Fermilab, AGH-UST, BNL

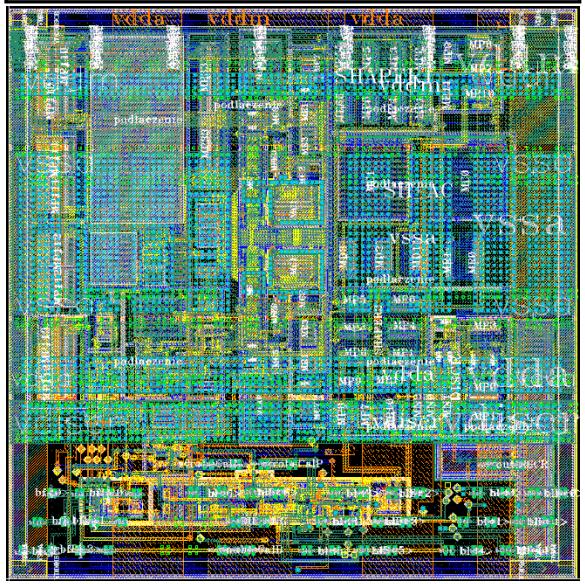


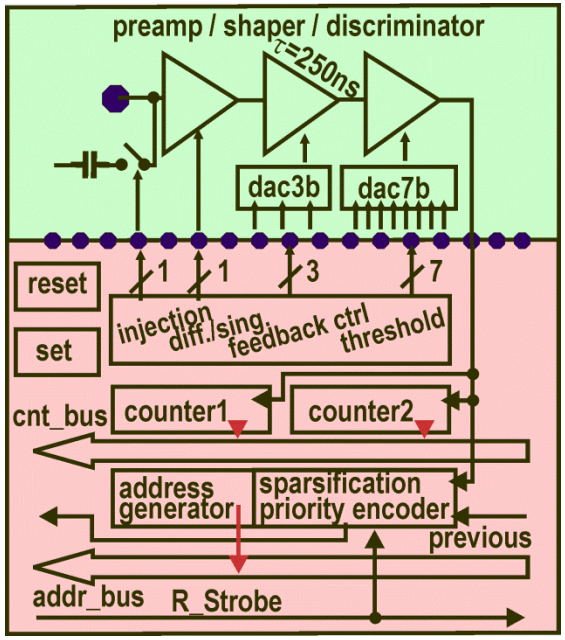
VIPIC bonded to sensor can be tested through wire bonded and bump-bonded connections

"Vertically Integrated Circuits at Fermilab", IEEE Transactions on Nuclear Science, vol. 57, no. 4, (2010), pp. 2178-2186
"VIPIC IC - Design and Test Aspects of the 3D Pixel Chip", Proc. of Nuclear Science Symposium, Knoxville, USA, Oct. 2010
"Design and Tests of the Vertically Integrated Photon Imaging Chip", IEEE Transactions on Nuclear Science, vol. 61, no. 1, (2014), pp. 663-674
"Fully 3-D Integrated Pixel Detectors for X-rays", IEEE Transactions on Electron Devices, vol.: 63, no. 1, (2016), pp. 205-214

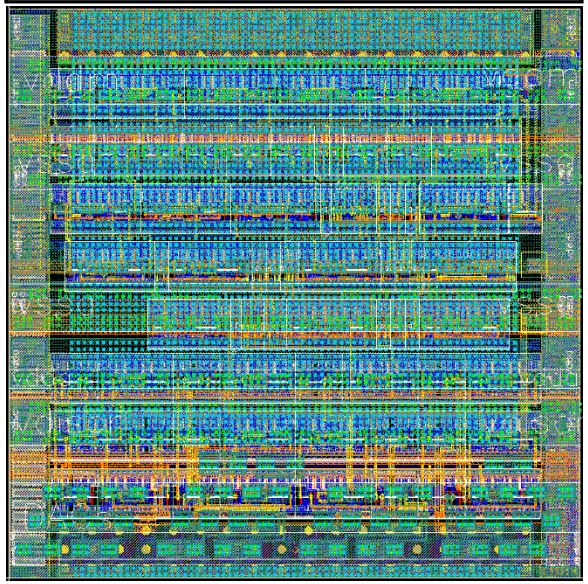
The two layers of VIPIC

Analog: 280 transistors





Digital:1400 transistors



- Single ended or pseudo-differential CSA-shaping filter-discriminator - design goals: shaping time τ_p=250 ns, power ~25 μW / analog pixel, noise <150 e^- ENC, gain(C_{feed}=8fF) = ~100mV/8keV (optimized for 8 keV in Si - linear up to 3 × 8 keV)
- 1 threshold discriminator
- 10 bit/pixel DAC adjustments

12-bit for configuration
7-bit trim offset, 3-bit trim R_f, single/dif mode, CAL enable

2-lines for CAL circuits

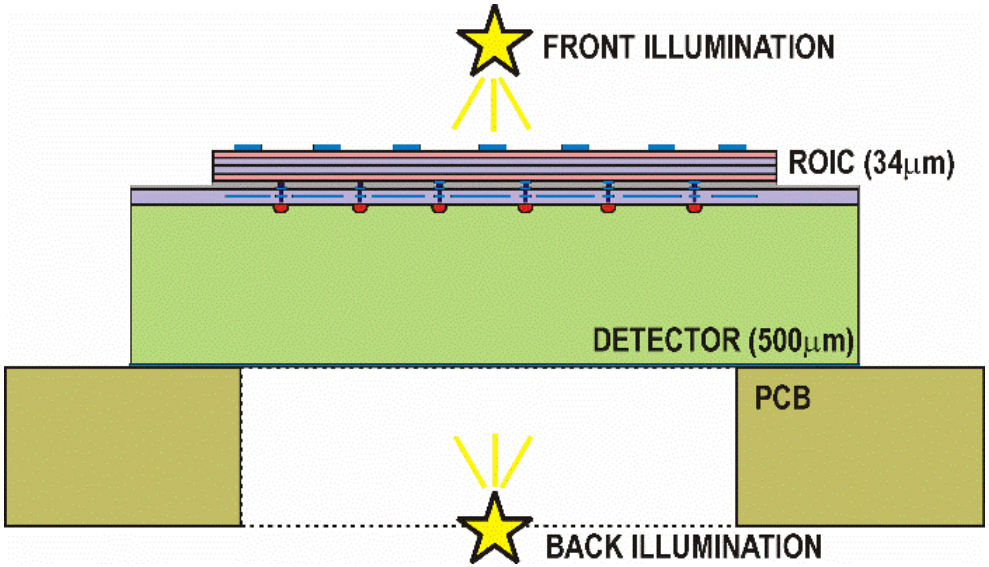
discriminator output

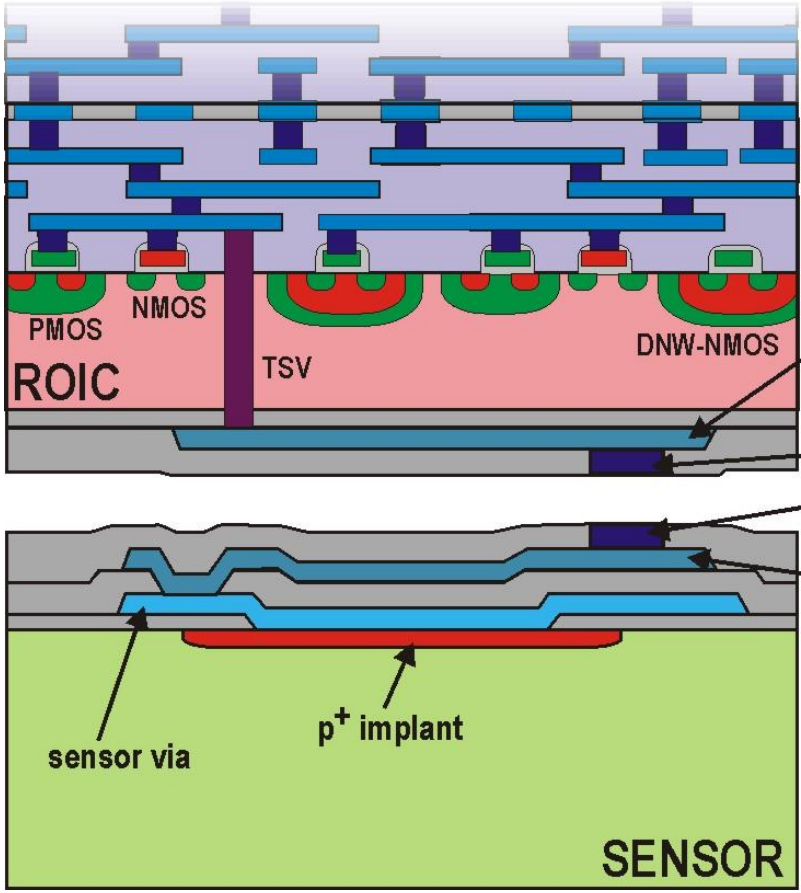
Doubled bond pads for each signal
Power supplies tied between tiers

- in-pixel 1-stage pipe-line logic
- distributed sparsifier: 8 bit priority encoder, pixel readout selector, pixel address generator and counter output
- 2 × 5-bit long counters
- configuration registers: single bit / pixel (pixel SET, pixel RESET) and 12 bit DAC and configuration (calib., singl./diff.)

Collaborating institutions:
Fermilab, AGH-UST, BNL

The VIPIX chip was successfully connected to a sensor (with a direct bonding process), and tested with back-side and front-side illumination.





An "ultimate 3D" device was bump-bonded on the other side to a PCB.

'ultimate 3D VIPIC1'

Ni-DBI (oxide-oxide fusion bonding) with DBI post ϕ=5 mm,

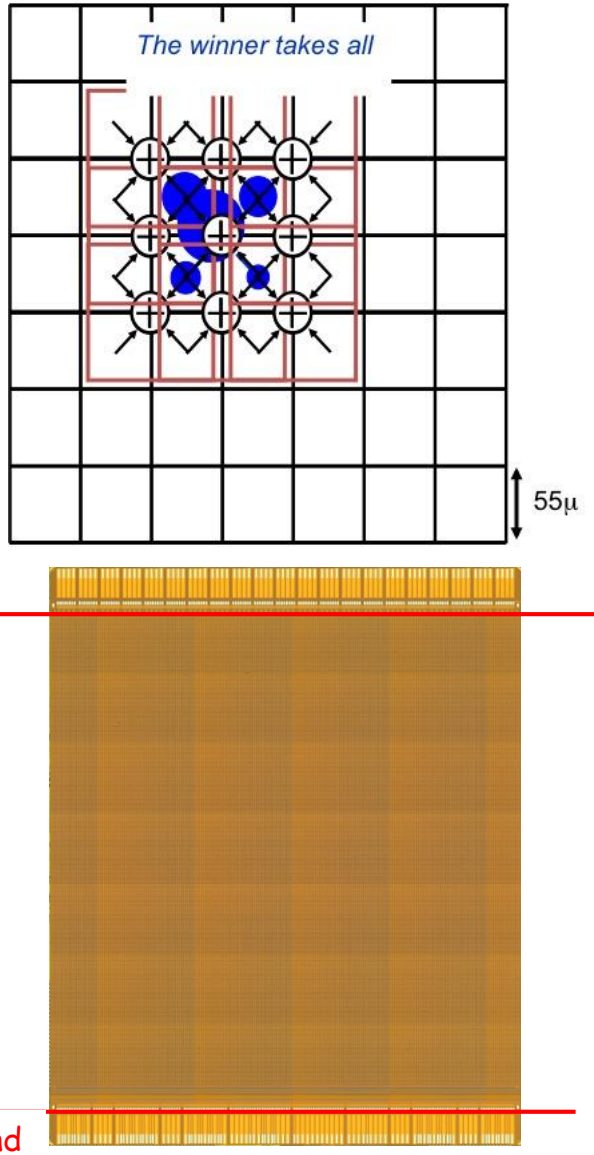
top-2-bottom: 50nm nitride, 1μm oxide, 300nm Al, 1μm oxide + 700nm DBI and 700nm DBI + 1μm oxide, 300nm Al, 1um oxide, 300nm thermal oxide

3D heterogeneous integration and "via last" approach

- Even with low-density 3D technologies, sizable performance improvements might be gained by fabricating devices with 2 layers, each optimized for its functions (particle sensing, readout electronics), with additional advantages such as removing dead areas.
- Low-density peripheral TSVs on fully processed CMOS wafers reach backside bonding pads for external connection.
- The **"via last"** approach and **3D heterogeneous integration** were tested both for HEP and imaging applications (with support from the AIDA FP7 project) and are still being pursued by our community
- Tests of TSV processing were performed on ATLAS pixel readout chips
- A demonstrator module with MEDIPIX chips with TSVs bonded to sensors was successfully tested

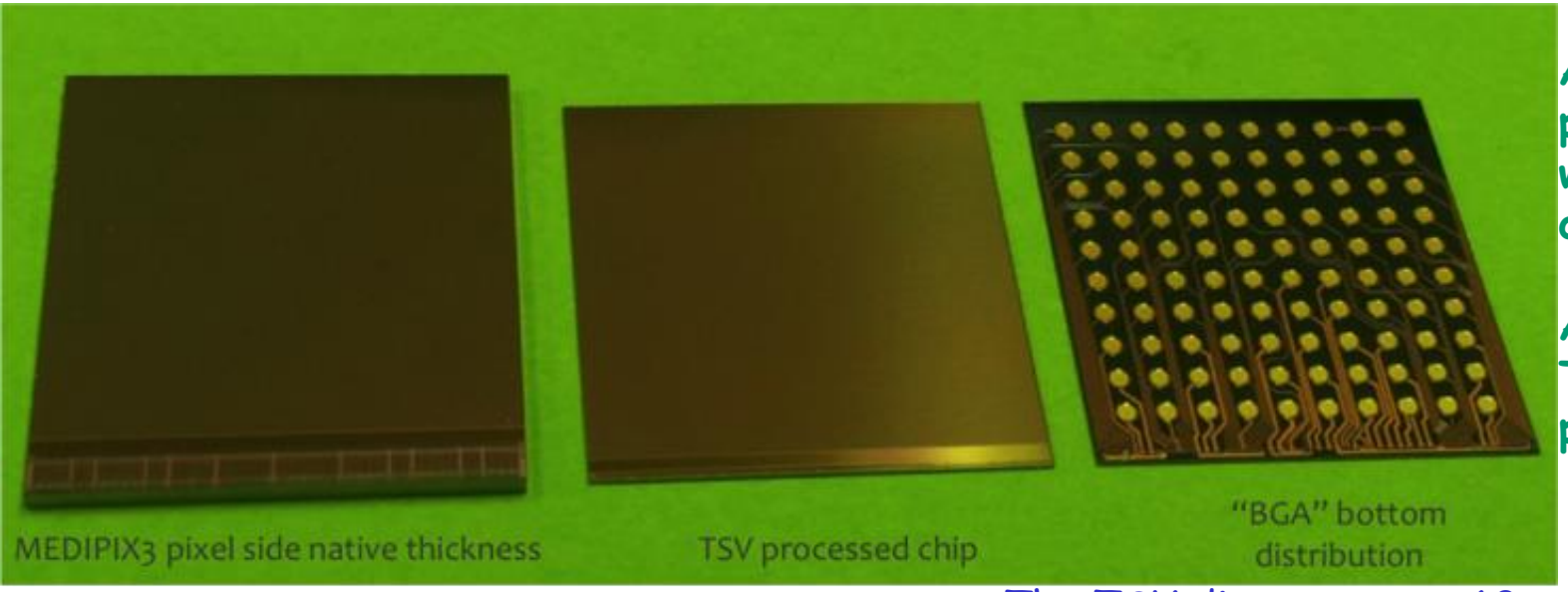
CERN: TSV on MEDIPIX3 for minimal dead area and 4-side butting

- MEDIPIX3: 130 nm CMOS chip for high resolution X-ray spectral imagers based on hybrid pixel detectors (256x256 square pixels of 55 μm size)
- Novel charge summing architecture: charge in 4-pixel cluster added to pixel with largest charge, eliminating spectral distorsion due to charge diffusion in the sensor (highly programmable, can operate at 110 μm pitch in spectroscopic mode)
- For 4-side buttable imaging tiles, remove periphery with I/O pads, insert TSVs and backside redistribution layer with BGA pads (CEA-LETI process)



D. Henry et al., TSV Last for Hybrid Pixel Detectors: Application to Particle Physics and Imaging Experiments , in proceedings of the 63rd IEEE Electronic Components and Technology Conference (ECTC) (2013), p. 568.

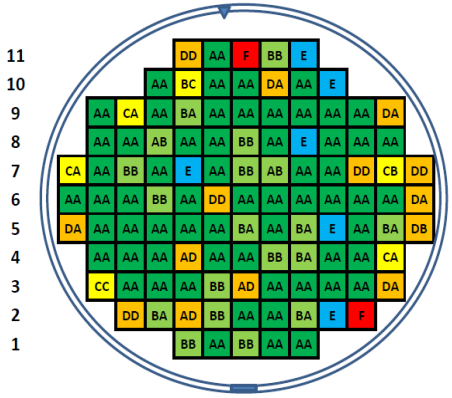
Low-density peripheral TSVs in the MEDIPIX chip



All IO logic and pads contained within one strip of 800µm width

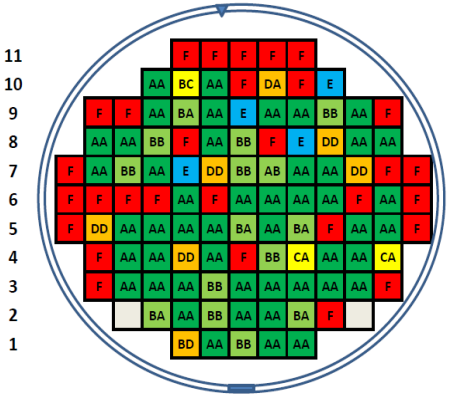
All IO´s have TSV landing pads in place

W128_AZPGBPH_before_TSV



AA	62	57%
BB, BA or AB	19	17%
CC, CA, AC, BC or CB	6	6%
D	14	13%
E	6	6%
F	2	2%
Total	109	100%

W128_AZPGBPH_after TSV



AA	48	45%
BB, BA or AB	15	14%
CC, CA, AC, BC or CB	3	3%
D	7	7%
E	4	4%
F	30	28%
Total	107	100%

C2 and K2 were not received

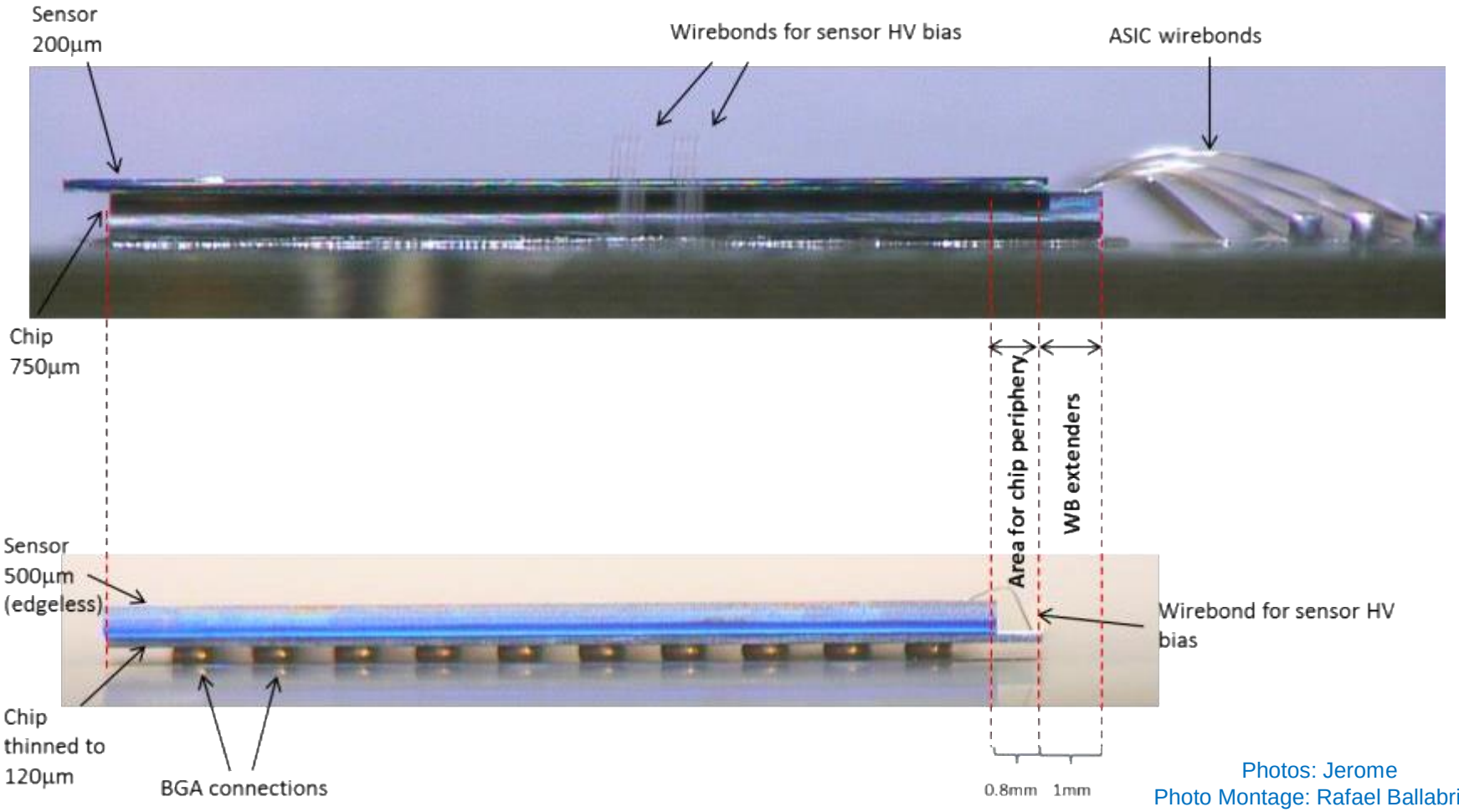
The TSV diameter was 60 µm (to match a wire bond pad pitch of roughly 100 µm) and the wafers were thinned to 120 µm for an optimised aspect ratio of 2.

TSV yield is adequate for small scale production; chip performance is preserved

Towards a new generation of pixel detector readout chips, M Campbell et al, IWORID 2015

Hybridization of TSV processed MEDIPIX chips

- Comparison between WB and TSV on board integration



Photos: Jerome
Photo Montage: Rafael Ballabriga

Flip chip interconnection to sensors: assemblies by VTT/ADVACAM

3D integration for the next generation of MEDIPIX and TIMEPIX chips

TSV processing on 'ultra-thin' MEDIPIX3RX chips was also performed with good yield (wafers thinned to 50 μm, TSV diameter 40 μm), as a test of extremely thin assemblies primarily for vertex detector applications in high energy physics.

Next generation of 65 nm MEDIPIX4 (spectroscopic X-ray images at rates compatible with human CT) and TIMEPIX4 readout chips (sub-ns time stamping and reduced pixel pitch):

- in both chips the **functions normally associated with the chip periphery will be located throughout the pixel matrix** taking full advantage of the opportunities provided by the TSV process.
- as the readout logic is no longer confined to one chip edge there is **more flexibility in the choice of readout architectures**. The chips should be abuttable on 4 sides.

"Via Last" 3D integration for HL-LHC Inner Trackers

AIDA-2020 WP4 groups are currently working with two different technology providers for **Through-Silicon Vias in 130 nm CMOS FE-I4 pixel readout chips.**

Results are expected in late 2016. Plans are to **extend this study to 65 nm CMOS wafers from the RD53 engineering run.**

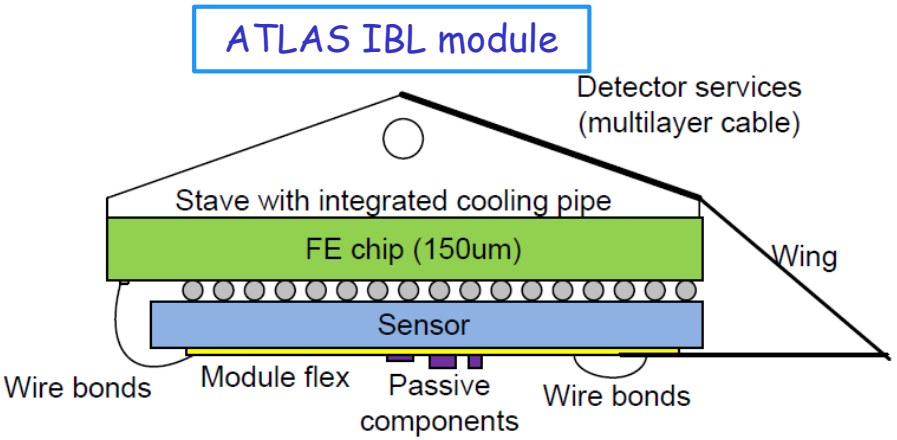
Plan is to overcome limitations of hybrid pixel modules

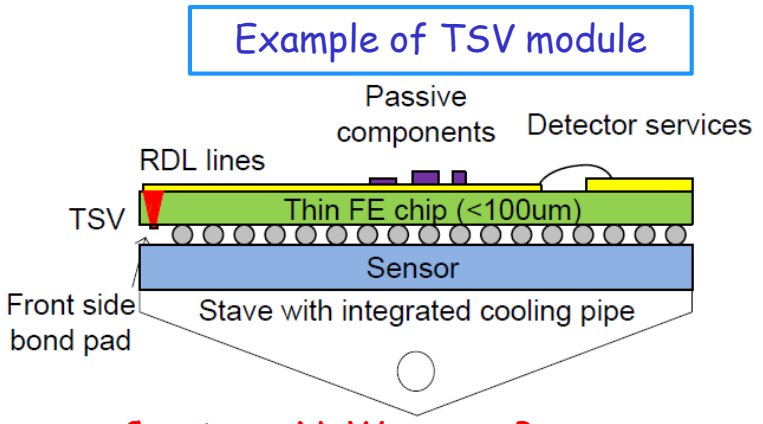
- Wire bonds connect FE to flex:
  - Oscillation in magnetic field
  - Limit on envelopes
- Access to bond area on FE limits sensor active area (not 4-side buttable)
- Requires expensive die-to-die assembly
- Wire bond Inductance limits signal speed
- Edge access -> power distribution over large chip challenging

via last TSV process on ATLAS pixel chips

- modules for ATLAS pixel detector at the HL-LHC using a via last TSV process
  - Post-processing technology applicable on existing FE electronics
  - Dead area at the chip periphery can be reduced
  - → Compact, low mass hybrid pixel modules with minimal modification to the FE layout and using standard CMOS technology
  - → No wire bonds needed if combined with advanced flex hybrid interconnection
  - → Potential for 4 side buttable modules using dedicated sensor layout
  - → With backside RDL, better power distribution over large chip

- Modules with TSV can be used for the outermost detector layers at the HL-LHC to provide full detector coverage over the large area





Courtesy: N. Wermes, Bonn

Successful TSV applicaJ on w/ AIDA_FP7 w/ FE-I3

- Process: IZM via last tapered TSV
- Demonstrator single chip modules built:
  - FE-I3 ATLAS pixel readout chip 90µm thin, with **tapered** profile TSV and RDL
  - Planar n-in-n sensor
  - Standard flip chip process (no handle wafer for thin chip handling used, unconnected pixels expected along the chip perimeter)
- No loss in performance wrt modules without TSV

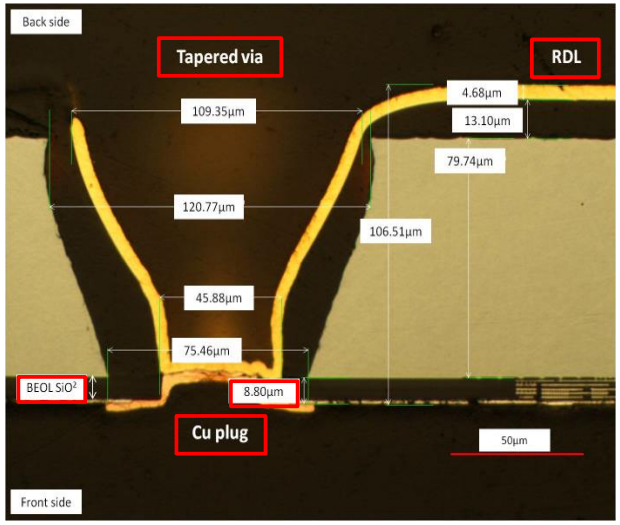
A via last TSV process applied to ATLAS pixel detector modules: proof of principle demonstration

M Barbero[a], T Fritzsch[b], L Gonella[a], F Hügging[a], H Krüger[a], M Rothermund[b] and N Wermes[a]

Published 10 August 2012 •

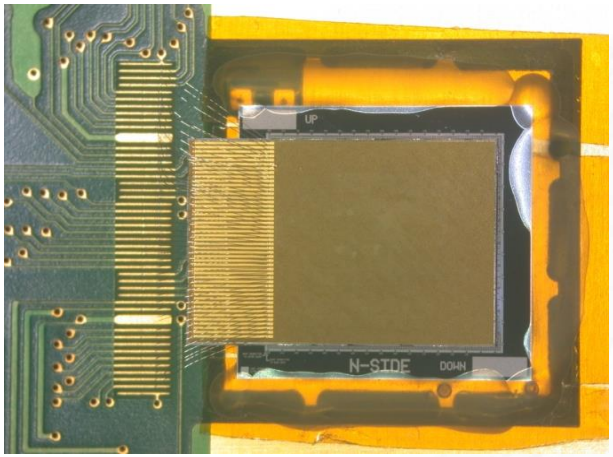
Journal of Instrumentation, Volume 7, August 2012

JINST 7, 2012

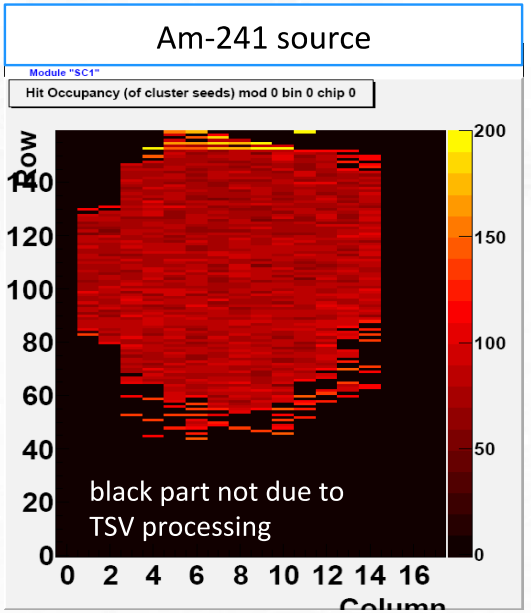


http://iopscience.iop.org/1748-0221/7/08/P08008/

Module on board



Am-241 source



Courtesy: N. Wermes, Bonn

Bonn/CPPM: TSV processing in FE_I4 chips by IZM

Goal: demonstration of BB method and TSV/RDL processes together on full FE-I4 wafers

- Pilot run with 3 FE-I4B wafers thinned to **160µm:**
  - Straight TSVs (aspect ratio ~1:2.7), copper vias, open in center
  - 2 metal layers of patterned RDL (1. Cu and 2. Ni/Au) with BCB passivation in between them on the backside
  - Flip-chip of thinned FE-I4B with TSVs w/o 2nd support wafer

Special flip chip bonder supporting the chip/sensor during reflow

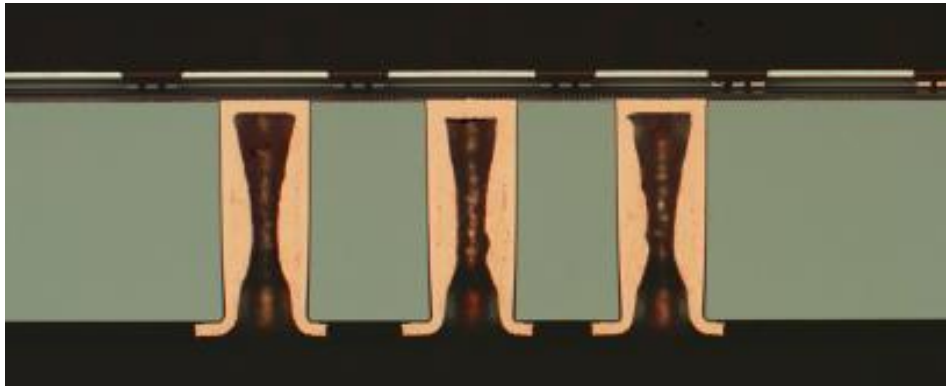
After reworking of TSV filling:

Cu layer connects nicely to M1 layer of the chip

Oxide passivation between bulk-Si and Cu-filling are perfect down to via bottom

More than 98% of the inspected TSVs show a good connection

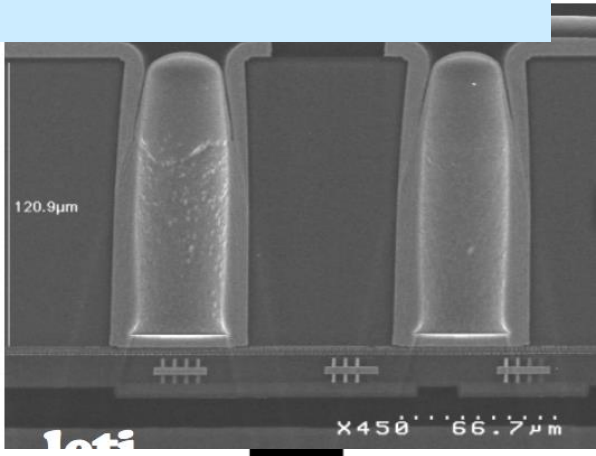
Electrical tests ongoing in Bonn



Courtesy: N. Wermes, Bonn

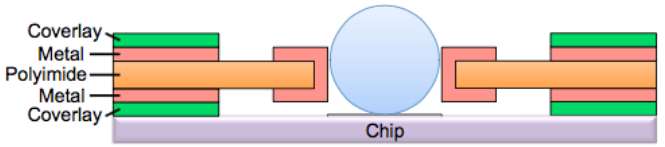
CERN, Glasgow, LAL, MPI: TSV processing in FEI4 chips by CEA-LETI

- TSV-last + RDL, build on MEDIPIX experience
- close to having first wafers back from CEA LETI. copper fill of the vias ongoing
- Besides TSV processing, plans to explore other relevant technologies for optimized interconnections



Direct laser soldering: flex to FEIx (developed within ALICE ITS)

Thin 2-layer Al flex
No glue layer needed
Connections are solder 1-by-1, module stays at RT
Re-workable



Courtesy: R. Bates, Glasgow

Wafer to wafer interconnection using direct bonding between sensor and readout chip

- FE & sensor wafers post processed with copper layer
- Wafers polished very smooth and flat
- Wafer aligned, bonded (Van der Walls force), bond annealed to 400C, wafer thinned, TSVs added
- Sensors must match readout chip on wafers: large area sensor wafers are needed (Infineon)

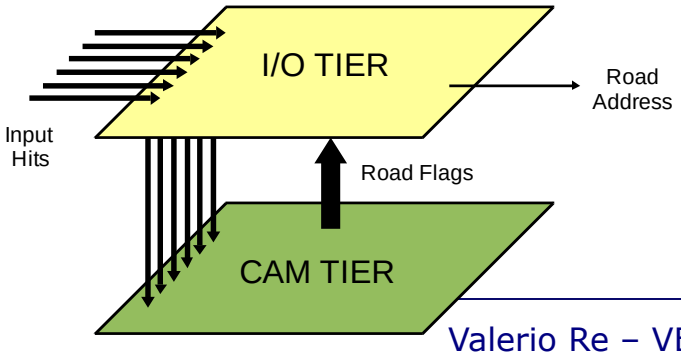
Future developments with the aggressive version of 3D integration and small pitch, pixel-level TSVs

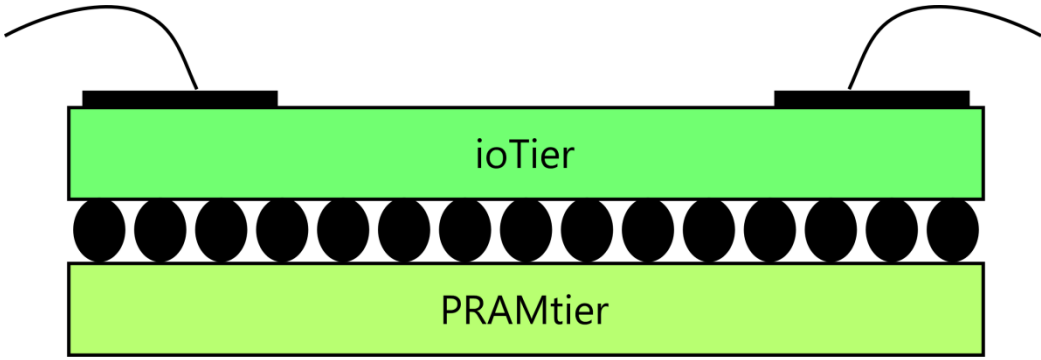
An internal 2nd 3D-IC run is organized by Fermilab, with 130 nm GF technology and Tezzaron Novati TSV post processing

Two large-size chips were designed and submitted for fabrication:

VIPIC-Large: 3D integrated pixel detector for XPCS experiments in photon science

VIPRAM: 3D integrated pattern recognition processors for HL-LHC hardware tracker



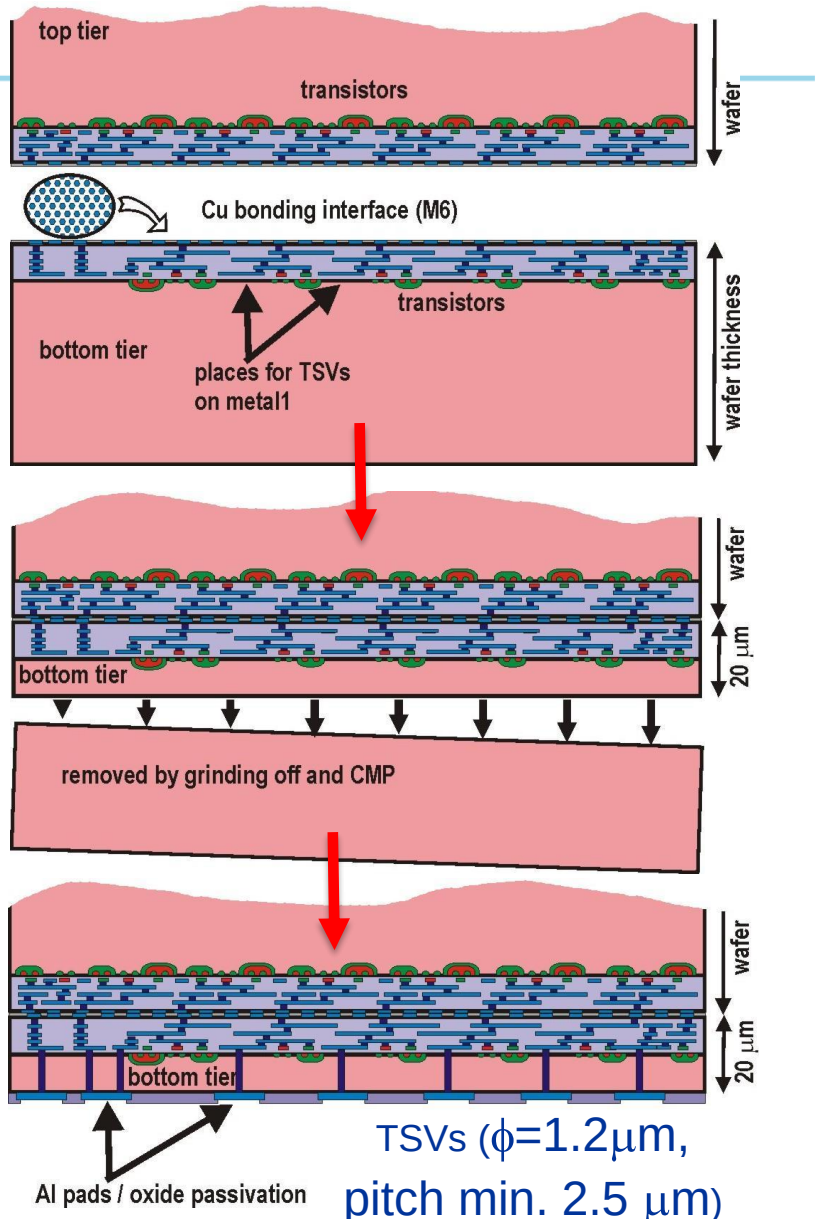


AM based approach for future Tracking Trigger applications
Ted Liu (Fermilab) CPAD meeting at Arlington, Oct 6th, 2015

Features of 2nd 3D run:

3D run Fermilab (designs from Fermilab and AGH-UST) - 2016

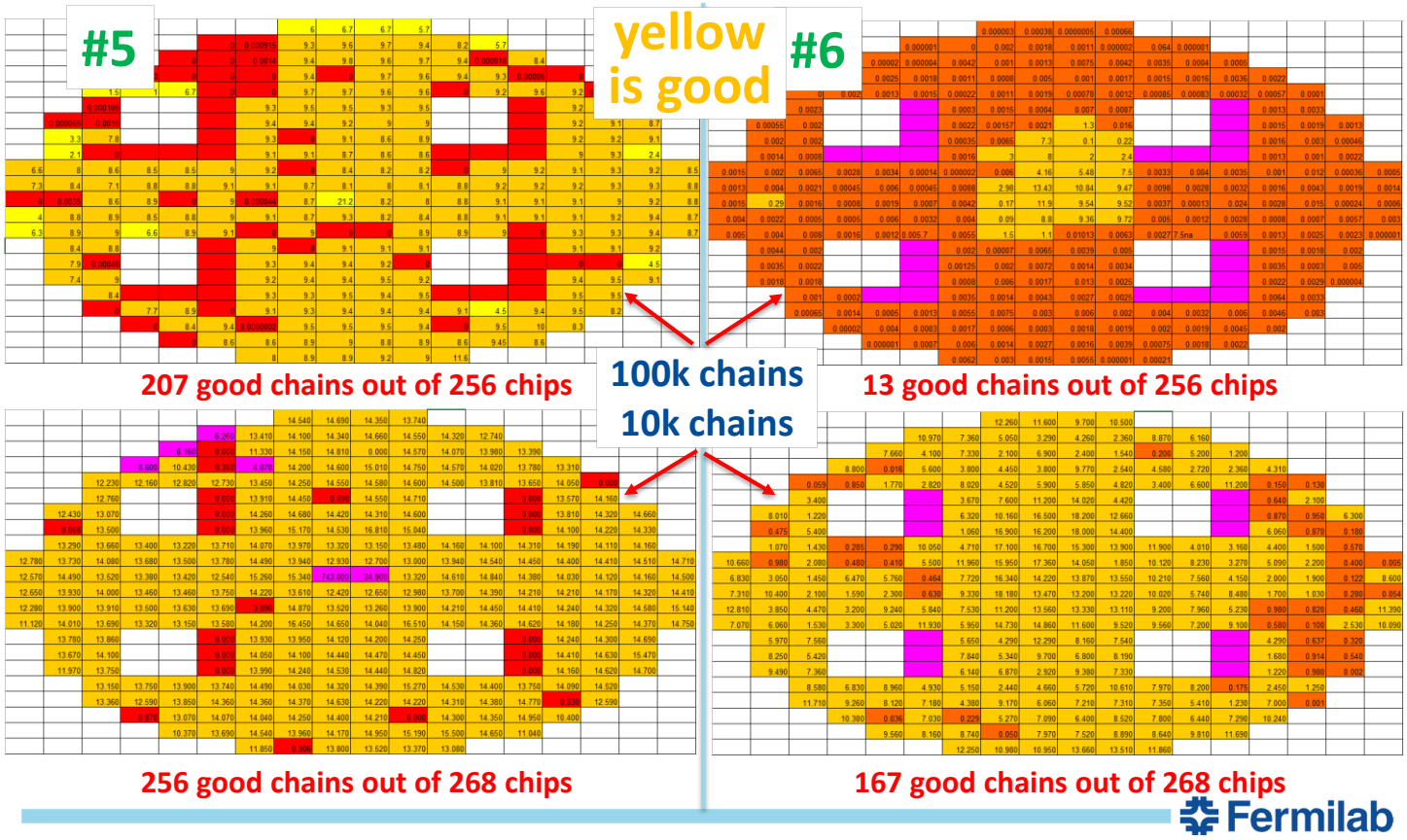
- 3D process uses standard wafers (not strictly unique foundry-dependent) but this time GlobalFoundries 130nm CMOS technology: 12" wafers, 26 × 31 mm^2 reticule, 8 metals with bond interface for face-face wafer bonding on top of 8th metal (ZIP-VIA + ZIP+PLUG)
- Through Silicon Vias added in postprocessing as Back-side TSVs – TSV cavities cut in 6 μm deep in silicon to landing pads on metal 1 (Al, Cu) applying Bosch process, filled with W
- Adding TSVs in both sides for D-2-W bonding of pixel ASICs requires passing through temporary bonding to a handle wafer
- Adding TSVs for building ASIC stack >2 layers does not require handle wafer



Test of B-TSV process

Barrier: Wafer#5: Ta 400Å / TiN 1,000Å + CVD W
Wafer#6: Ti 400Å / TiN 1,000Å + CVD W

Wafer maps of B-TSV chains connectivities (WAFER #5 and WAFER #6)



deposition spacer dielectric: 500Å Si_3N_4 + 1,500Å SiO_2.
about 50% of the deposition thickness at the side wall of TSV, which is 250Å Si_3N_4 + 750Å SiO_2 is left eventually .

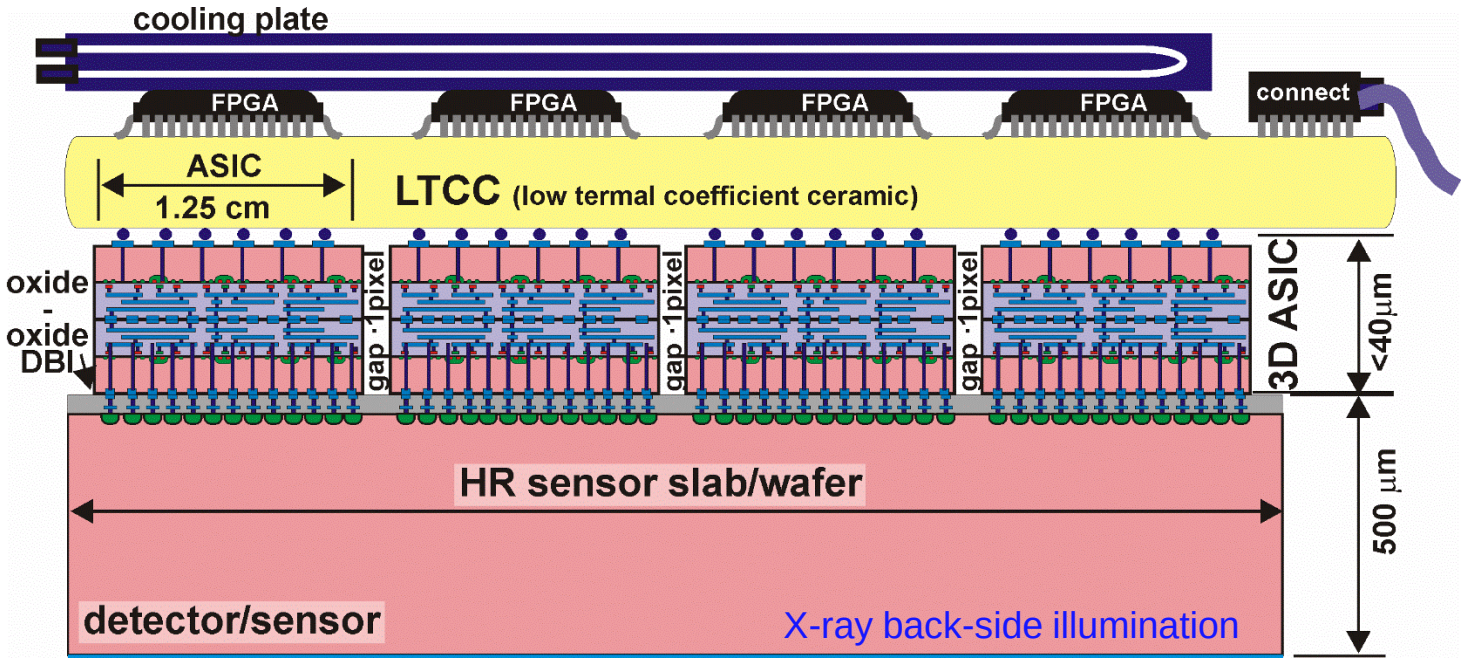
Good capacitance (~ 8 fF) and resistance properties (~ 0.3 Ohm) were demonstrated on the B-TSV pilot run

Fermilab

Level of defective B-TSV on the order of 10^{-5} is satisfactory.

Contacts to pads contain arrays of B-TSVs, small number of defective pixels is acceptable, design of vertically integrated memory needs to allow skipping locations/reorganization

From VIPIC1 to VIPIC-Large: 1Mpixel XCS Detector



- Features:

Ultimate GOAL: to build a single module 3D camera with minimal gap

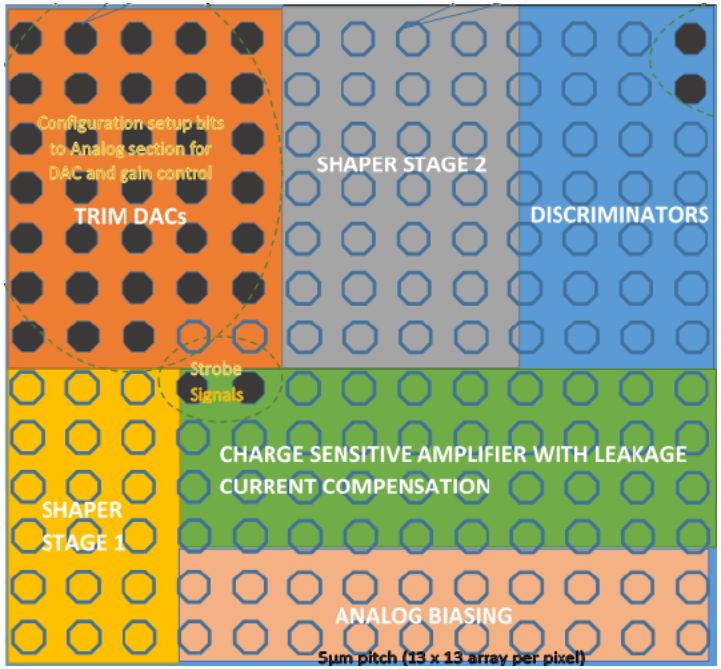
  - 1Mpixel = 3 shingles of 6 × 2 or straight 7 × 7 VIPICs-L LTD-bonded (D2W) to a sensor wafer
  - No dead edges, no peripheral circuitry on the ASIC
  - 65 μm - pitch square pixel, 36,864 pixels/chip grouped in indiv. readout subchips of 1024 pixels
  - 1 FPGA per VIPIC-L for on the fly data processing (up to 0.7 Tbps of raw data produced)
  - Multi-layer (>20 routing layer LTCC) supports b-bonded detector structure
  - Flat back-side - friendly for mounting of a cooling plate

VIPIC-Large DOE BES detector project:
BNL-Fermilab-Argonne +AGH-UST

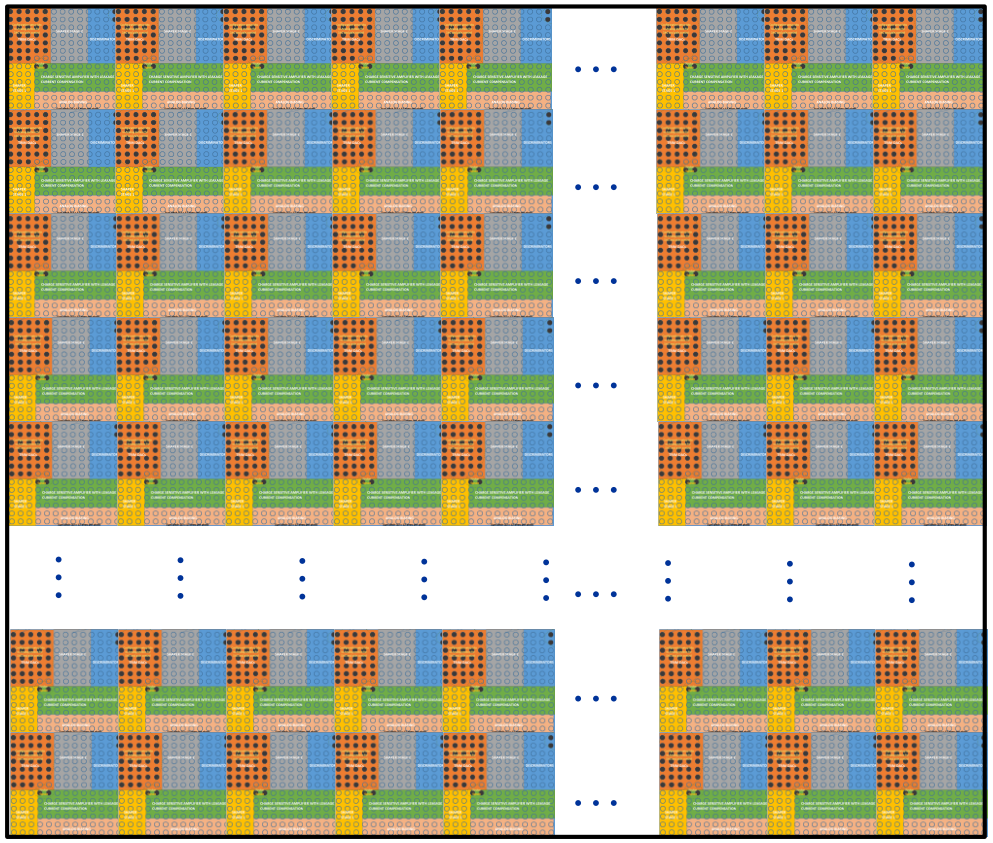
VIPIC-L: Design Highlights -2

VIPIC-L realizes new approach for entirely edgeless design – enabled by 2 tier 3D integration:

- array of pixels on the analog tier
- whole digital tier P&R-ed at once without respecting individual pixel boundaries



VPIC-L analog pixel $65 \times 65 \mu m^2$ with an array of octagonal metal dots forming analog-digital tiers bonding interface

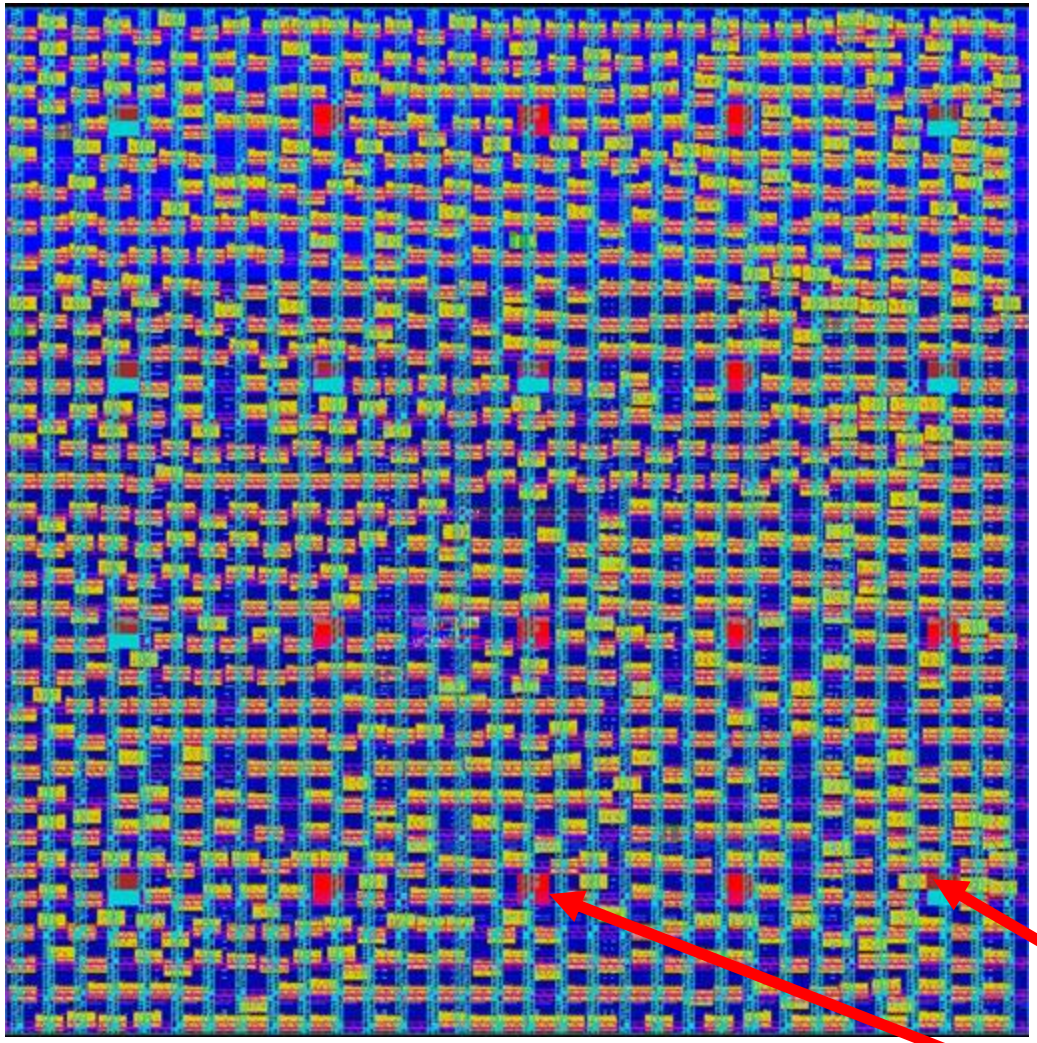


32×32 VIPIC-L analog pixels forming single analog tier subchip

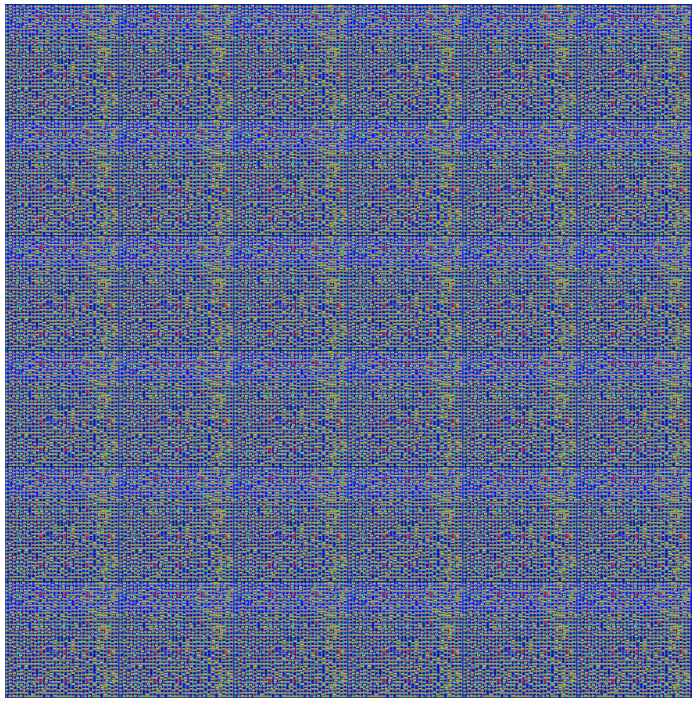
(6×6 subchips form one full analog tier chip)

VIPIC-L: Design Highlights - 3

Digital tier chip designed in 130nm process; next design is clearly 65nm or beyond



32 × 32 pixels VIPIC-L digital tier subchip with no explicit boundaries of pixels



VIPIC-L digital tier chip composed of 6 × 6 subchips and NO periphery

- pixel front-end logic blocks embedded in the digital sea of common logic (including the chip back-end)
- All pads are b-bonding pads on the back-side of the digital tier

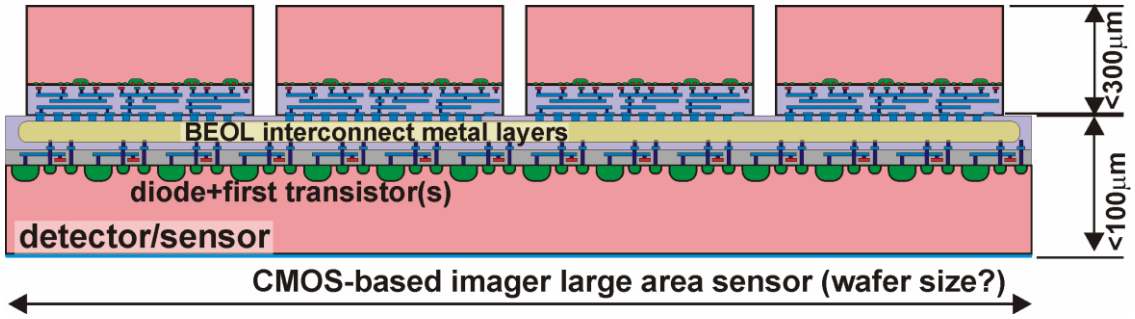
3D integration and CMOS sensors

A CMOS sensor for imaging or tracking) can be augmented by an additional layer of dedicated high performance electronics, 3D integrated at the pixel level.

The pixel in the CMOS sensor contains only minimal circuitry for the conversion of the charge packet into voltage or current right at the source of the signal; most functionality is located in the additional electronics layer.

FLORA: Fermilab-LCLS CMOS 3D-integRated with Autogain

2M pixel, soft 0.2-2 keV X-rays, high speed 10kfps, high dynamic range 10^3 camera for LCSL II, (Fermilab-SLAC, P.I. G. Carini, G. Deptuch))



Conclusions: the prospects of 3D vertically integrated pixels

- Demonstrators of 3D integrated devices are available and confirm the potential advantages of this technology, both for HEP and imaging applications. The pixel sensors and front-end electronics community will definitely continue to use 3D integration as a way of devising (and dreaming) advanced detectors.

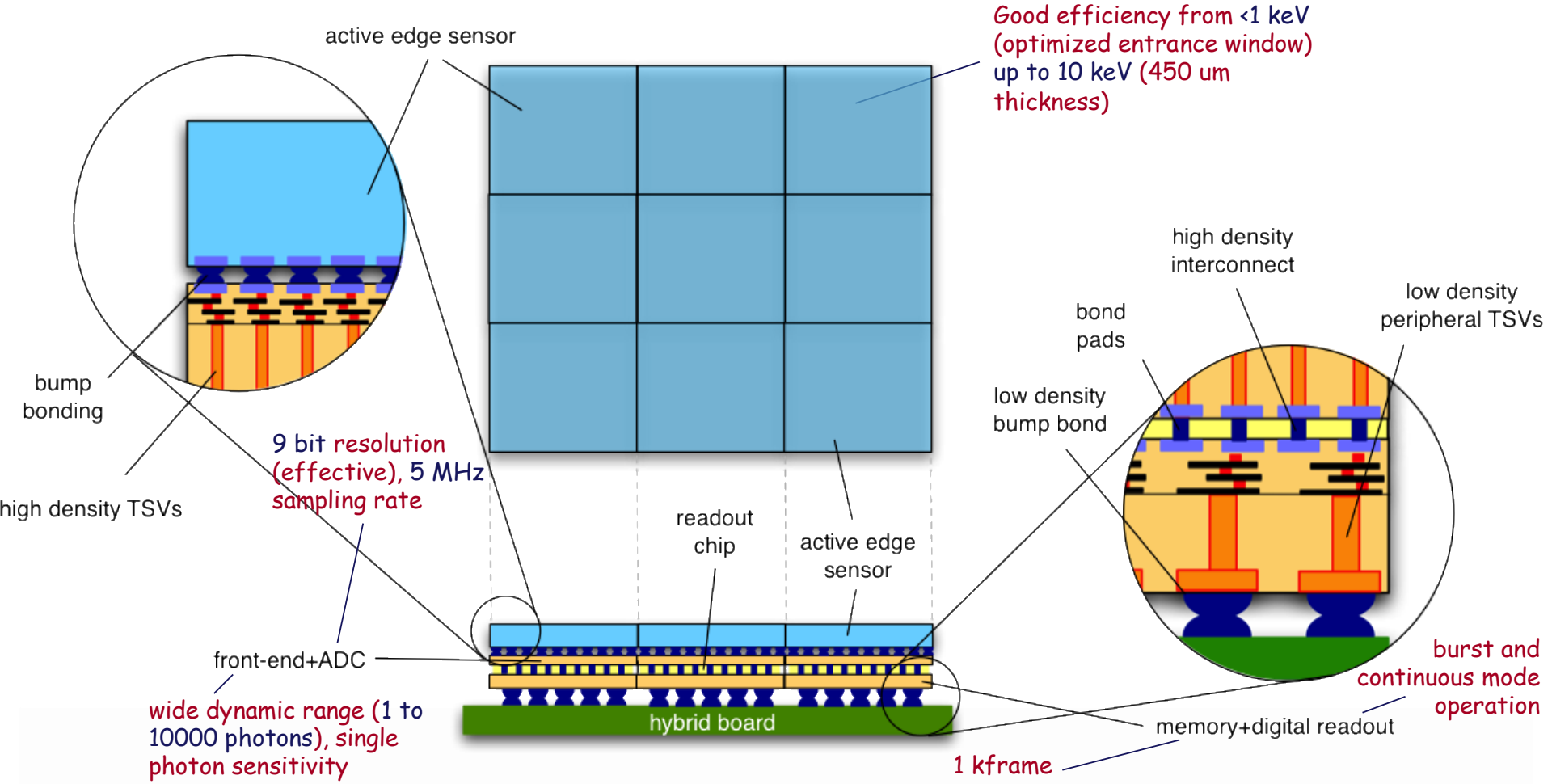
- Low-density large peripheral TSVs are going to be processed in 65 nm CMOS chips in the next future, as this process appears to have reached a good level of maturity

- Small size pixel-level TSVs will be a crucial ingredient to achieve the ultimate performance of the real 3D-IC technology. They may allow for the effective interconnection of an analog signal sensing and/or processing layer to a digital and memory layer, which could be even designed in an advanced CMOS process (beyond 65 nm)

The PIXFEL design of a pixel detector for FELs: small pixel level TSVs in a 65 nm pixel readout chip and peripheral TSVs in a digital memory layer

INFN Pavia, Pisa, Trento
P.I. Lodovico Ratti

- Higher functional density, larger memory capacity



Backup slides