ATLAS ITk Pixel detector

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on behalf of the ATLAS Collaboration

Vertex 2016
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ATLAS will have to cope with much harsher conditions, induced by both peak and integrated luminosity. **Staged** approach for calo, muons and trigger/DAQ using Phase-I intermediate upgrades, while the tracker will be completely replaced in LS3.

In the following I present the main challenges for the new tracker (**ITk**), **Pixel detector**, reporting on the preparation towards the Technical Design Report due for late 2017.
Limitations of the current tracker

- HL-LHC scenario implies significant scaling of the ID design parameters:
  - **Peak luminosity:** $5-7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ → $\sim x5-7$
  - **Average pile-up:** up to $<\mu> \sim 200$ → $\sim x8$
  - **Integrated luminosity:** 3000 fb$^{-1}$ → $\sim x10$
  - Requested **radiation hardness:** $2 \times 10^{16} \text{ n}_{\text{eq}}/\text{cm}^{2}$ → $x20$

- Requirements for the new tracker:
  - Similar or better performance than the ID in these harsher conditions.
In the last two years focus on finalizing the layout for the TDRs.

- It is important also to have the community behind it.

4 layouts under study different in pixel barrel and eta coverage.

- Strip TDR
- Layout decision
- Pixel TDR

**Timeline:**

- **2012 LoI**
- **Q4 2015 Step1.0**
- **Q2 2016 Step1.5**
- **Q4 2016 Step1.6**
- **Q1 2017 Step2.0**
- **Step3.0**
ITK Layouts under study

Strip layout and Pixel end-cap all the same. Changes only in the Pixel barrel.
ITK Layouts under study

Strip layout and Pixel end-cap all the same. Changes only in the Pixel barrel.

The layouts have:

- ✔ Pixel volume up to 345 mm radius; then strip to the edge of the solenoid
- ✔ 4 Strip Barrel layers + 2x6 EC disks
- ✔ 5 Pixel Barrel and 4 (or 3) Rings layers, surface ~14 m²
- ✔ η coverage up to 4.0 (or 3.2) with at least 9 space points
- ✔ Pixel innermost detector replaceable.
From ideas to layout:

- Sensors are designed to be “perpendicular” to the particles trajectories, reducing the material seen by the particles.
- “Tracklets” are reconstructed increasing the number of hits per layer.
Multiple options are available for inclined sensor supports.

- Layers may be joined in pairs: each stave would support two layers of pixel sensors, leading to increased stiffness.
- Thermal performance satisfy requirements.
Extended concept

✓ “Traditional” layout, either longitudinal or perpendicular to the beam:
  • Extended long innermost barrel so that the cluster size may allow to reconstruct tracklets.
  • Critical aspects:
    • Cluster size robustness vs broken clusters;
    • Use this information in the track seeding and reconstruction.
Extended implementation

☑ Extended layouts joins pairs of pixel layers with support structure, for increased stiffness:
  • Default CO$_2$ cooling tube material is Titanium.
  • Also looking at carbon pipes for CO$_2$ cooling pipes, to reduce mass and radiation length of the staves.

I-beam

Carbon stave

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Pixel end-caps will consist of rings in four layers at different radius and z.
Stepping from Disks (ID and LoI) to Rings allows for much more flexibility in space points coverage.

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Forward region

- Pixel end-caps will consist of rings in four layers at different radius and z.
- Stepping from Disks (ID and LoI) to Rings allows for much more flexibility in space points coverage.

- Each ring consists of a carbon core containing cooling and electrical services. Each ring is built out of two half-rings, for ease of construction.
- Modules are mounted on both sides of each ring to allow overlap.
Expected performance

Work in progress!

✓ Preliminary results will be shown at ECFA meeting next week and will support the strip TDR.
Modules

- Baseline is the well understood hybrid pixel module concept
  - 50x50 or 25x100 µm² sensor, both compatible with 50x50 µm² electronics cell.
  - 3D and planar considered for innermost layers, planar in the other layers and disks
  - 1 or 2-chip modules (inner) and 4-chip modules (outer and disk)

- Modules components:
  - FE chip
  - Sensor: 3D, planar, CMOS
  - Interconnection
Readout chip

✓ Joint effort among CMS-ATLAS communities to deliver a large scale front-end ASIC prototype for Pixel-Phase 2 detectors.
✓ Full scale prototype RD53A will be submitted on March 2017:
  • 65nm design
  • Matrix of 400x192 pixels 50x50 um², ~2 cm²
✓ Two small 64x64 pixel matrix prototypes already finalized
  • FE65-P2 (Received on Dec 2015)
  • CHIPIX65 (Submitted July 2016)

✓ ATLAS chip: RD53B-ATLAS submission planned for Q1-2018
  • Considered the possibility for two iterations in the schedule
✓ Deal with trigger schema for ATLAS to be finalized within 2016 (two hardware triggers: L0 2-4 MHz in 2 µs, L1 0.6 MHz with Track trigger input 25 µs in total)
  • Outer pixel: readable at L0 rate → usable by Track trigger
  • Inner pixel: L0 for fast clear & 600 kHz L1 for readout
✓ Electrical transmission over 5-7 m, 5 Gb/s looks possible.
✔ 3D technology has been proven to be reliable with the IBL detector, and more recently in AFP and PPS. It is the baseline for the innermost layers, thanks to excellent radiation hardness at low operational voltages and moderate temperatures with low power dissipation.

\[ \varepsilon = 97\% \text{ at } 170V \text{ for fluence } 1 \times 10^{16} \text{ } n_{eq}/\text{cm}^2 \]

\text{power dissipation of } 11 \text{ mW/cm}^2 \text{ at } -25C
Sensors: 3D

The main challenges are the design of small cells and thinner substrate; production rate and yield should be regarded as critical issues.

- Columns of 5-8 µm diameter alternately n- and p-type doped
- Single sided process, thin 50-200 µm thick thanks to support wafers
- Slim edges of 15-150 µm, even active edges sensitive up to the physical edge
- Steady progress on 50 x 50 µm² & 25 x 100 µm² pixel design
- Sintef, FBK and CNM making devices: moving at RD53A-prototypes

Test with FEI4 50x250 µm² cell size, clustering is tricky!

Small pitch sensors, 230 µm thick:
Tested in TB before irradiation (eff = 97% for perp tracks) being tested now after irradiation.
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FBK

Small pitch sensors, 130 um thick:
Tested on TB in Aug.
Main challenges are **low cost for the outer radii** and radiation hardness, thermal runaway, material budget in the inner radii.

**Achievements:**

- Technology **n-on-p**
- Different vendors (Cis, Advacam, MPG-HLL, FBK, HPK, .. ) and interconnection technologies for thin planar pixel sensors investigated in a thickness range (50-200) µm.
- 50x50 µm² pixel test structures demonstrated

- Good hit efficiencies up to the physical perimeter of the devices obtained with (100-150) µm thin active edge sensors

- FE-I4 modules with 100 µm thin sensors found to deliver 97% hit efficiency at a fluence of at Φ=1x10¹⁶ n_eq/cm² for a moderate bias voltage of 500 V.
- 4-chip modules have been built and inter-chip distances, in the range of 180-280 mm, tested
- First RD53-P2 are in test; RD53A compatible sensors already produced.
Sensors: Planar

Main challenges are low cost for the outer radii and radiation hardness, thermal runaway, material budget in the inner radii.

Achievements:

- Technology n-on-p
- Different vendors (Cis, Advacam, MPG-HLL, FBK, hamamatsu) and interconnection technologies for thin planar pixel sensors investigated in a thickness range (50-200) µm.
- 50x50 µm² pixel test structures demonstrated.
- Good hit efficiencies up to the physical perimeter of the devices obtained with (100-150) µm thin active edges.
- FE-I4 modules with 100 µm thin sensors found to deliver 97% hit efficiency at a fluence of at $\Phi=1\times10^{16}$ n$_{eq}$/cm$^2$ for a moderate bias voltage of 500 V.
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Efficiency at $5\times10^{15}$ n$_{eq}$/cm$^2$ vs thickness:
The thinner sensor performs the best $\rightarrow$ 100 µm
Sensors: Planar

✓ Main challenges are low cost for the outer radii and radiation hardness, thermal runaway, material budget in the inner radii.

✓ Achievements:
  • Technology n-on-p
  • Different vendors (Cis, Advacam, MPG-HLL, FBK, Hamamatsu) and interconnection technologies for thin planar pixel sensors investigated in a thickness range (50-200) µm.
  • 50x50 µm$^2$ pixel test structures demonstrated
  • Good hit efficiencies up to the physical perimeter of the devices obtained with (100-150) µm thin active edges sensors
  • FE-I4 modules with 100 µm thin sensors found to deliver 97% hit efficiency at a fluence of at $\Phi=1\times10^{16}$ n$_{eq}$/cm$^2$ for a moderate bias voltage of 500 V.
  • 4-chip modules have been built and inter-chip distances, in the range of 180-280 mm, tested
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Efficiency at $5\times10^{15}$ n$_{eq}$/cm$^2$

Efficiency vs thickness: The thinner the best are the performance

Efficiency for 100 µm vs fluence:
Significant lower efficiency at 200-300 V; similar 97% at 500 V.

Power dissipation in 25-45 mW/cm$^2$ in 500-700 V range


**Sensors: Planar**

- Main challenges are low cost for the outer radii and radiation hardness, thermal runaway, material budget in the inner radii.

- Achievements:
  - Technology n-on-p
  - Different vendors (Cis, Advacam, MPG-HLL, FBK, Hamamatsu) and interconnection technologies for thin planar pixel sensors investigated in a thickness range (50-200) µm.
  - 50 µm pixel test structures demonstrated.
  - Good hit efficiencies up to the physical perimeter of the devices obtained with (100-150) µm thin active edges sensors.
  - FE-I4 modules with 100 µm thin sensors found to deliver 97% hit efficiency at a fluence of Φ = 1x10^{16} n_{eq}/cm^2 for a moderate bias voltage of 500 V.
  - 4-chip modules have been built and inter-chip distances, in the range of 180-280 mm, tested.
  - First RD53-P2 are in test; RD53A compatible sensors already produced.

4-chip module in HPK
Interconnections

✓ Traditional bump bonding is the baseline. Still several challenges:
  • Minimum pitch 50 µm, but density X5 with respect to best achieved (IBL) on a relatively large chip surface (~4 cm²) and large wafer size (ROC 12”).

✔ High density tested with dummy chains so far on 6”
Interconnections

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  • Minimum pitch 50 um, but density X5 with respect to best achieved (IBL) on a relatively large chip surface (~4 cm²) and large wafer size (ROC 12”).
  • Low material in electronics and sensor mainly for the innermost layers.

Use Indium and thermo-compression at low T (Selex, HPK)

Thin ROIC bow during solder reflow process → Results in many open bumps

Thin electronics – 100 µm
Source scan (Selex)

Thin Electronics – 200 µm
Disconnected pixel map, due to ROIC bow during solder reflow at 260°C
Interconnections

- Traditional bump bonding is the baseline. Still several challenges:
  - Minimum pitch 50 um, but density X5 with respect to best achieved (IBL) on a relatively large chip surface (~4 cm²) and large wafer size (ROC 12").
  - Low material in electronics and sensor mainly for the innermost layers.

How to live with solder bumps and possible bow:

IZM: Temporary wafer bonding of thinned 150 um ROIC to thick glass support wafer. Laser debonding after flip-chip. Used for IBL.

Backside compensation layer to counteract bow from front side stack (HPK, CEA LETI)

- Stress Compensation Layer (SLC) applied on thinned wafer backside
- 100um ROIC +300 um sensor

- FEI4b bow with temperature
  - Offset due to SiN layer thickness change: 0.5 to 1 µm
  - Die Bow (µm)
  - Temperature (°C)
  - No SCL
  - SLC CL SiN C 0.5 µm/Ti/AISI 4 µm
  - SLC WL SiN C 0.3 µm/Ti/AISI 4 µm

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Interconnections

✓ Traditional bump bonding is the baseline. Still several challenges:
  • Minimum pitch 50 um, but density X5 with respect to best achieved (IBL) on a relatively large chip surface (~4 cm²) and large wafer size (ROC 12”).
  • Low material in electronics and sensor mainly for the innermost layers.
  • ~X7 production scale with respect to ATLAS Pixel detector

✓ Qualify several vendors with survey market and preproduction: 2017-2018.
✓ Also decouple bump deposition and flip-chip (we can partially do it in-house).
✓ Reduce cost and increase production speed. Exploring solutions:
  • UBM at sensor foundry (CIS, HPK, MICRON, ADVACAM …)
  • Chip to Wafer bonding → Requires TVSs
Interconnections: CMOS

Exploring evolution of the default module concept:

If a reliable solution will be available in time, it will be used in the outermost layer to minimize cost and production time.

Hybrid pixel with passive CMOS sensor

Hybrid pixel with active CMOS sensor

Fully monolithic
In the last two years focus on finalizing the layout for the TDRs.
- It is important also to have the community behind it.

4 layouts under study different in pixel barrel and eta coverage

Layout for the TDR: $\eta$ coverage, optimize (reduce) endcap, fix innermost layer radius, supports and material description.
ITk Pixel timeline: future

- Module production and loading: 32-36 months
- Start of module production depends on FE chip availability
Huge amount of work for the Pixel detector in all critical areas. Simulation now in good shape, will allow fast turnaround between technology and performance. Still several options open: some will be closed by the TDR (layout, higher eta coverage, number of pixel disks, supports). Many challenges still ahead:

- Readout chip design and production
- Sensor choice (cell size, thickness, technology) per layer
- Interconnect optimization for sensor and layer
- Trigger and data transmission

This is a huge pixel detector: need to develop a massive production approach!
**Sensors: Planar**

- Main challenges are low cost for the outer radii and radiation hardness, thermal runaway, material budget in the inner radii.

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  - 4-chip modules have been built and inter-chip distances, in the range of 180-280 mm, tested.
  - RD53A compatible sensors with SOI technology.
Main challenges are low cost for the outer radii and radiation hardness, thermal runaway, material budget in the inner radii.

Achievements:

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Data transmission and rates

- Preference to place optical conversion stages in a relatively accessible area, i.e. more than 5-9 m from the detector.
  - It means we need a low mass copper solution.
  - Several prototypes are under test, including controlled impedance flex lines, twisted pairs, micro-coaxial cables.

In the range 5-7 m, 5-6 Gb/s looks possible, provided error correction algorithms and pre-emphasis are used: design of TX section in the FE chip must be tuned for the specific transmission line in use.
$B$ field
**Sensors: 3D**

- **p-** high $\Omega$ cm wafer
- **p++** low $\Omega$ cm wafer
- Metal to be deposited after thinning
- Handle wafer to be thinned down

*FBK layout, NIMA 824 (2016) 386*