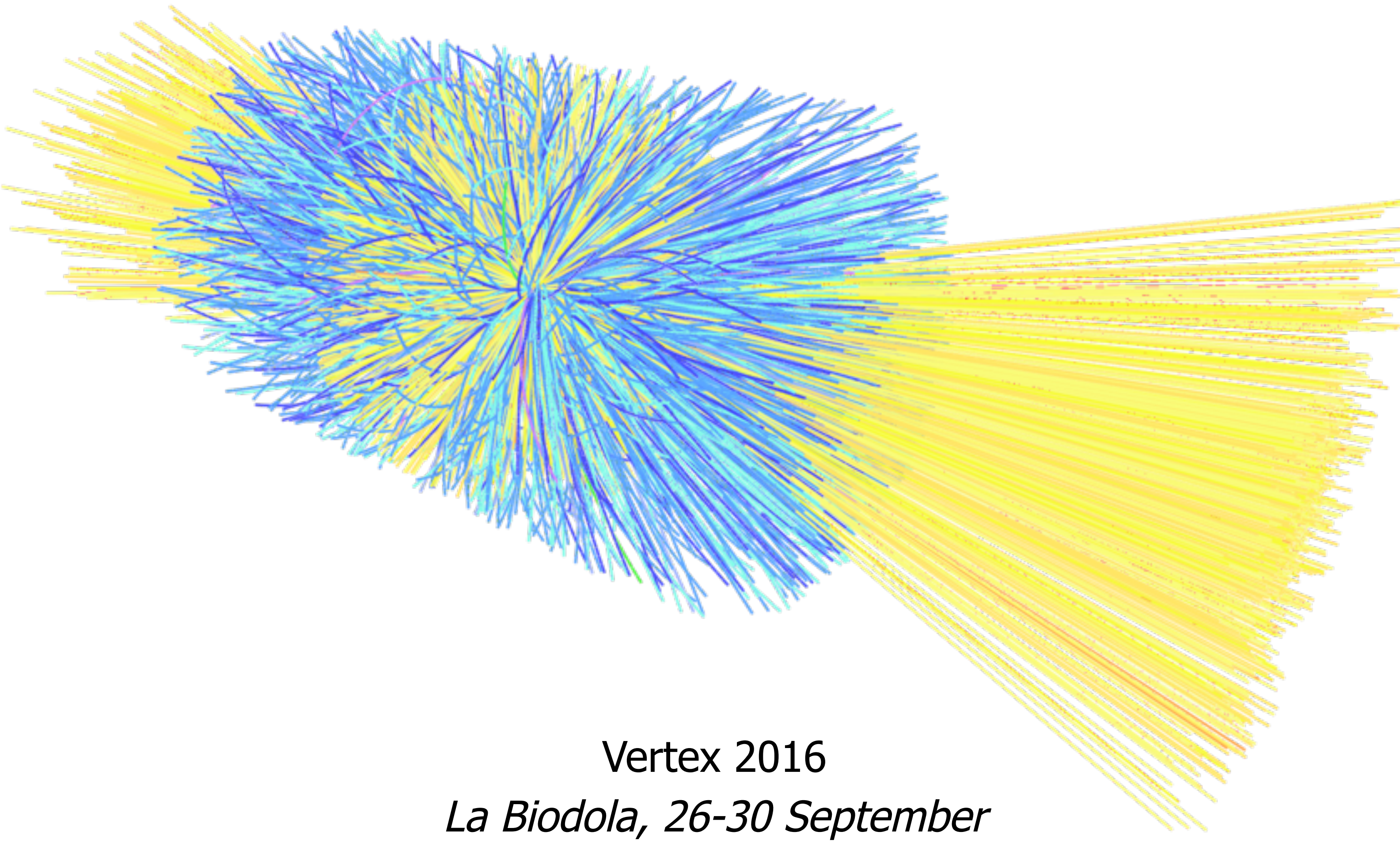
ATLAS ITk Pixel detector

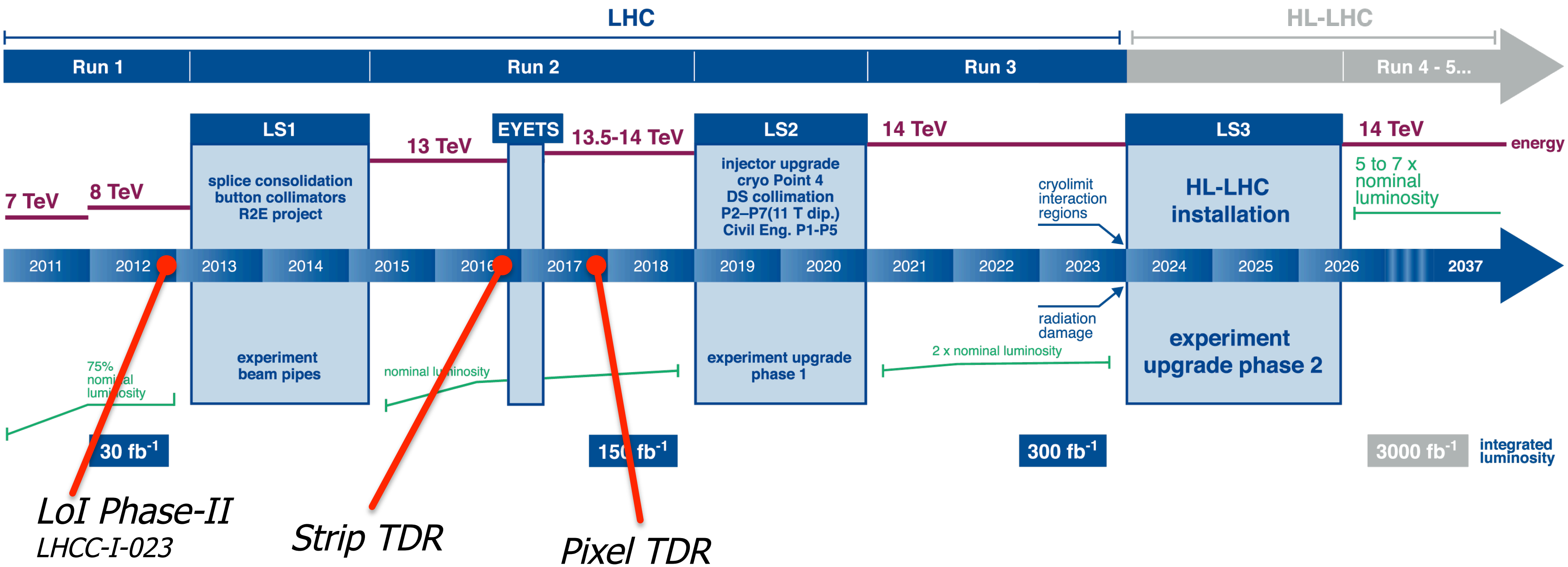
C. Gemme, INFN Genova
on behalf of the ATLAS Collaboration



Vertex 2016

La Biodola, 26-30 September

The High Luminosity LHC

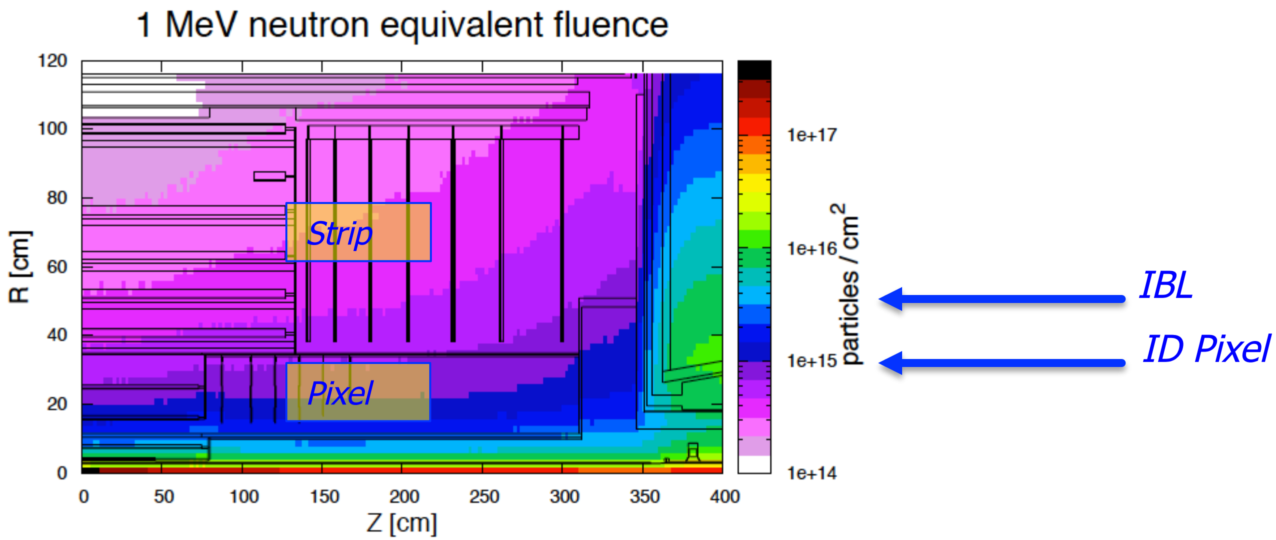


ATLAS will have to cope with much harsher conditions, induced by both peak and integrated luminosity. Staged approach for calo, muons and trigger/DAQ using Phase-I intermediate upgrades, while the tracker will be completely replaced in LS3.

In the following I present the main challenges for the new tracker (ITk) Pixel detector, reporting on the preparation towards the Technical Design Report due for late 2017.

Limitations of the current tracker

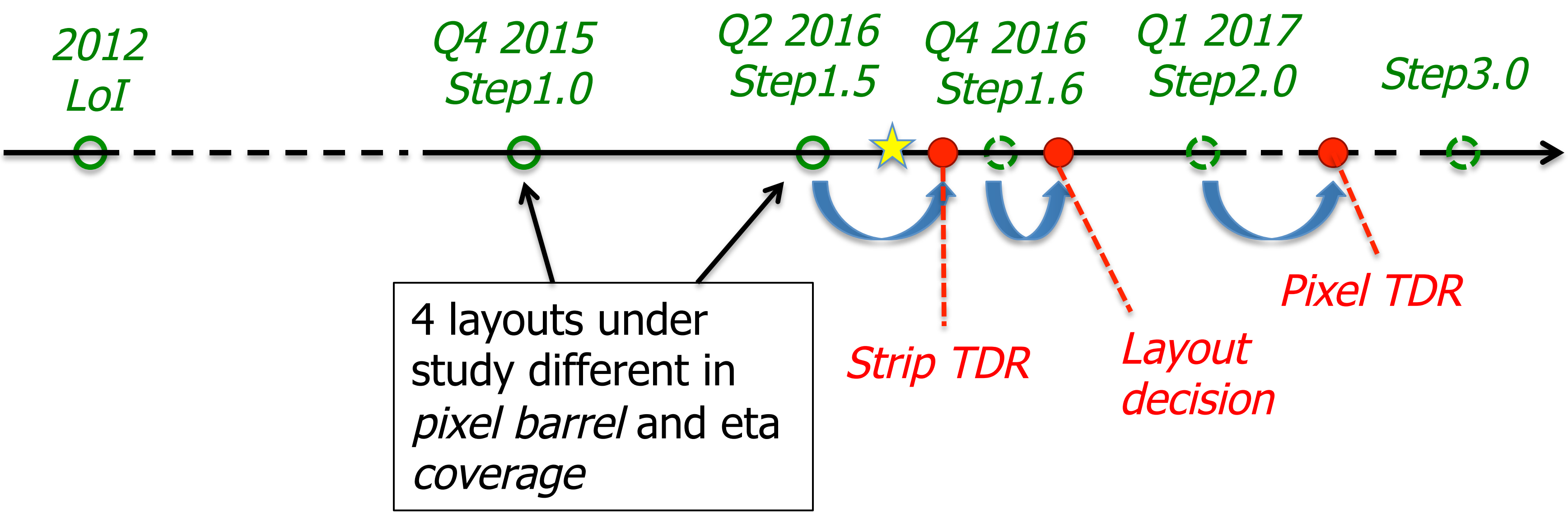
- HL-LHC scenario implies significant scaling of the ID design parameters:
  - *Peak luminosity:* 5-7 x 10^{34} $cm^{-2}s^{-1}$ → ~x5-7
  - *Average pile-up:* up to <μ> ~200 → ~x8
  - *Integrated luminosity:* 3000 fb^{-1} → ~x10
  - Requested *radiation hardness:* $2x10^{16}$ n_{eq}/cm^2 → x20



- Requirements for the new tracker:
  - Similar or better performance than the ID in these harsher conditions.

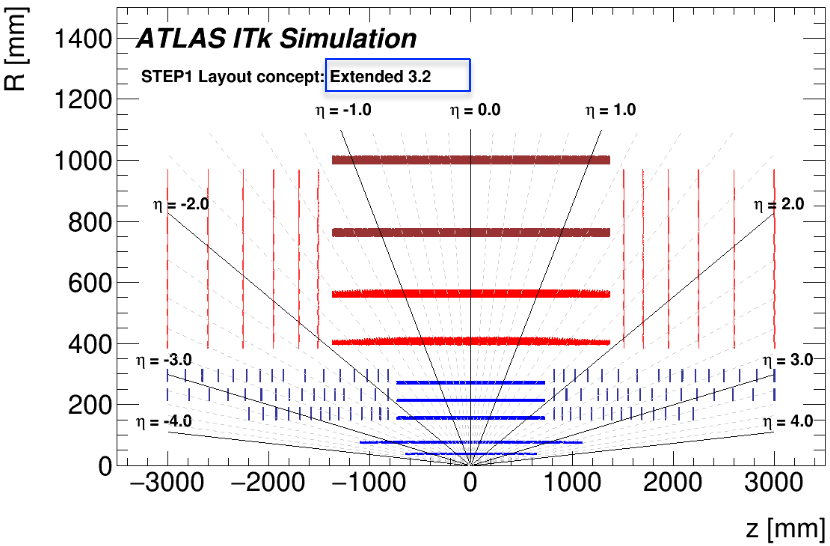
ITk Layout timeline

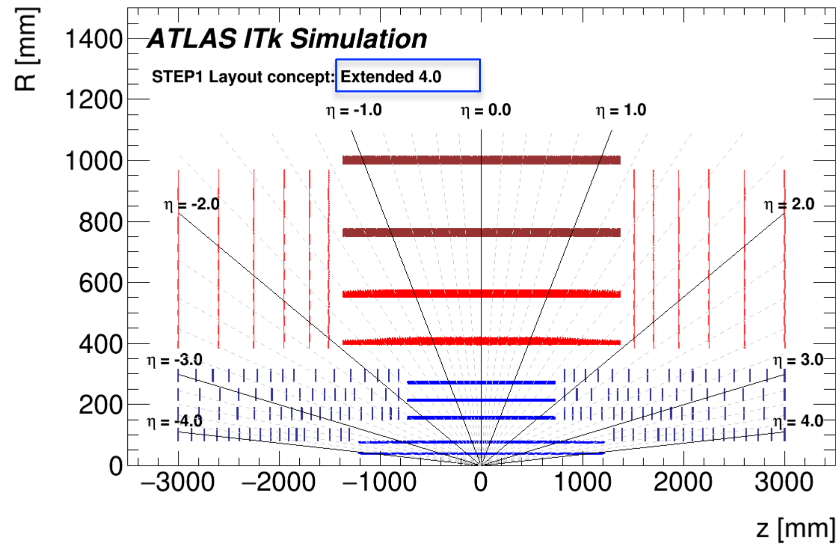
- ✓ In the last two years focus on finalizing the layout for the TDRs.
  - It is important also to have the community behind it.

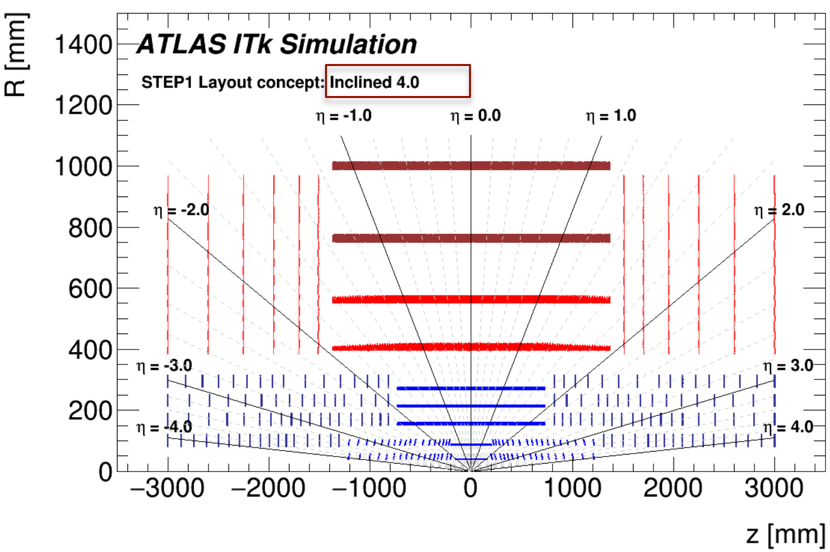


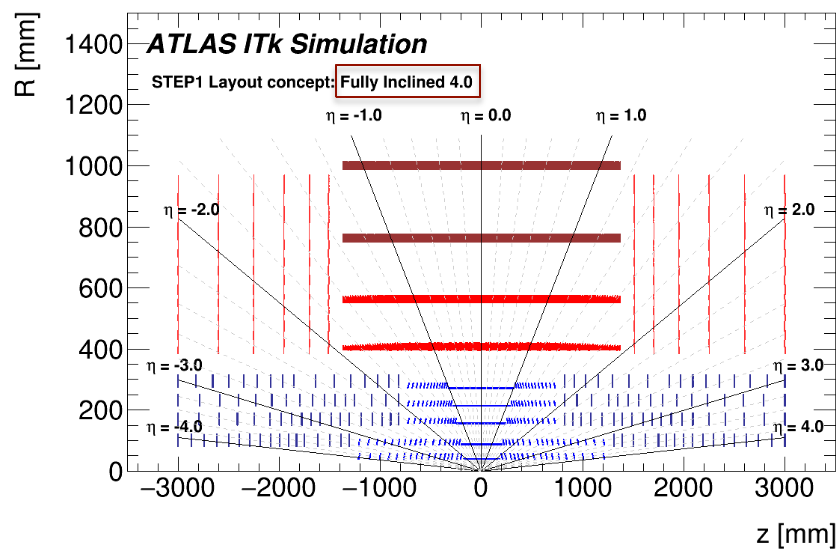
ITK Layouts under study

Strip layout and Pixel end-cap all the same. Changes only in the Pixel barrel.









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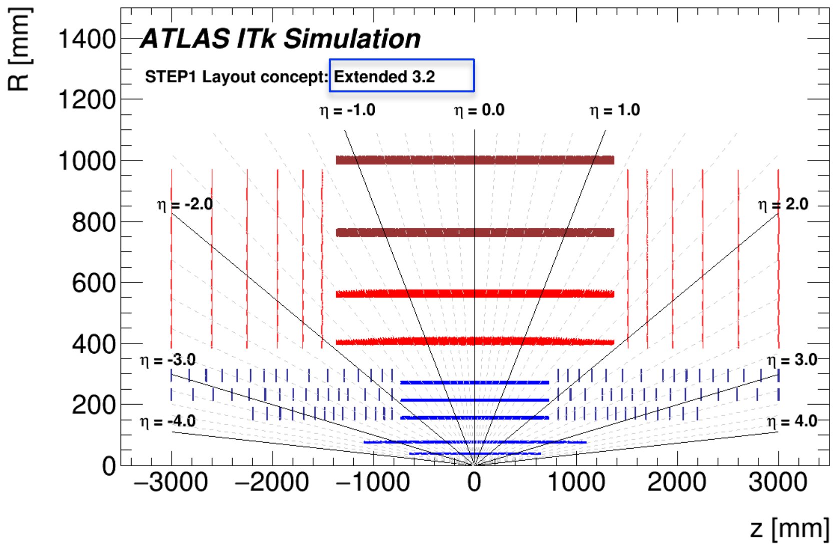
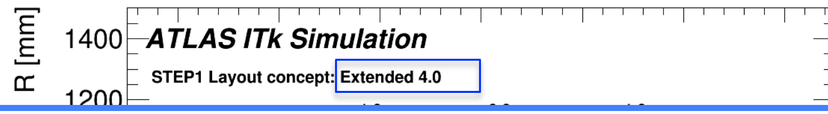
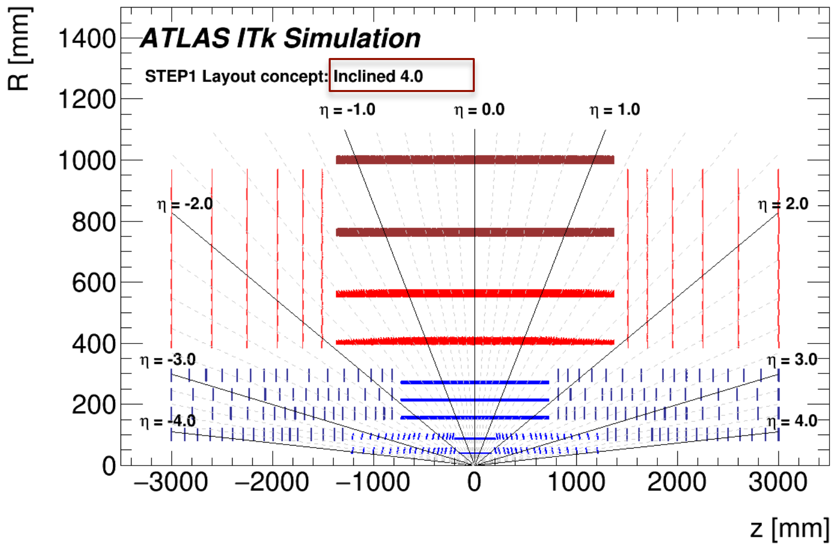






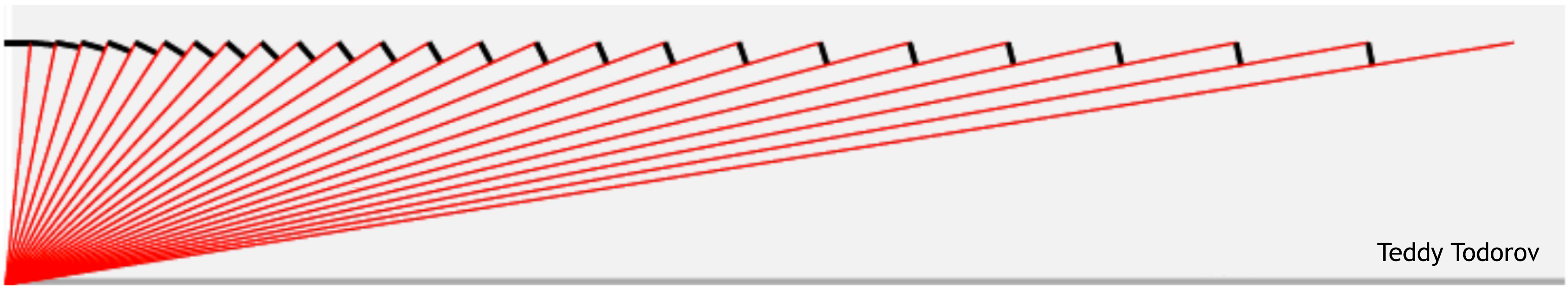
The layouts have:

- ✓ Pixel volume up to 345 mm radius; then strip to the edge of the solenoid
- ✓ 4 Strip Barrel layers + 2x6 EC disks
- ✓ 5 Pixel Barrel and 4 (or 3) Rings layers, surface ~14 m^2

Layer	Radius ID [mm]	Radius ITk [mm]
0	33.5	39
1	50.5	75
2	88.5	155
3	122.5	213
4	–	271

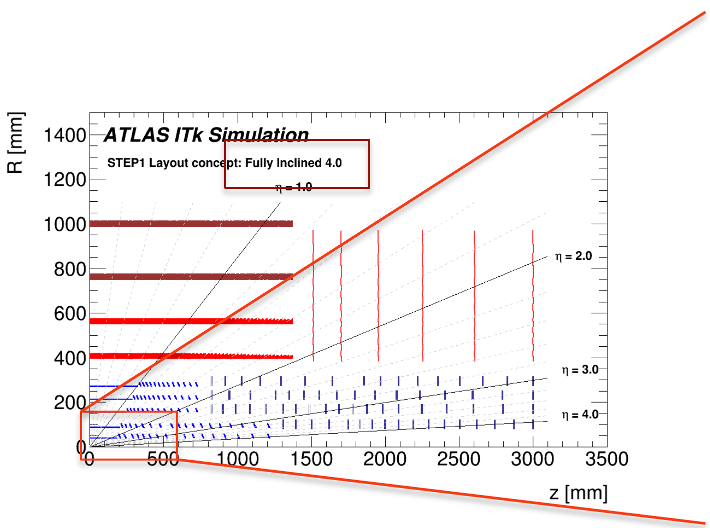
- ✓ η coverage up to 4.0 (or 3.2) with at least 9 space points
- ✓ Pixel innermost detector replaceable.

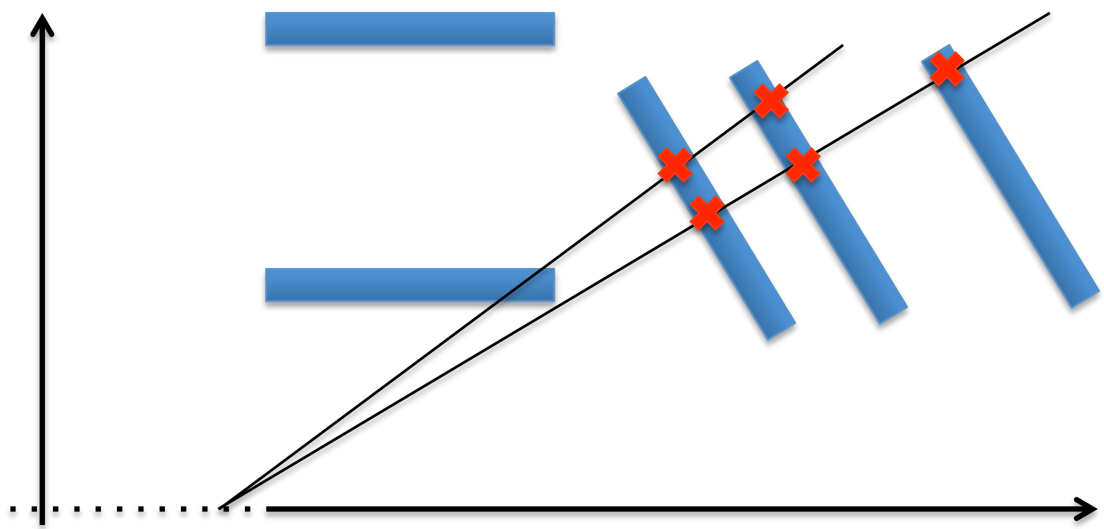
Inclined concept



✓ From ideas to layout:

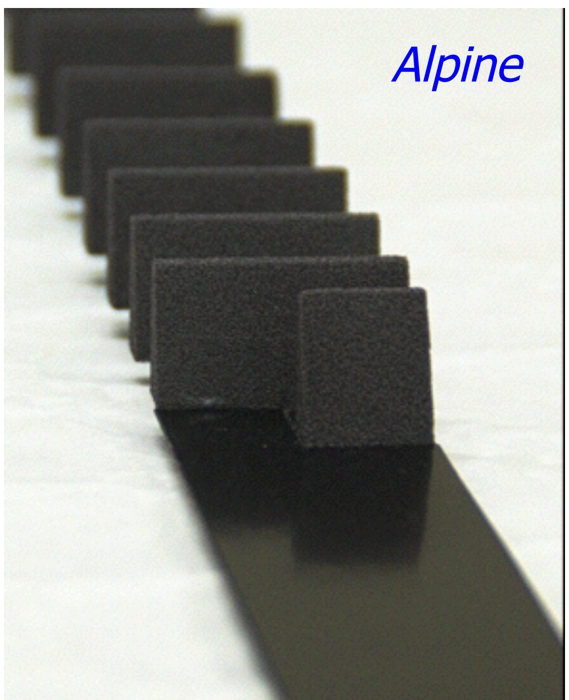
- Sensors are designed to be "perpendicular" to the particles trajectories, reducing the material seen by the particles.
- "Tracklets" are reconstructed increasing the number of hits per layer.

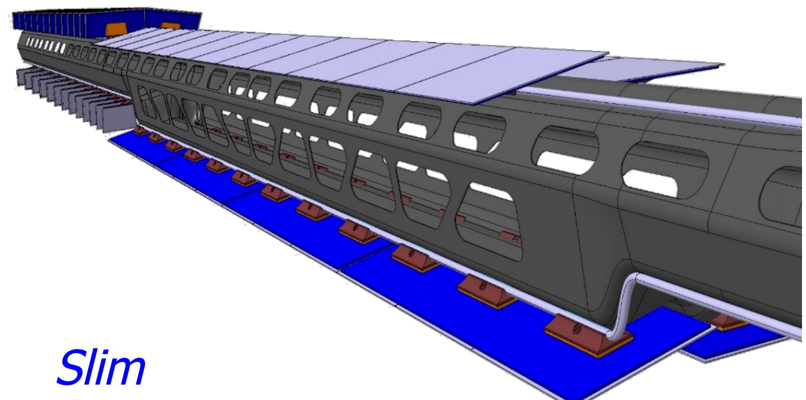




Inclined implementation

- ✓ Multiple options are available for inclined sensor supports.
  - Layers may be joined in pairs: each stave would support two layers of pixel sensors, leading to increased stiffness.
  - Thermal performance satisfy requirements.

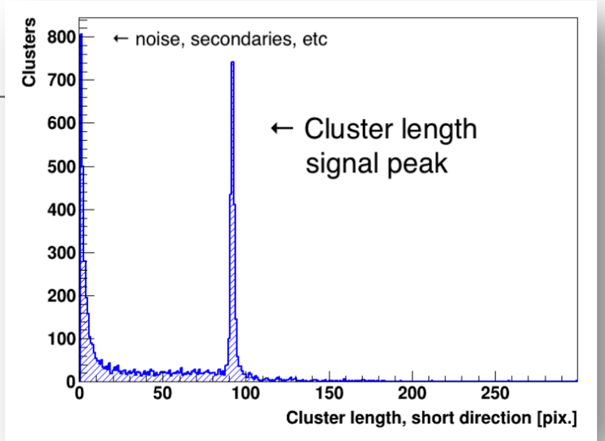


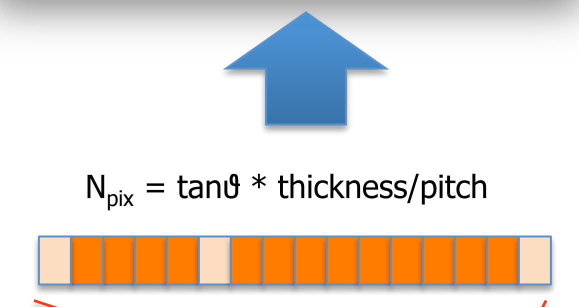


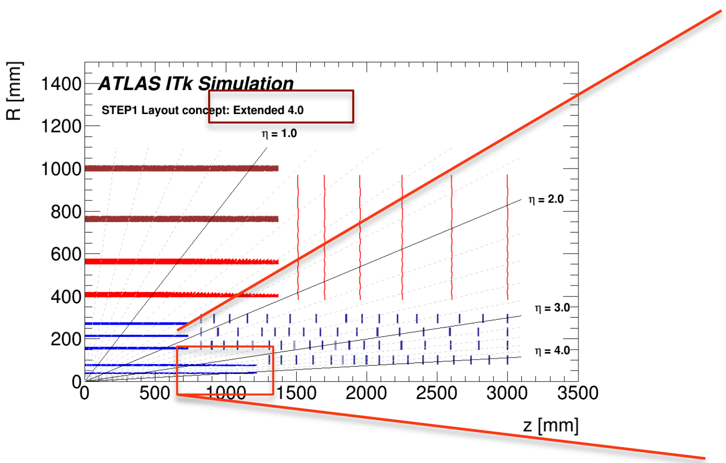
Slim

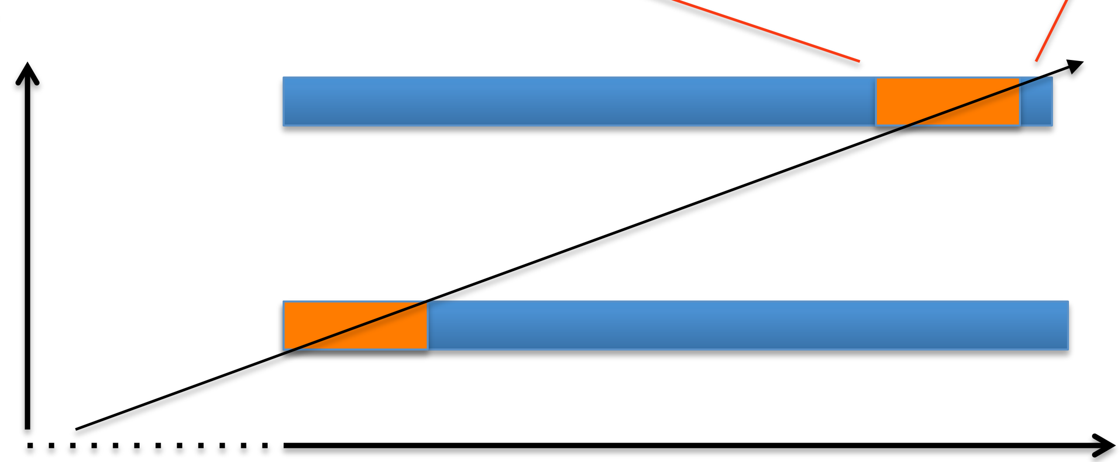
Extended concept

- ✓ “Traditional” layout, either longitudinal or perpendicular to the beam:
  - Extended long innermost barrel so that the cluster size may allow to reconstruct tracklets.
  - Critical aspects:
    - Cluster size robustness vs broken clusters;
    - Use this information in the track seeding and reconstruction.



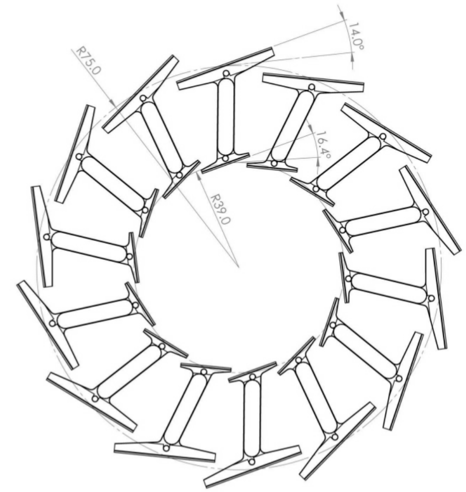


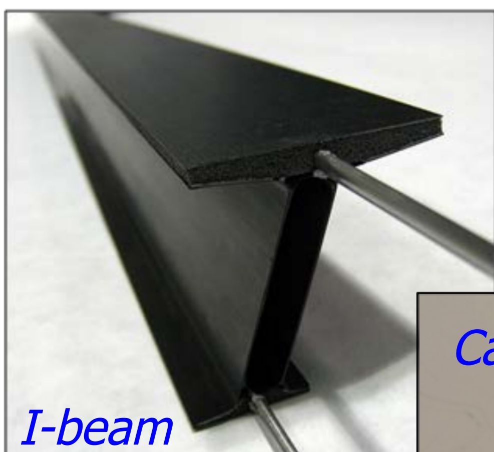


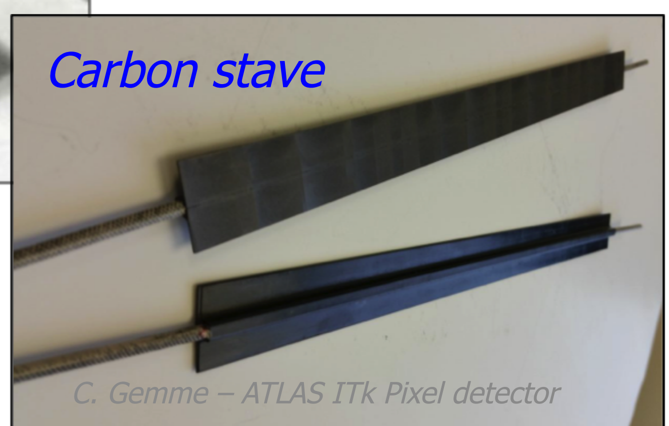


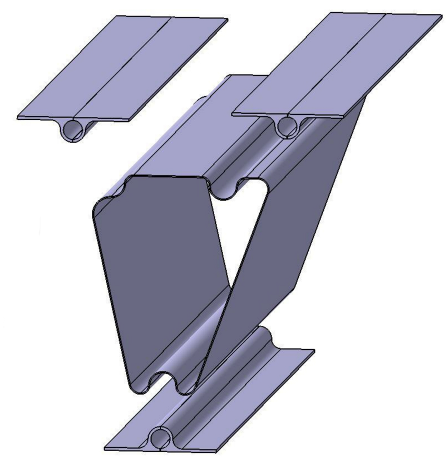
Extended implementation

- ✓ Extended layouts joins pairs of pixel layers with support structure, for increased stiffness:
    - Default CO_2 cooling tube material is Titanium.
    - Also looking at carbon pipes for CO_2 cooling pipes, to reduce mass and radiation length of the staves.



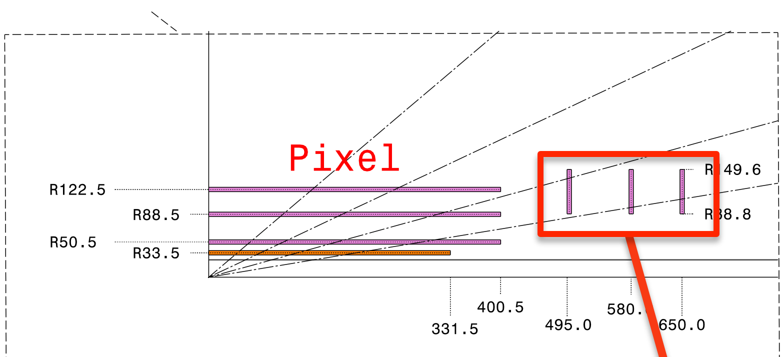


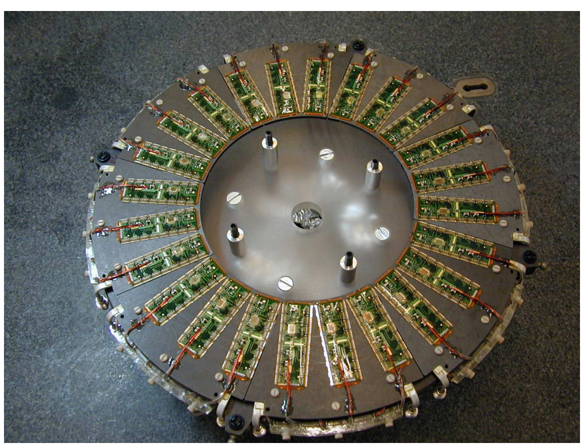


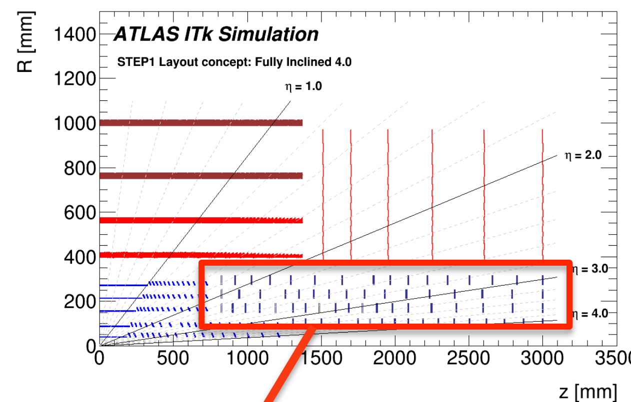


Forward region

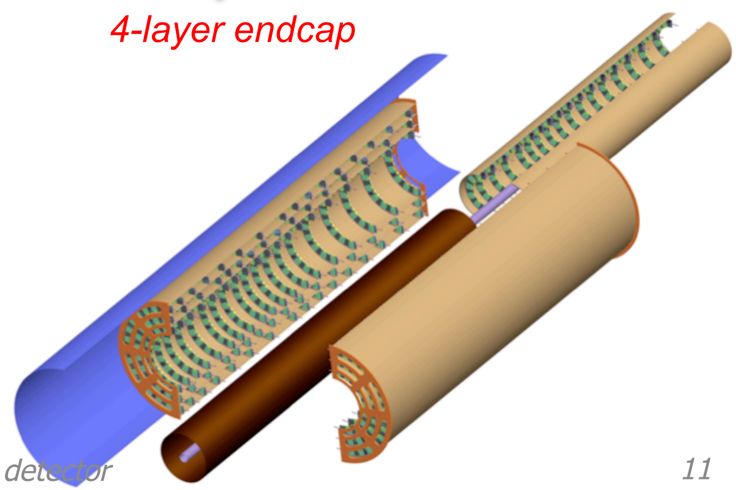
- ✓ Pixel end-caps will consist of rings in four layers at different radius and z.
- ✓ Stepping from Disks (ID and LoI) to Rings allows for much more flexibility in space points coverage







4-layer endcap



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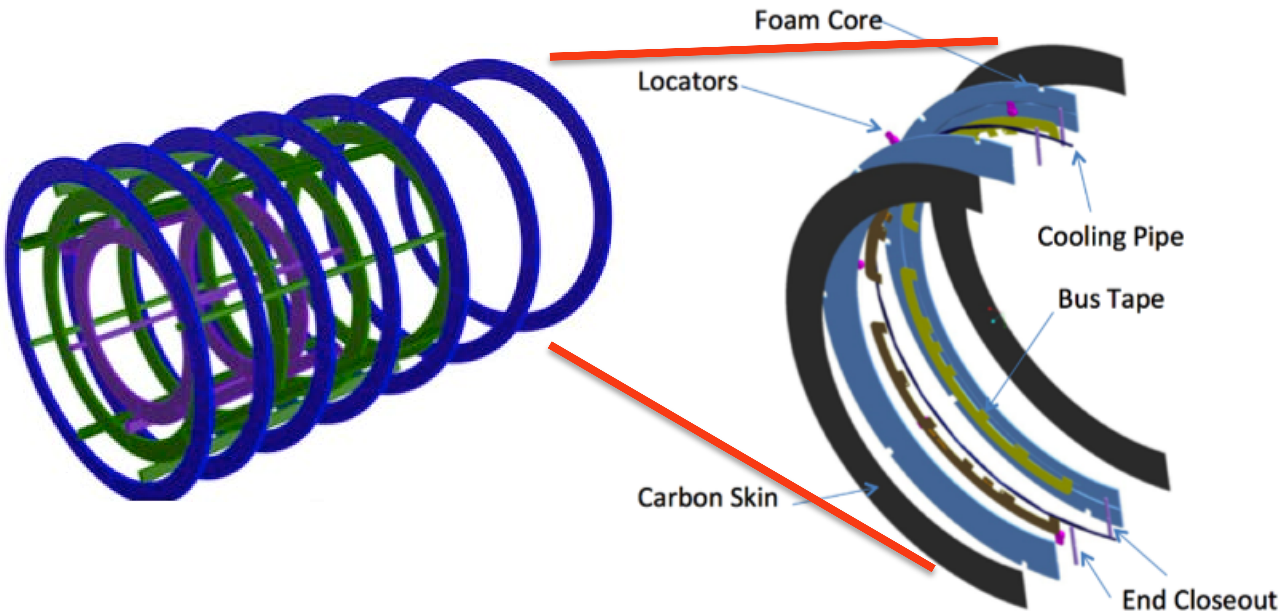
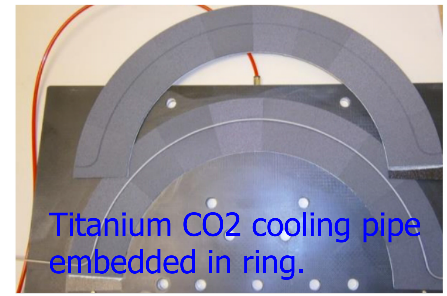
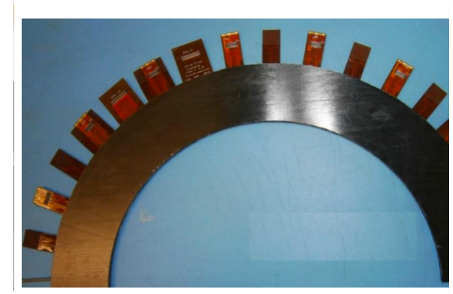






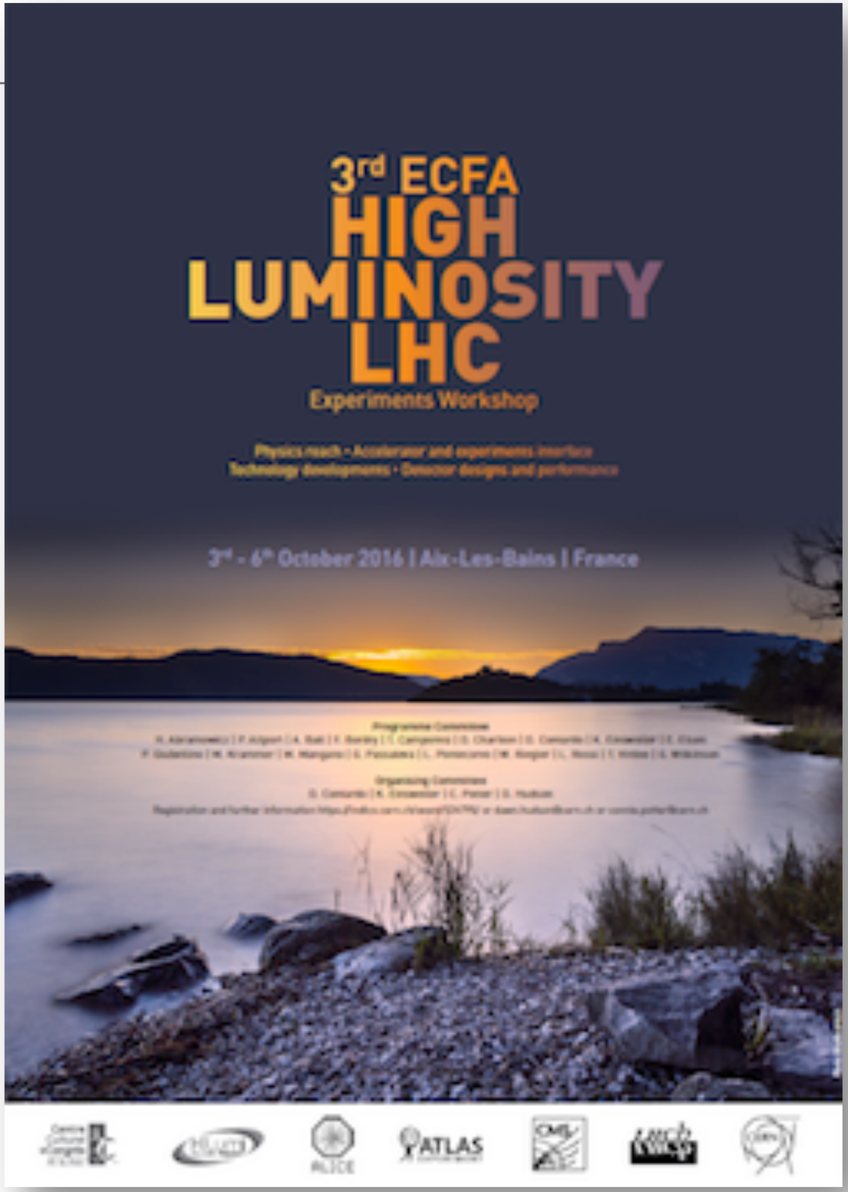
Electrical services (flex) embedded in ring.

- ✓ Each ring consists of a carbon core containing cooling and electrical services. Each ring is built out of two half-rings, for ease of construction.
- ✓ Modules are mounted on both sides of each ring to allow overlap.

Expected performance

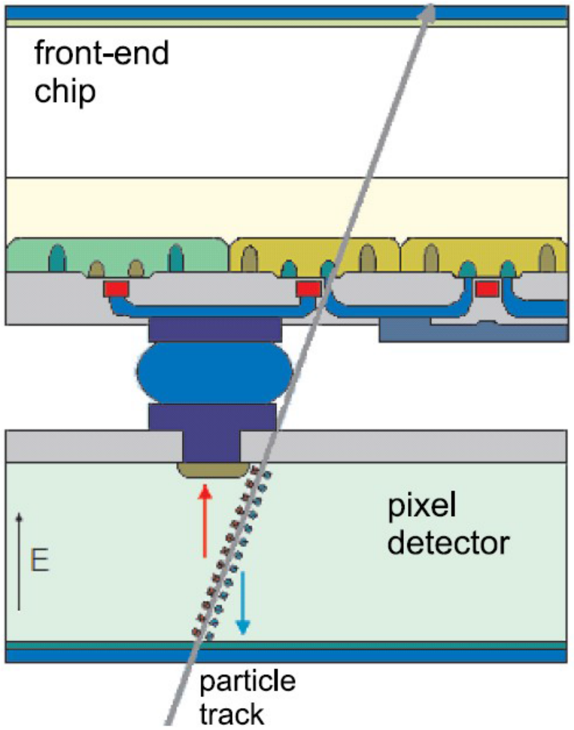
Work in progress!

- ✓ Preliminary results will be shown at ECFA meeting next week and will support the strip TDR.



Modules

- Baseline is the well understood hybrid pixel module concept
  - 50x50 or 25x100 μm^2 sensor, both compatible with 50x50 μm^2 electronics cell.
  - 3D and planar considered for innermost layers, planar in the other layers and disks
  - 1 or 2-chip modules (inner) and 4-chip modules (outer and disk)



- Modules components:
  - FE chip
  - Sensor: 3D, planar, CMOS
  - Interconnection

Readout chip

→ *Luigi Gaioni:*
RD53 Status and plans

- ✓ Joint effort among CMS-ATLAS communities to deliver a large scale front-end ASIC prototype for Pixel-Phase 2 detectors.
- ✓ Full scale prototype RD53A will be submitted on March 2017:
  - 65nm design
  - Matrix of 400x192 pixels 50x50 um^2, ~2 cm^2
- ✓ Two small 64x64 pixel matrix prototypes already finalized
  - FE65-P2 (Received on Dec 2015)
  - CHIPIX65 (Submitted July 2016)

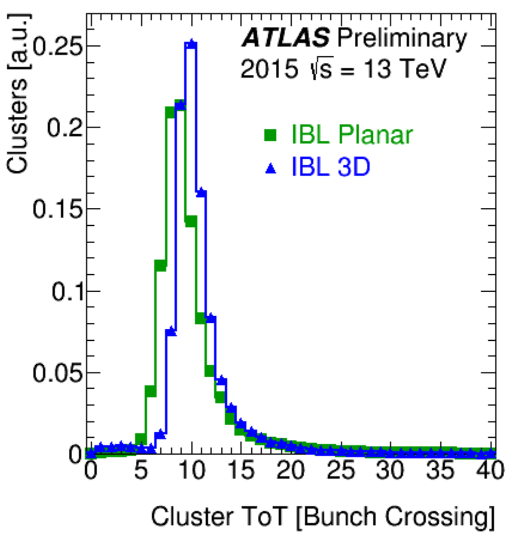
- ✓ ATLAS chip: RD53B-ATLAS submission planned for Q1-2018
  - Considered the possibility for two iterations in the schedule
- ✓ Deal with trigger schema for ATLAS to be finalized within 2016 (two hardware triggers: L0 2-4 MHz in 2 μs, L1 0.6 MHz with Track trigger input 25 μs in total)
  - Outer pixel: readable at L0 rate→ usable by Track trigger
  - Inner pixel: L0 for fast clear & 600 kHz L1 for readout
- ✓ Electrical transmission over 5-7 m, 5 Gb/s looks possible.

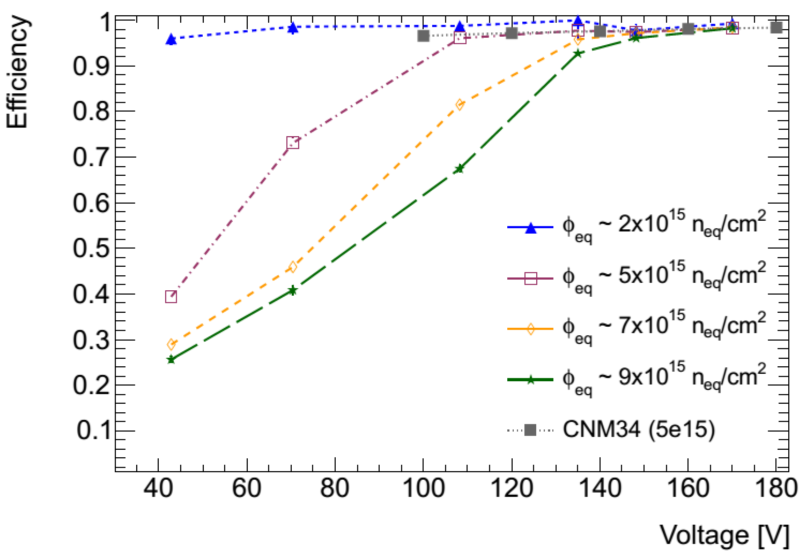
→ *Jahred Adelman:*
Track trigger in ATLAS at HL-LHC

Sensors: 3D

→ *Gianfranco Dalla Betta*
Small pitch 3D devices

✓ 3D technology has been proven to be reliable with the IBL detector, and more recently in AFP and PPS. It is the baseline for the innermost layers, thanks to excellent radiation hardness at low operational voltages and moderate temperatures with low power dissipation.





ε=97% at 170V for fluence 1x10^{16} n_{eq}/cm^2
*power dissipation of **11** mW/cm^2 at -25C*

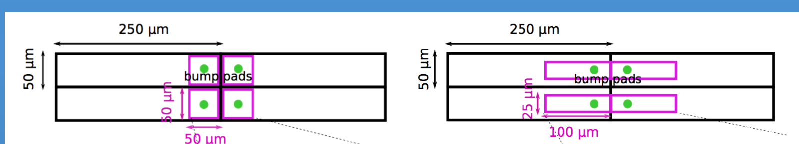
Sensors: 3D

→ *Gianfranco Dalla Betta*
Small pitch 3D devices

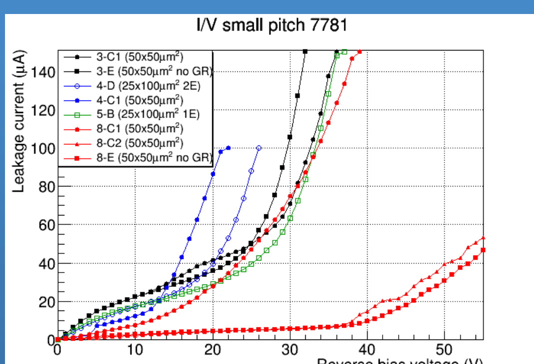
- The main challenges are the design of small cells and thinner substrate; production rate and yield should be regarded as critical issues.
  - Columns of 5-8 um diameter alternately n- and p-type doped
  - Single sided process, thin 50-200 μm thick thanks to support wafers
  - Slim edges of 15-150 μm, even active edges sensitive up to the physical edge
  - Steady progress on 50 x 50 μm^2 & 25 x 100 μm^2 pixel design
  - Sintef, FBK and CNM making devices: moving at RD53A-prototypes

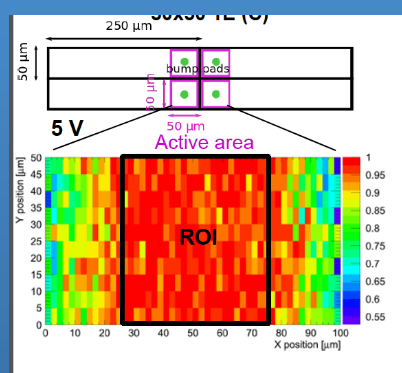
Test with FEI4 50x250 um^2 cell size, clustering is tricky!

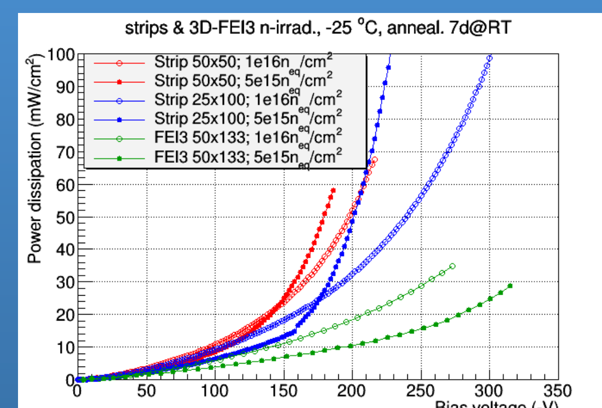
CNM



Small pitch sensors, 230 um thick:
Tested in TB before irradiation (eff = 97% for perp tracks)
being tested now after irradiation.







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- Steady progress on 50 x 50 μm^2 & 25 x 100 μm^2 pixel design
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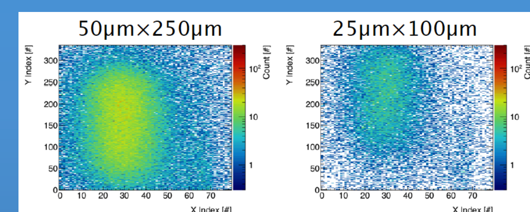
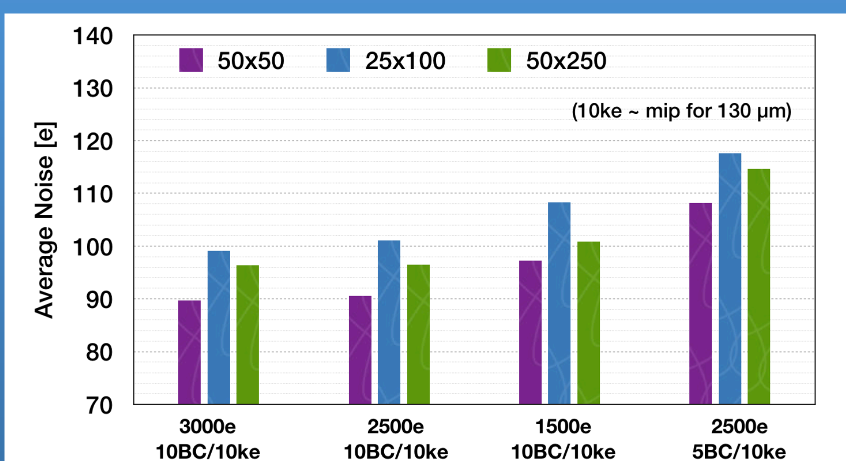
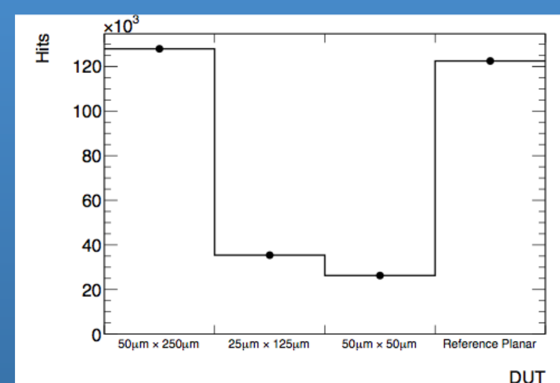
FBK

Small pitch sensors, 130 um thick:
Tested on TB in Aug.





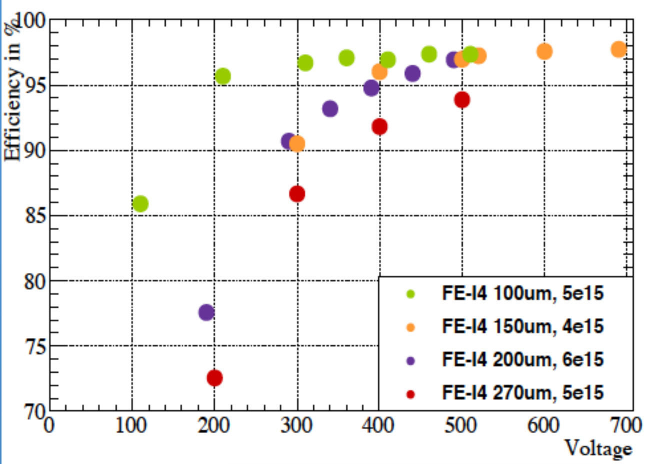


Sensors: Planar

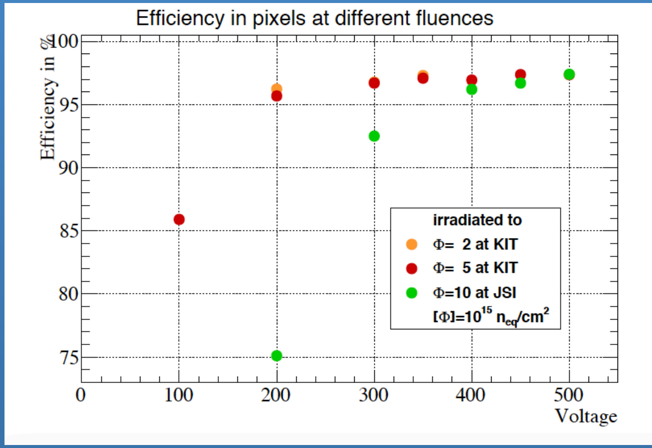
- ✓ Main challenges are low cost for the outer radii and radiation hardness, thermal runaway, material budget in the inner radii.
- ✓ Achievements:
  - Technology n-on-p
  - Different vendors (Cis, Advacam, MPG-HLL, FBK, HPK, ..) and interconnection technologies for thin planar pixel sensors investigated in a thickness range (50-200) µm.
  - 50x50 µm^2 pixel test structures demonstrated
  - Good hit efficiencies up to the physical perimeter of the devices obtained with (100-150) µm thin active edge sensors
  - FE-I4 modules with 100 µm thin sensors found to deliver 97% hit efficiency at a fluence of at $\Phi=1\times10^{16}$ n_{eq}/cm^2 for a moderate bias voltage of 500 V.
  - 4-chip modules have been built and inter-chip distances, in the range of 180-280 mm, tested
  - First RD53-P2 are in test; RD53A compatible sensors already produced.

Sensors: Pl

- ✓ Main challenges a hardness, thermal
- ✓ Achievements:
  - Technology n-or
  - Different vendor interconnection a thickness rang
  - 50x50 μm^2 pixel
  - Good hit efficier obtained with (1



Efficiency at 5x10^{15} n_{eq}/cm^2 vs thickness:
The thinner sensor performs the best → 100 um



Efficiency for 100 um vs fluence:
Significant lower efficiency at 200-300 V; similar 97% at 500 V.

  - FE-I4 modules with 100 μm thin sensors found to deliver 97% hit efficiency at a fluence of at $\Phi=1\times10^{16}$ n_{eq}/cm^2 for a moderate bias voltage of 500 V.
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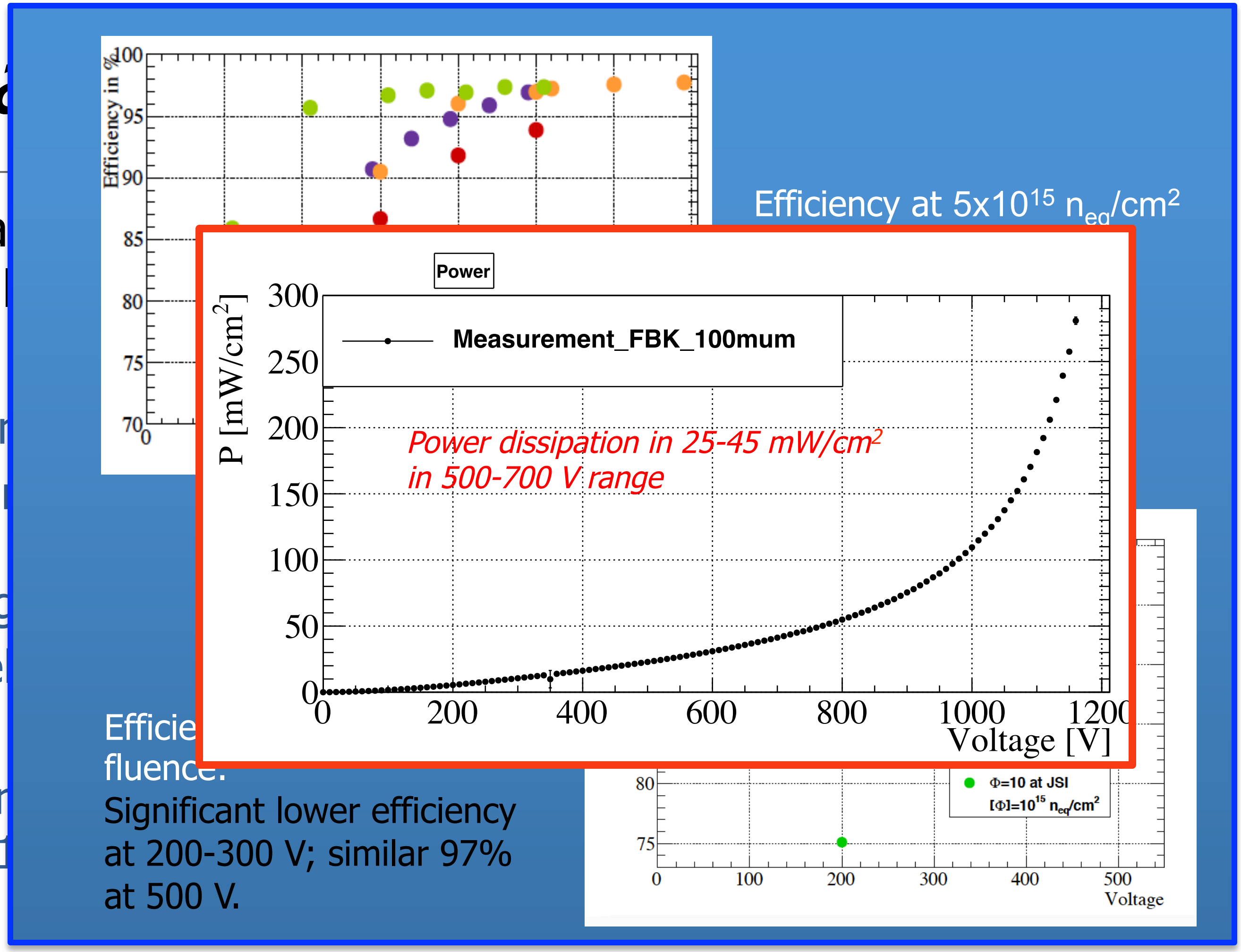

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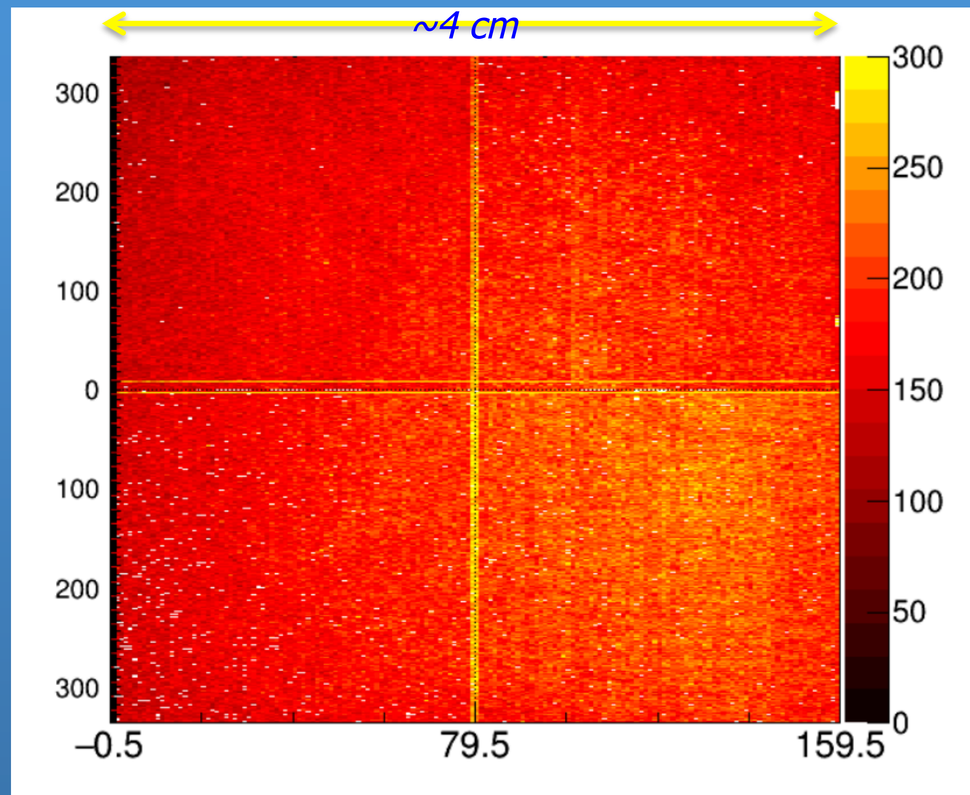


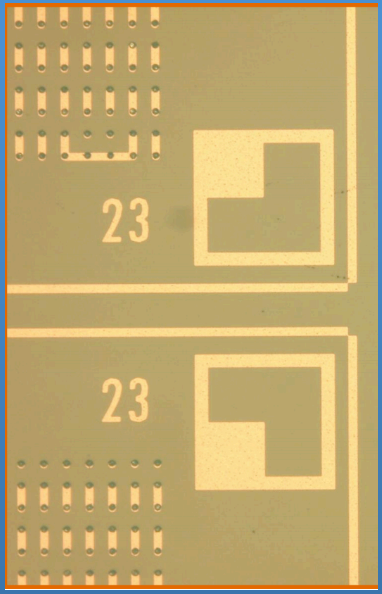
4-chip module in HPK

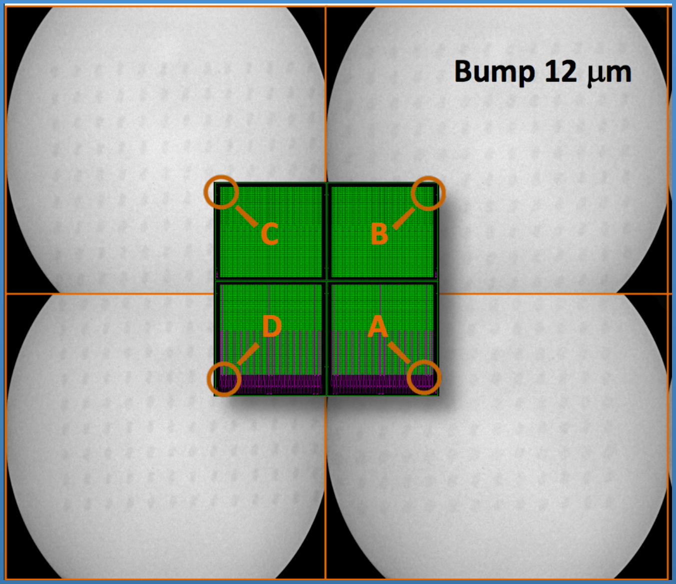
Interconnections

✓ Traditional bump bonding is the baseline. Still several challenges:

- Minimum pitch 50 um, but density X5 with respect to best achieved (IBL) on a relatively large chip surface (~4 cm^2) and large wafer size (ROC 12”).

✔ High density tested with dummy chains so far on 6” *Pub_PIXEL2016*





FBK wafer + Selex In bumps

Interconnections

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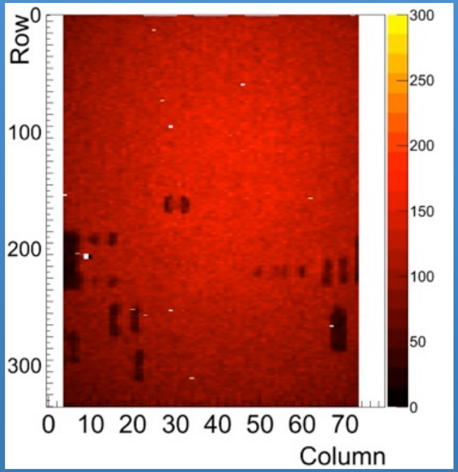
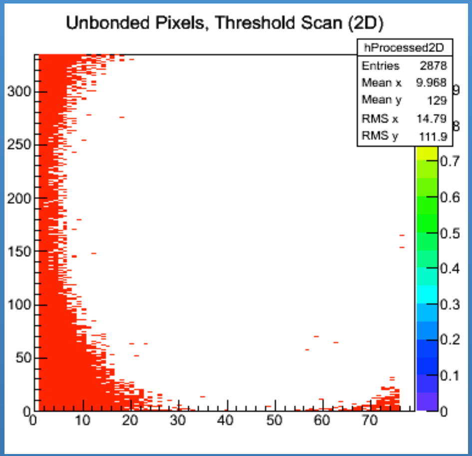
  - Minimum pitch 50 um, but density X5 with respect to best achieved (IBL) on a relatively large chip surface (~4 cm^2) and large wafer size (ROC 12”).
  - Low material in electronics and sensor mainly for the innermost layers.

Use Indium and thermo-compression at low T (Selex, HPK)



Thin electronics – 100 µm
Source scan (Selex)

Thin ROIC bow during solder reflow process → Results in many open bumps



Thin Electronics – 200 µm
Disconnected pixel map, due to ROIC bow during solder reflow at 260C

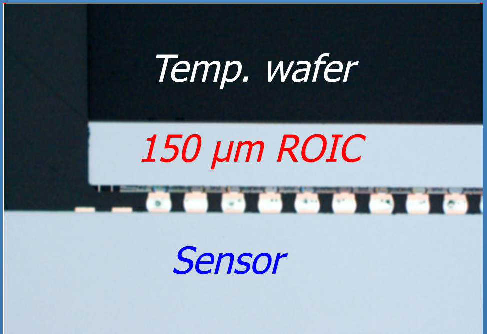
Interconnections

✓ Traditional bump bonding is the baseline. Still several challenges:

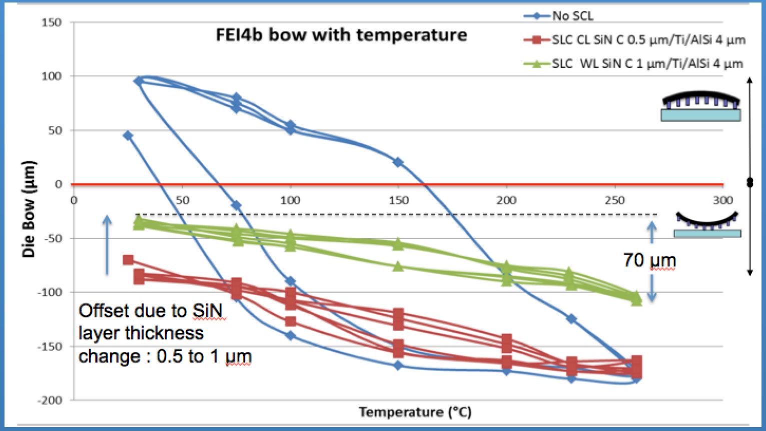
- Minimum pitch 50 um, but density X5 with respect to best achieved (IBL) on a relatively large chip surface (~4 cm^2) and large wafer size (ROC 12”).
- Low material in electronics and sensor mainly for the innermost layers.

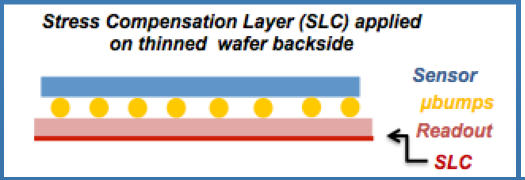
How to live with solder bumps and possible bow:

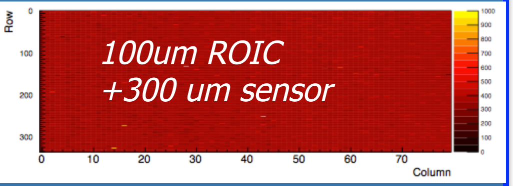
IZM: Temporary wafer bonding of thinned 150 um ROIC to thick glass support wafer. Laser debonding after flip-chip.
Used for IBL.



Backside compensation layer to counteract bow from front side stack (HPK, CEA LETI)







Interconnections

- ✓ Traditional bump bonding is the baseline. Still several challenges:
  - Minimum pitch 50 um, but density X5 with respect to best achieved (IBL) on a relatively large chip surface (~4 cm^2) and large wafer size (ROC 12”).
  - Low material in electronics and sensor mainly for the innermost layers.
  - ~X7 production scale with respect to ATLAS Pixel detector

✓*Qualify several vendors with survey market and preproduction: 2017-2018.*

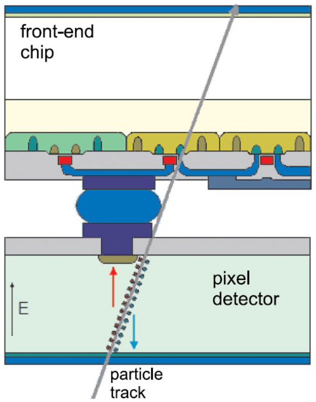
✓*Also decouple bump deposition and flip-chip (we can partially do it in-house).*

✓*Reduce cost and increase production speed. Exploring solutions:*

- UBM at sensor foundry (CIS, HPK, MICRON, ADVACAM …)
- Chip to Wafer bonding → Requires TVSs

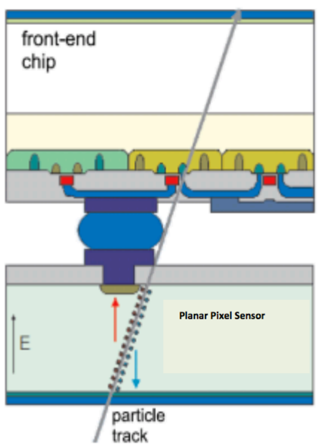
Interconnections: CMOS

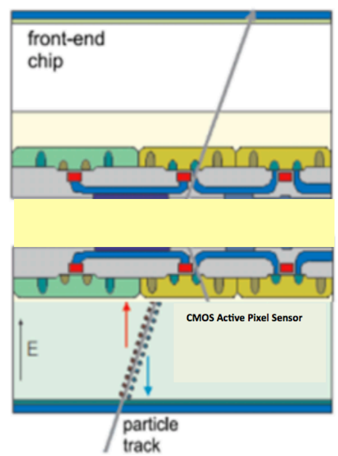
→ *F. Huegging talk*
CMOS Pixel development for HL-LHC

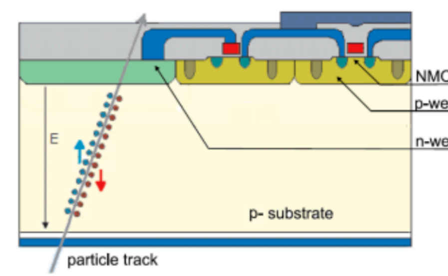


✓ Exploring evolution of the default module concept:

If a reliable solution will be available in time, it will be used in the outermost layer to minimize cost and production time.







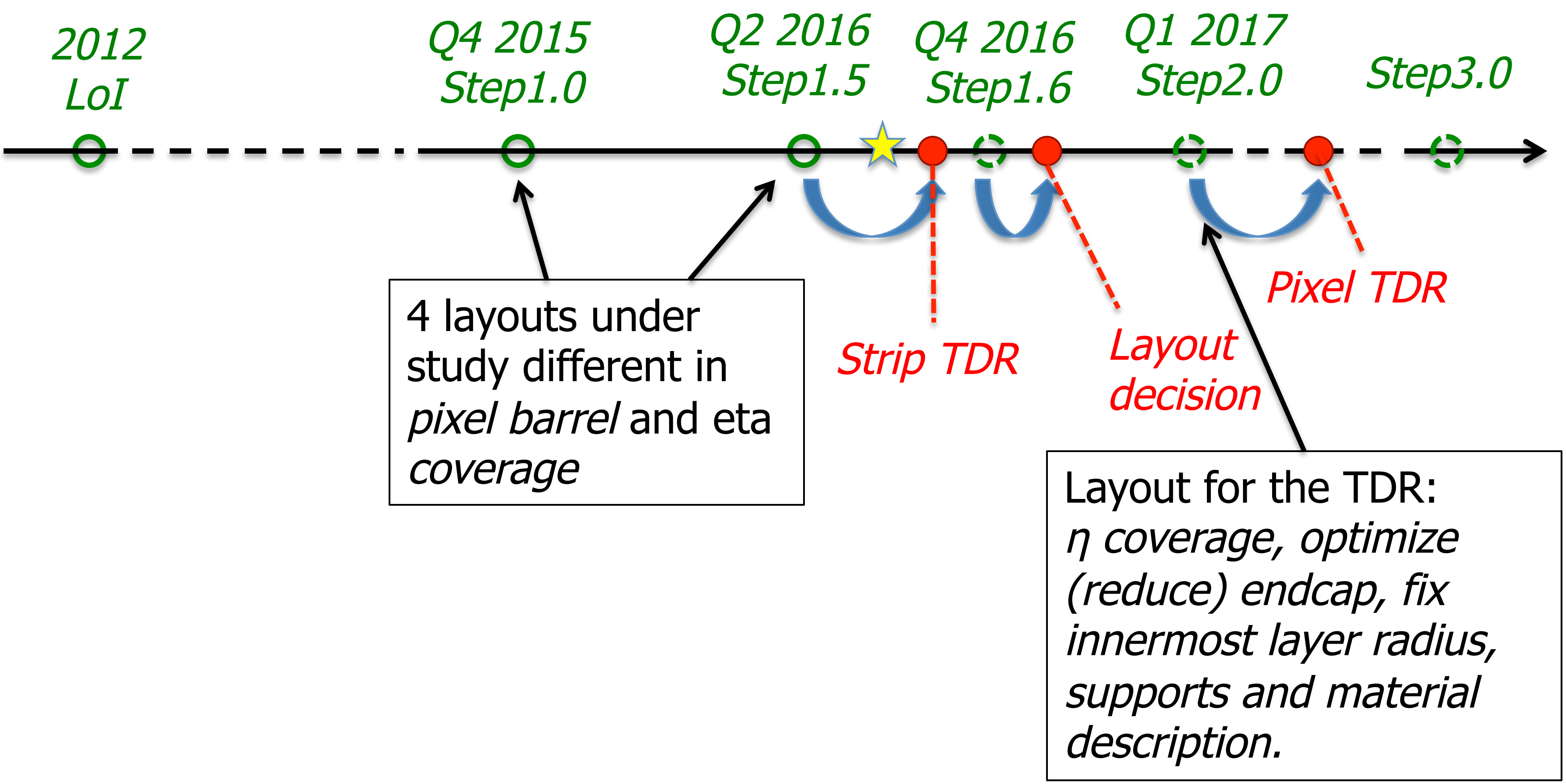
Hybrid pixel with passive CMOS sensor

Hybrid pixel with active CMOS sensor

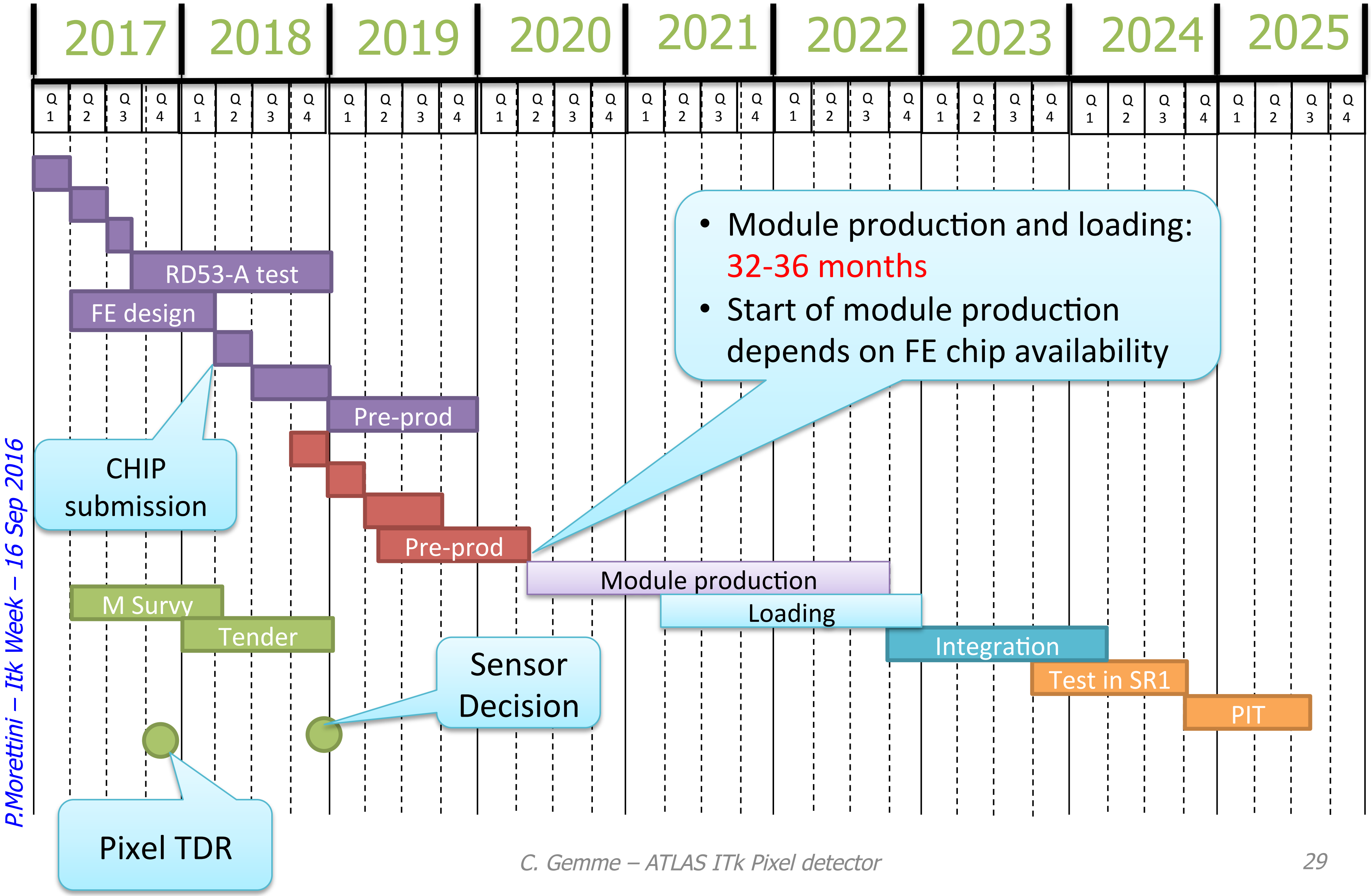
Fully monolithic

ITk Pixel timeline: close future

- ✓ In the last two years focus on finalizing the layout for the TDRs.
  - It is important also to have the community behind it.

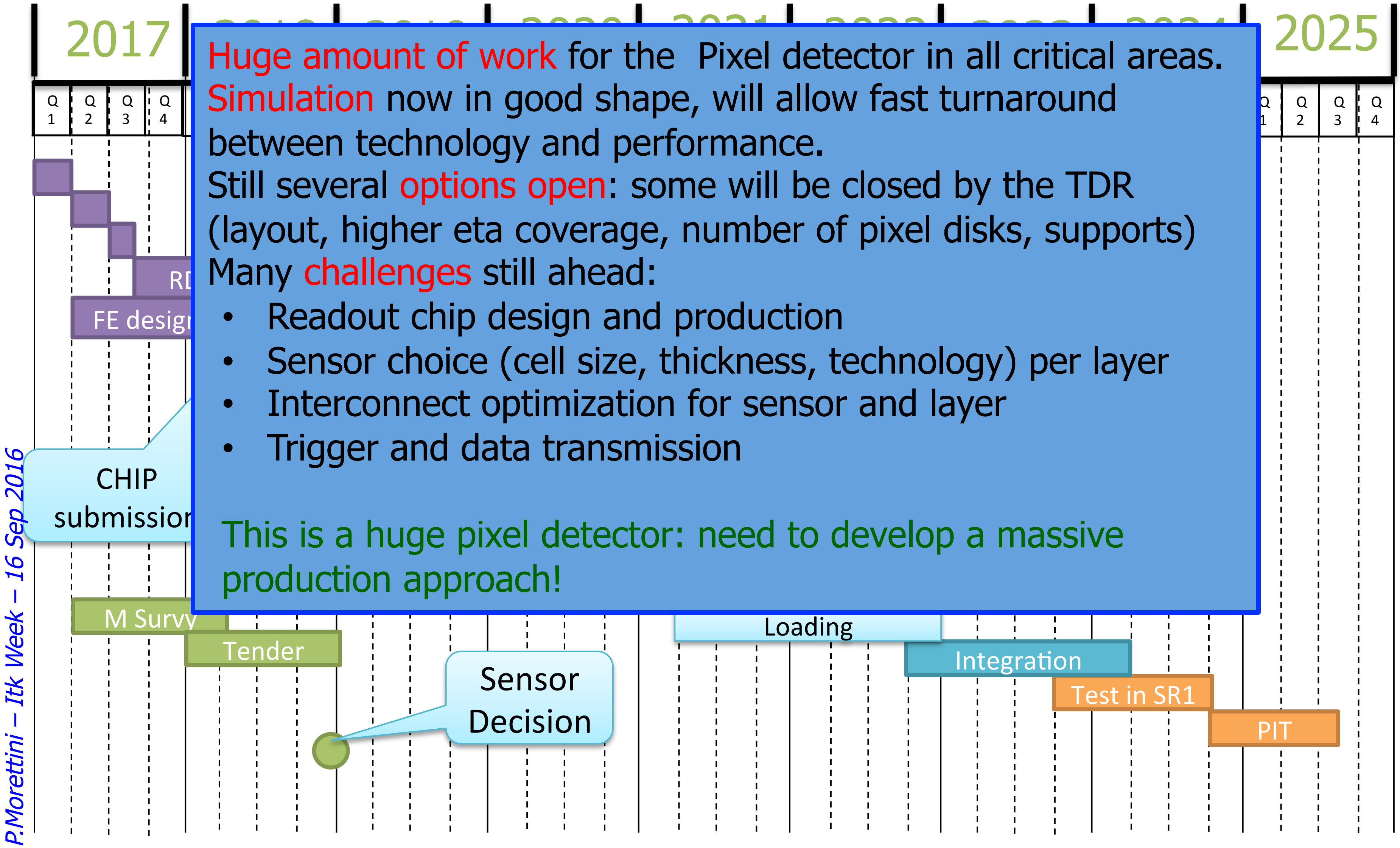


ITk Pixel timeline: future



P.Morettini – Itk Week – 16 Sep 2016

ITk Pixel timeline: future



Huge amount of work for the Pixel detector in all critical areas.
Simulation now in good shape, will allow fast turnaround between technology and performance.
Still several options open: some will be closed by the TDR (layout, higher eta coverage, number of pixel disks, supports)
Many challenges still ahead:

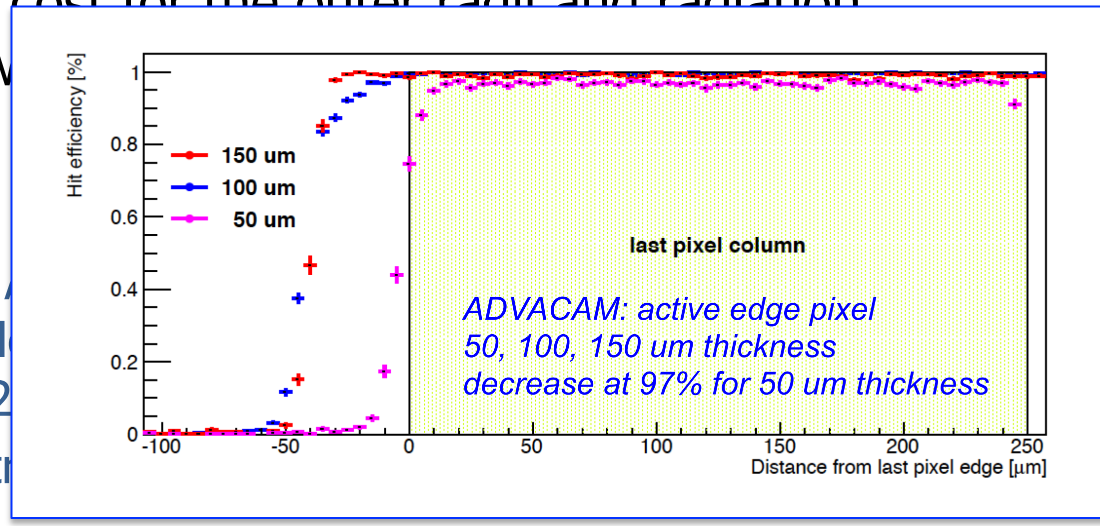
- Readout chip design and production
- Sensor choice (cell size, thickness, technology) per layer
- Interconnect optimization for sensor and layer
- Trigger and data transmission

This is a huge pixel detector: need to develop a massive production approach!

spare

Sensors: Planar

- Main challenges are low cost for the outer radii and radiation hardness, thermal runaw
- Achievements:
  - Technology n-on-p
  - Different vendors (Cis, interconnection technol a thickness range (50-2
  - 50x50 μm² pixel test str



  - Good hit efficiencies up to the physical perimeter of the devices obtained with (100-150) μm thin active edge sensors
  - FE-I4 modules with 100 μm thin sensors found to deliver 97% hit efficiency at a fluence of at $\Phi=1\text{x}10^{16}\ n_{eq}/cm^2$ for a moderate bias voltage of 500 V.
  - 4-chip modules have been built and inter-chip distances, in the range of 180-280 mm, tested
  - RD53A compatible sensors with SOI technology.

Sensors: Planar

- ✓ Main challenges are low cost for the outer radii and radiation hardness, therma
- ✓ Achiev
  - Tec
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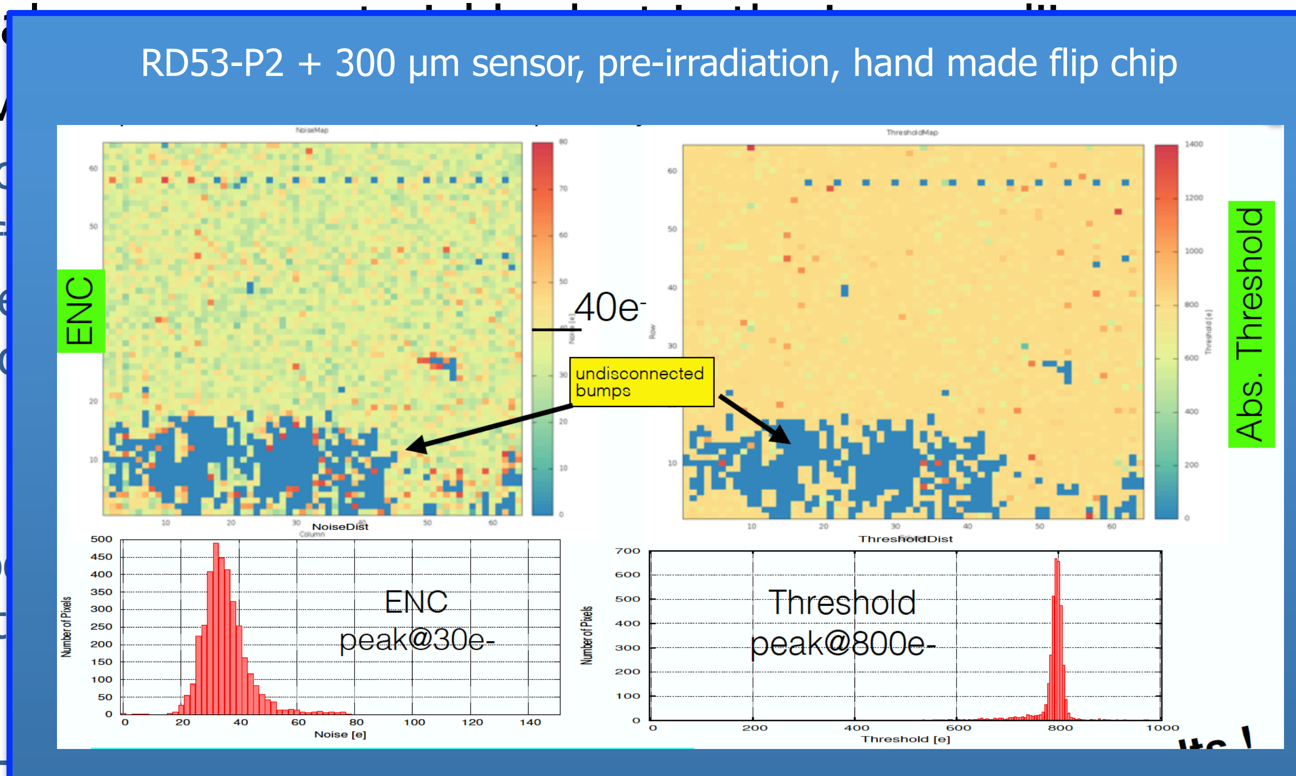
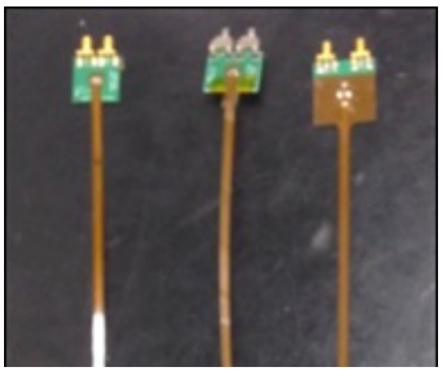
  - 50
  - Go obtained wit
  - FE- it efficiency at a fluence of at $\Phi = 1\times10^{16}\ n_{eq}/cm^2$ for a moderate bias voltage of 500 V.
  - 4-chip modules have been built and inter-chip distances, in the range of 180-280 um, tested
  - First RD53-P2 are in test; RD53A compatible sensors already produced.



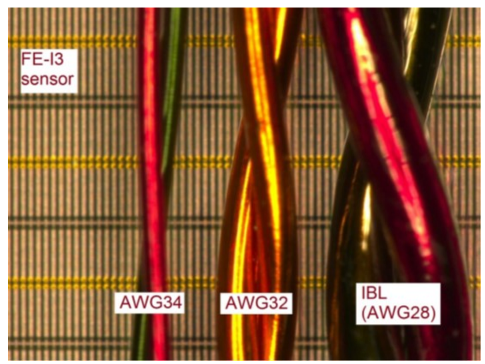
Data transmission and rates

- ✓ Preference to place optical conversion stages in a relatively accessible area, i.e. more than 5-9 m from the detector.
  - It means we need a low mass copper solution.
  - Several prototypes are under test, including controlled impedance flex lines, twisted pairs, micro-coaxial cables

Flex cables

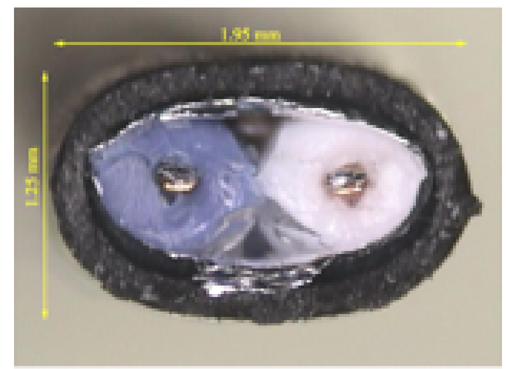


Micro twisted pairs



0,3 mm

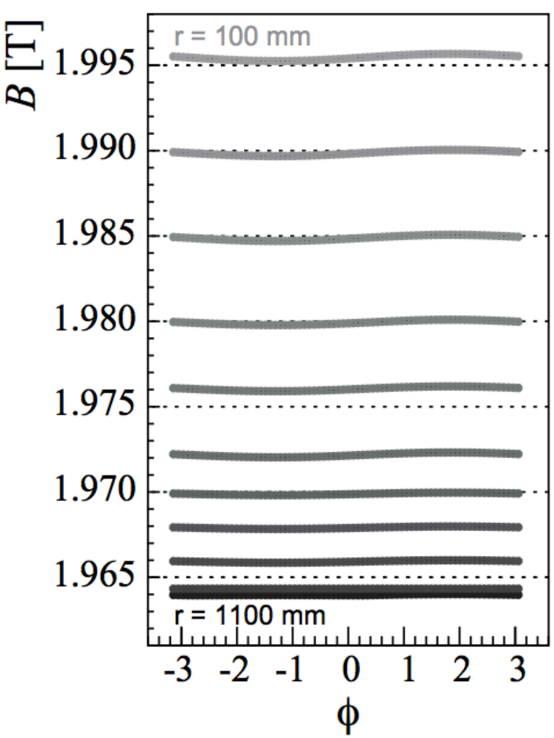
Twinax



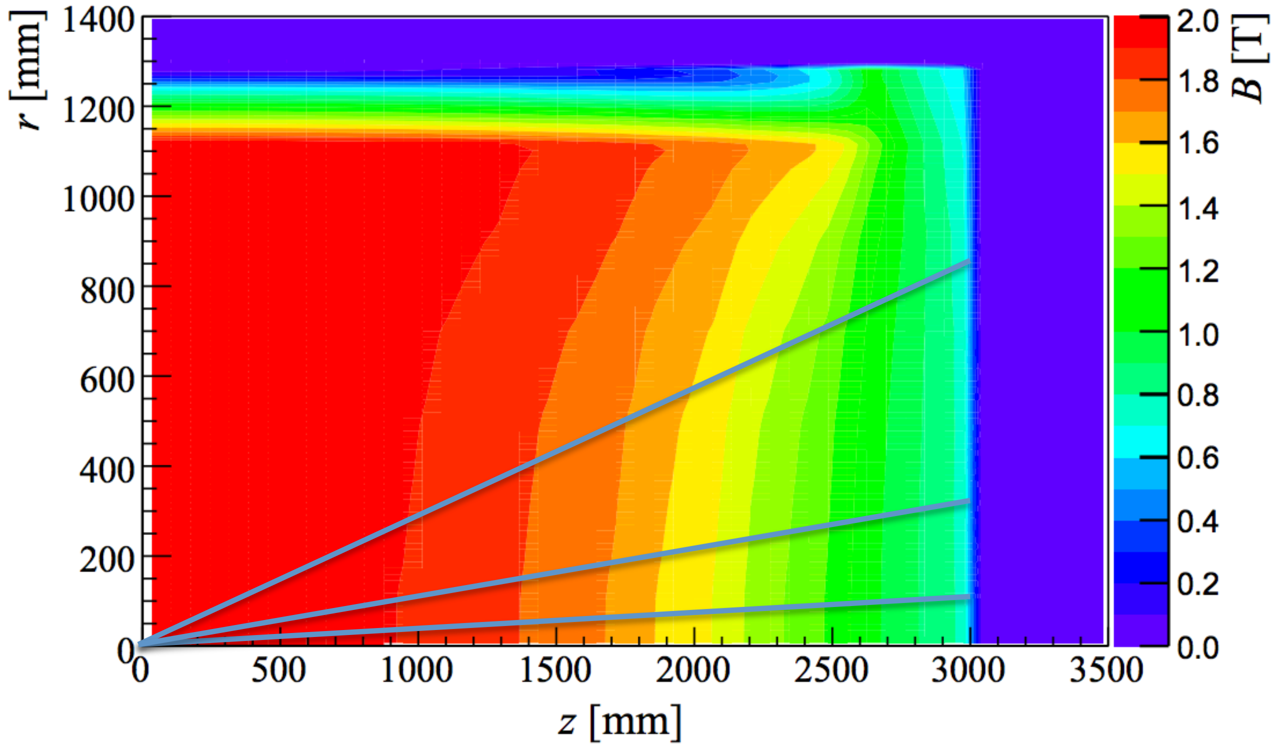
2 mm

- ✓ In the range 5-7 m, 5-6 Gb/s looks possible, provided error correction algorithms and pre-emphasis are used: design of TX section in the FE chip must be tuned for the specific transmission line in use.

B field



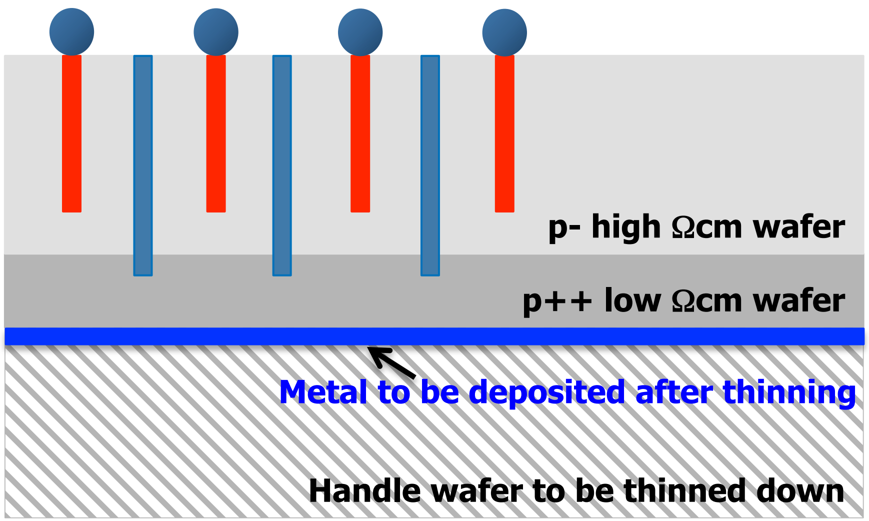
B [T]
1.995
1.990
1.985
1.980
1.975
1.970
1.965
r = 100 mm
r = 1100 mm
-3 -2 -1 0 1 2 3
ϕ



r [mm]
1400
1200
1000
800
600
400
200
0
0 500 1000 1500 2000 2500 3000 3500
z [mm]
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
B [T]

Sensors: 3D

→ *Gianfranco Dalla Betta*
Small pitch 3D devices



FBK layout, NIMA 824 (2016) 386