Universität Hamburg
DER FORSCHUNG | DER LEHRE | DER BILDUNG

PHYSICS AT THE TERA SCALE
Helmholtz Alliance

SPONSORED BY THE
Federal Ministry of Education and Research

CMS
Compact Muon Solenoid

The CMS Silicon Pixel Detector for HL-LHC

Georg Steinbrück, Hamburg University

for the CMS Collaboration

Vertex 2016

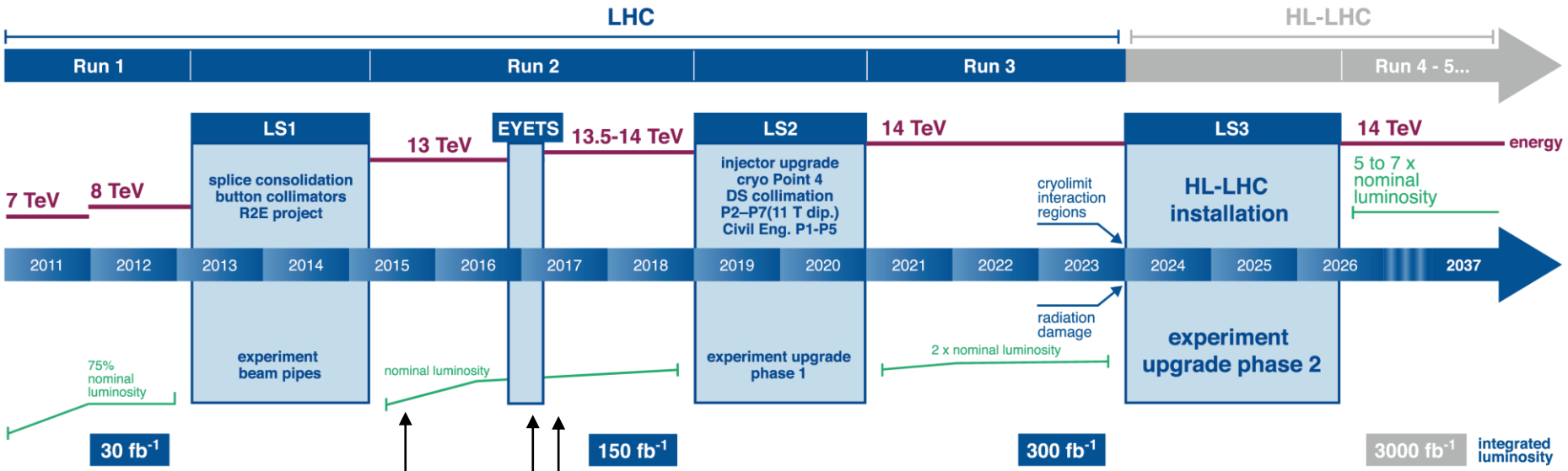
September 25-30, 2016

La Biodola, Isola d'Elba, Italy

Outline

- The CMS Tracking Detector Upgrade for the HL-LHC
- Detector layout
- Status of pixel sensor R&D
  - Planar and 3D silicon
- Serial powering
- Modules

The High Luminosity LHC: Roadmap



Tracker TDR
(Q2 2017)

Installation of phase-1 Pixels
(Q1 2017)

CMS Technical Proposal
& Scope Document
(Q2/Q3 2015)

Georg Steinbrück
georg.steinbrueck@desy.de

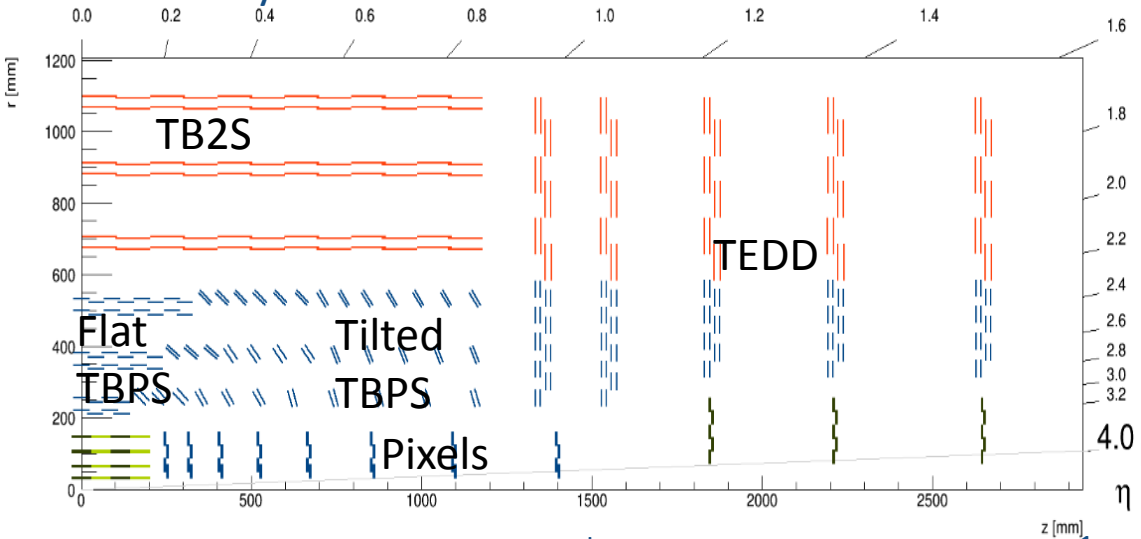
The Phase II Upgrade of the CMS Pixel Detector

High-Luminosity LHC:

- Luminosity of $5x10^{34}\,cm^{-2}s^{-1}$, up to 200 events/ 25 ns bunch crossing
- Maintain occupancy at ≈ % level and increase the spatial resolution

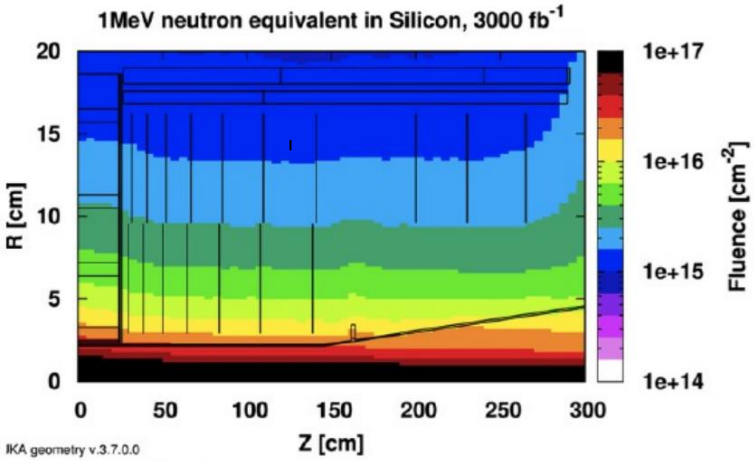
→ Pixel size ~ 25x100 μm^2 or 50x50 μm^2 (currently 100x150 μm^2)

Tilted layout:



Pixel detector:

- 4 barrel layers and 11 disks
- |η| up to 4



Radiation level for the 1st pixel layer after 3000 fb^{-1}:

- $\Phi_{eq} \approx 2x10^{16}\,cm^{-2}$, dose ≈ 10 MGy

3D or planar pixel sensors for 1st layer?

- R&D in parallel. Both options will be described and costed for TDR

Georg Steinbrück
georg.steinbrueck@desy.de

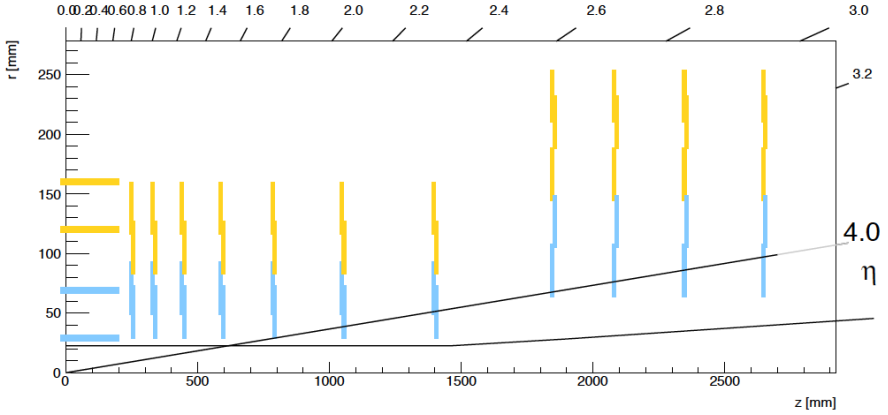
Pixel Detector Layout

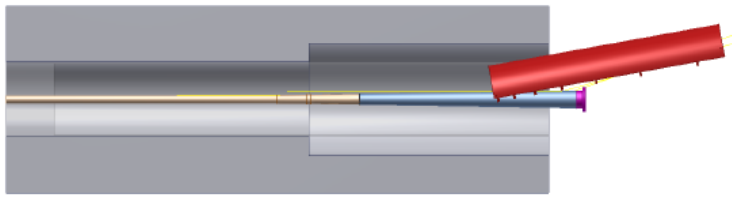
Coverage of geometrical acceptance:

- Barrel:
  - 4 layers à la phase I: $r_1 = 2.9$ cm, $r_4 = 16.0$ cm but shorter: $z_{max} = \pm 20$ cm instead of ± 27 cm
- Forward:
  - coverage at large $|\eta|$ obtained by increasing the number of discs (11+11) $z_1 = \pm 25$ cm $z_{11} = \pm 265$ cm

Total: ~4.5 m² of Si

- Simple mechanics:
  - no turbines/blades in the FPIX discs
- Step in the pixel envelope
  - r=20 cm → r =30 cm at z=160 cm
  - to allow the installation of the central section with beam pipe in place





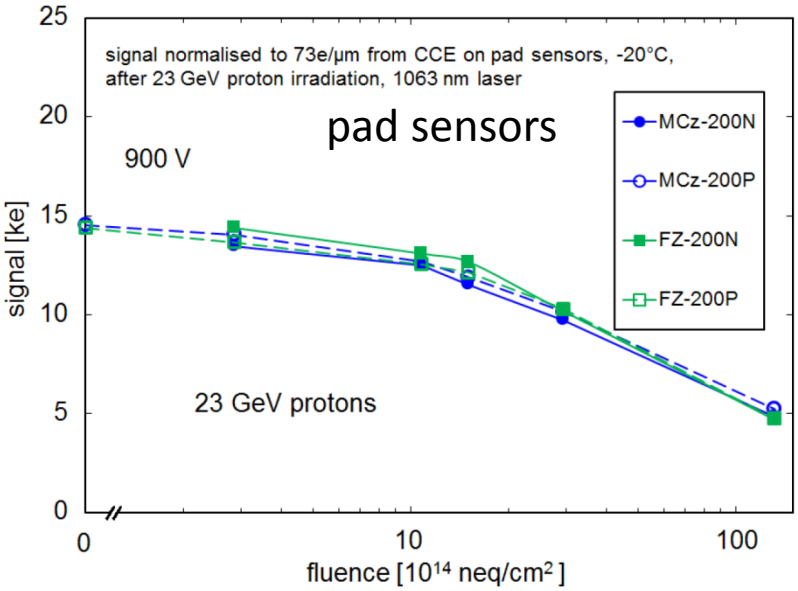
Radiation hardness

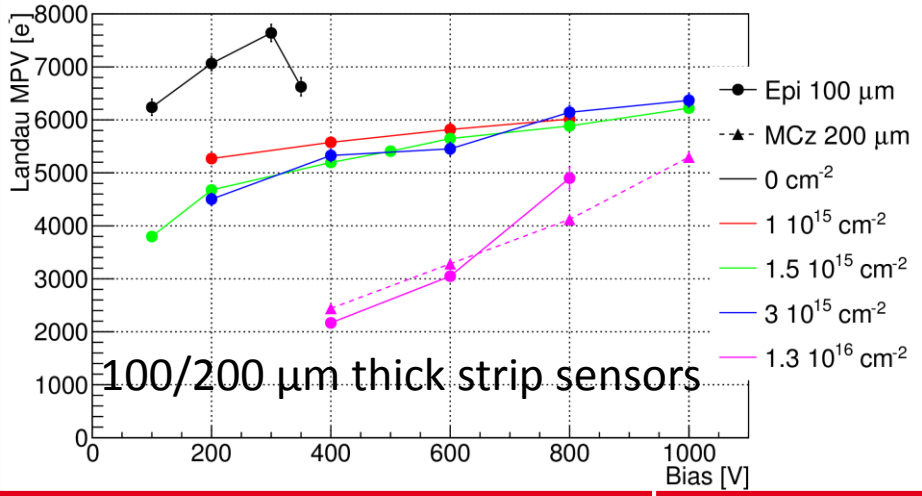
- Charge collection studied for irradiated 200 µm thick n-in-p **pad diodes**
  - 5k electrons at Φ_{eq} = 1.3x10^{16} cm^{-2} (900 V bias)

Thin silicon:

- Similar signal in 100 µm epi strip sensors as in 200 µm MCz: 5 k electrons at ~800V
  - However: Strong increase of current and noise with voltage at Φ_{eq} = 1.3x10^{16} cm^{-2}: Signs of soft breakdown/ charge multiplication

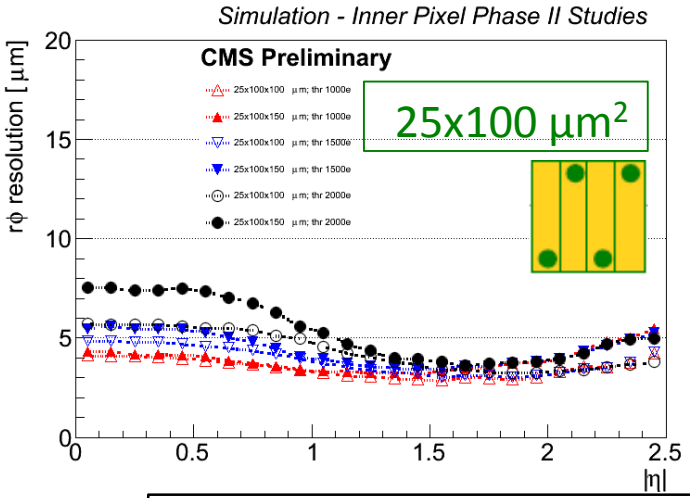
- Charge collection measurements need to be redone with pixel sensors: Weighting field
  - HPK submission, INFN/FBK submission

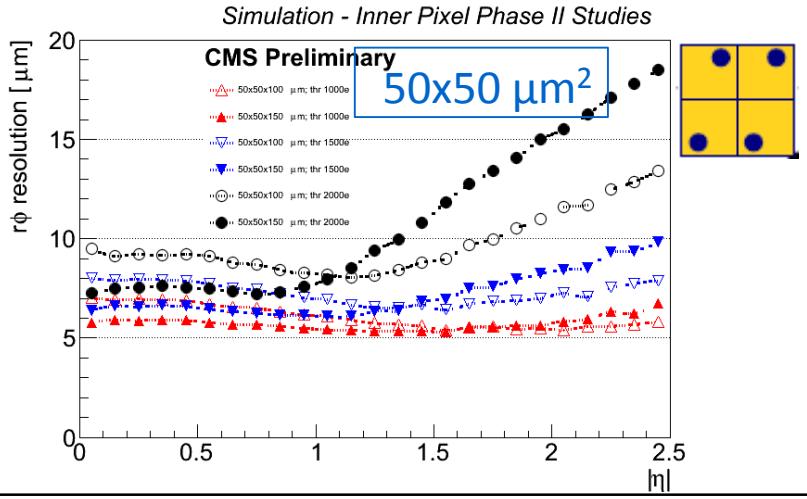




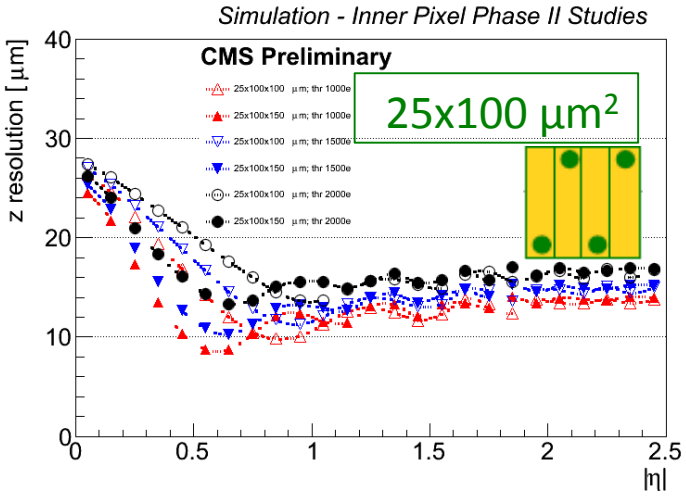
Georg Steinbrück
georg.steinbrueck@desy.de

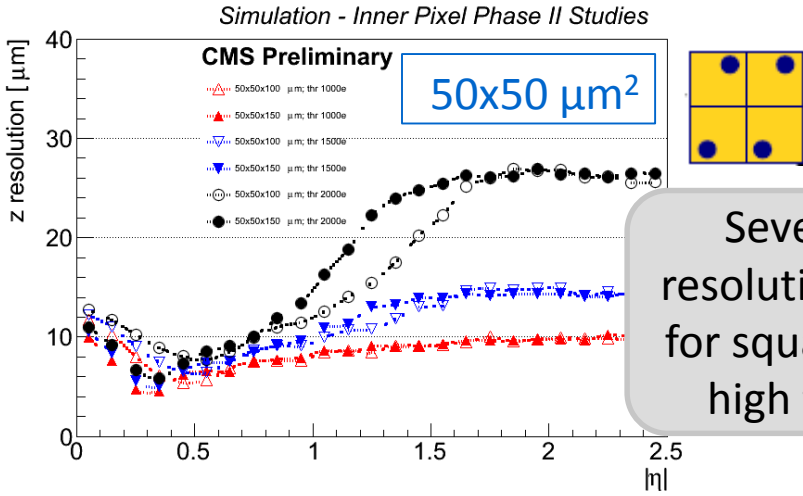
Fine Pitch Sensors





thickness open=100 µm/full=150 µm threshold 1000e/1500e/2000e



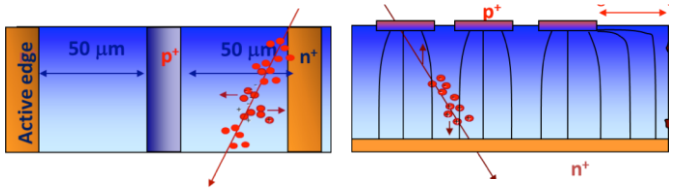


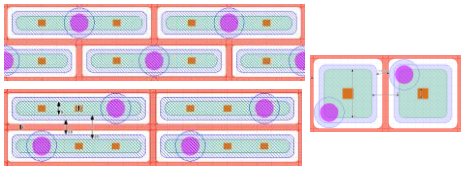
Severe loss of resolution at large η for square pixels for high thresholds

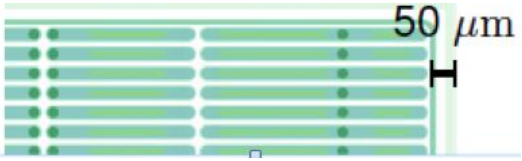
Georg Steinbrück
georg.steinbrueck@desy.de

Tasks: Pixel Sensors and Modules

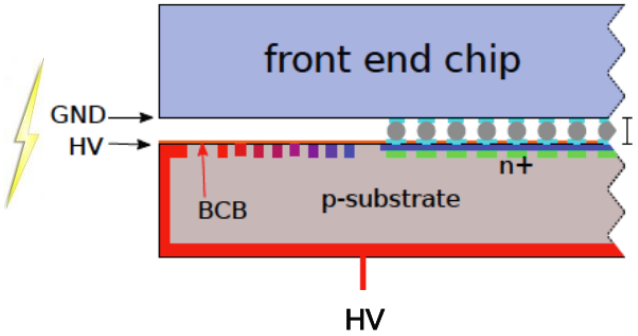
- Technical choice for inner layer: 3D or planar Si
- Sensor bulk material: 6” n^+-p wafers
- Chose sensor thickness
- Optimize sensor geometry and design
  - Evaluate Radiation hardness
- Sensor periphery
  - Design thin/ active edges







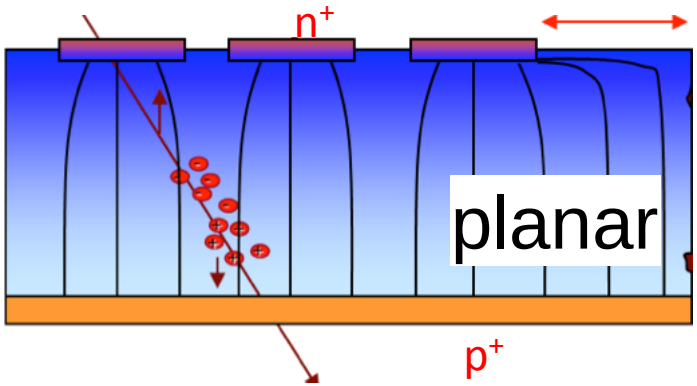
- Bump bonding: Fine pitch, thin silicon
  - Find cost effective solution
- Spark protection at sensor edges
  - Choose BCB polymer deposition or parylene coating

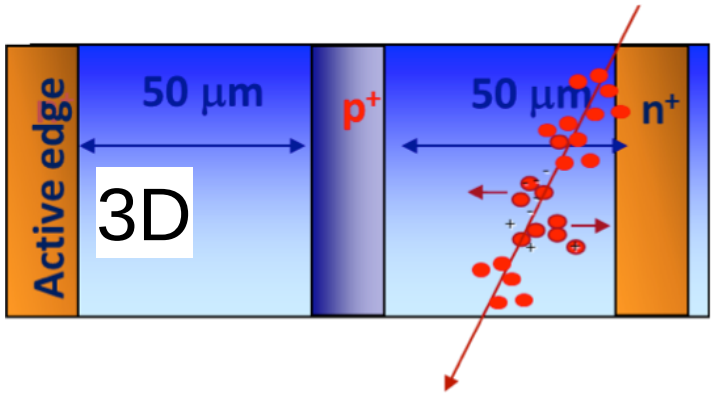


Thin Planar or 3D Pixel Sensors

Promising candidates for layers with very high radiation damage are:

- 3D pixel sensors
- thin planar pixel sensors (100 µm ≤ d ≤ 200 µm, currently d = 285 µm)





Common advantage:

- Short drift path
- Higher field at same V_{bias}

➞ Lower operation voltage

➞ Less power consumption

Thin planar sensors (n-in-p):

- Lower total I_{leak} after irradiation
- Less material (multiple scattering)

Drawbacks:

- Smaller initial signal (76 e^-/µm)
- Thinning step required
- Sensor „bow“

3D sensors:

- Thicker sensors possible

Drawbacks:

- Higher capacitance
- Lower yield
- Higher cost

Georg Steinbrück
georg.steinbrueck@desy.de

Sensor R&D programs in CMS

- Thin, small pitch planar pixel sensors
  - HPK submission (n^+-p)
    - (**50x50, 25x100**, 30x100 **µm²**) sensor design options on thin (150 µm) n-in-p wafers
  - INFN – FBK R&D program, together with ATLAS (n^+-p)
  - SINTEF (n^+-n)

First thin small pixel test sensors work well
Next step: Demonstrate radiation hardness

INFN/FBK

- 3D silicon
  - INFN – FBK R&D program (3D batches)
  - CNM Barcelona

Successful production of 3D sensors. Next step: Demonstrate feasibility of small pixels.

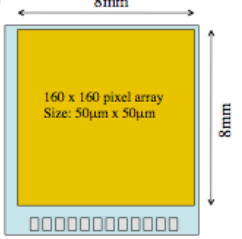
INFN/FBK
CNM

ROC Options for R&D

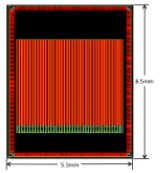
- PSI46dig and PROC600
  - **IBM 250 nm, 100 x 150 µm²**, 80 x 52 pixels, rad hard > 5 MGy (PROC600)

PSI46dig only chip available as of today, but not as rad. hard

- ROC4Sens (PSI)
  - **IBM 250 nm, 50 x 50 µm²** , 155 x 160 pixels, no charge threshold, rad hard > 5 MGy, operated with CMS pixel test board, **staggered BB pattern**, opening 15 µm
  - available since summer 2016 (on PROC600 wafer)



- FCP130 (FNAL)
  - **GF 130nm, 30 x 100 µm2** , 160 x 48 pixels, threshold: ~1000 e- , rad hard few MGy, DAQ under development
  - availability foreseen early 2017



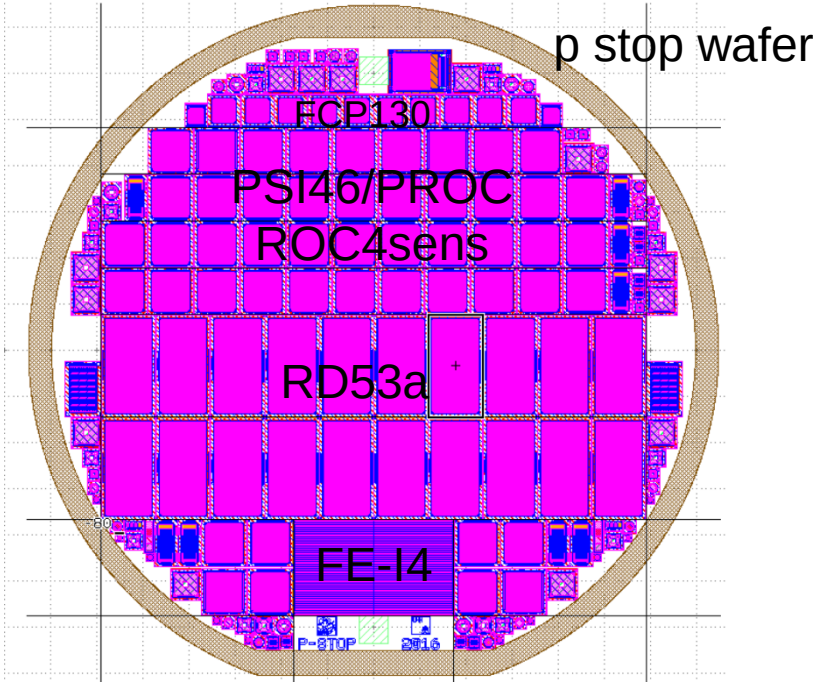
- RD53A:
  - **65nm, 50 x 50 µm2** , 400 x 192 pixels, min. threshold: 600 e- , rad hard up to 10 MGy **non-staggered BB pattern**
  - availability 2017

For ROC developments, see also talks on "*RD53 status and plans*" by L. Gaioni and "*Radiation Tolerance of 65nm CMOS*" by M. Menouni (Thu)

- FEI4 (ATLAS) (used for serial powering studies)
  - **GF 130 nm, 50 x 250 µm²**, 336 x 80 pixels, threshold < 2000 e^- , rad hard > 5 MGy

HPK Submission on 6” n^+-p wafers

- 35 wafers 6” n^+-p FZ, 3 materials
  - 150 µm, no handle wafer
  - 150 µm + 50 µm Si-Si direct bond
  - Deep diffused 150 µm + 50 µm
  - P-stop and p-spray isolation (only dir. bond)



Aims of the R&D submission:

- Evaluate pixel geometry: 25x100 vs. 50x50 µm²
- Study and Optimize sensor design
  - Pixel isolation: p-stop vs p-spray (rad-hardness)
  - Bias scheme for small pixels
    - no bias, common punch through, polysilicon bias
  - Metal overhang to mitigate E-field
  - Signal routing

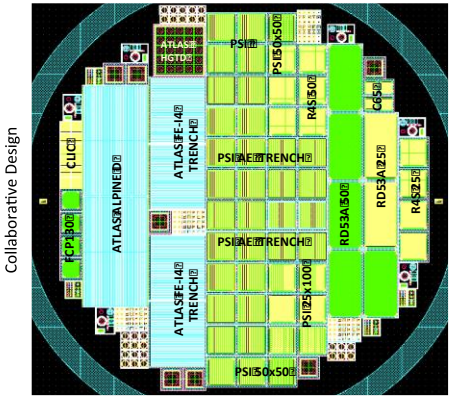
Pixel sensors for these r/o chips:

- PSI46/PROC600, ROC4sens, RD53a, FCP130, CHIPIX65, (FE-I4)

Design with HPK, wafers expected back early 2017

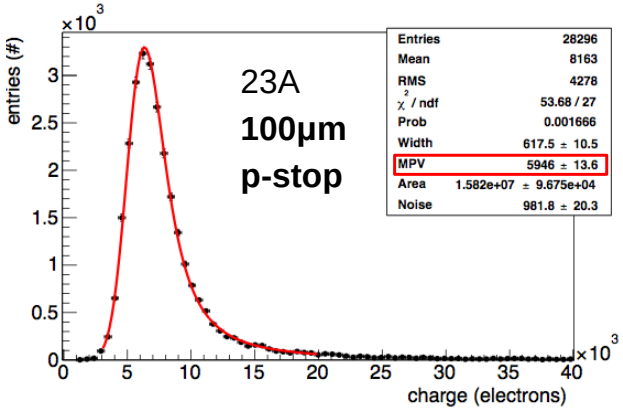
INFN Planar Submission

- Common ATLAS and CMS pixel R&D at FBK Trento funded by INFN
  - n-in-p pixels on 6”, new 6” production line!



Aims of the R&D submission:

- Study and optimize pixel sensor design
  - P-spray vs P-stop isolation
  - Punch through versus no punch through bias structures
- Evaluate module/ interconnectivity issues
  - Thinning (before/after processing)
  - Explore bump bonding technologies: IZM Berlin, SELEX Rome
  - Spark protection (BCB)

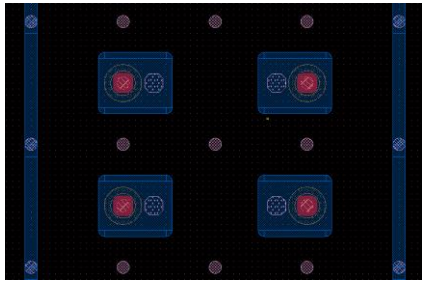


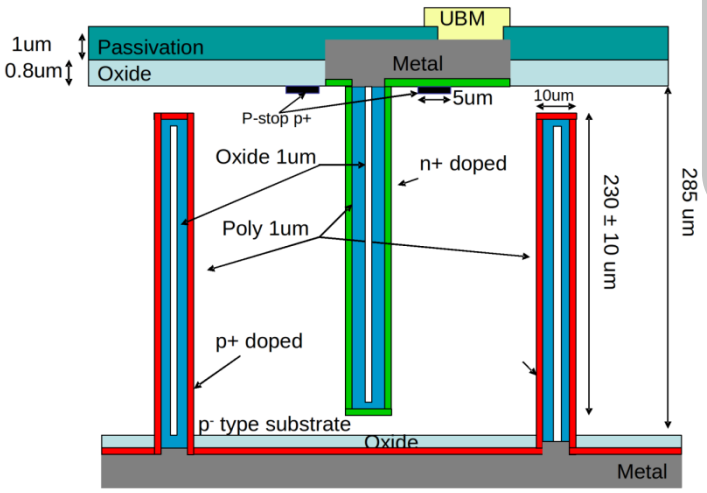
- 2 planar batches (plus 1 more to come)
  - Dec 14: Qualification batch, 100/130 µm thickness
    - 31 modules (PSI46): First results, irradiation and analysis ongoing → Successful 100 µm pixel production!
  - **Planar Active/Slim Edge** batch: Sensors in production, first process steps done

Georg Steinbrück
georg.steinbrueck@desy.de

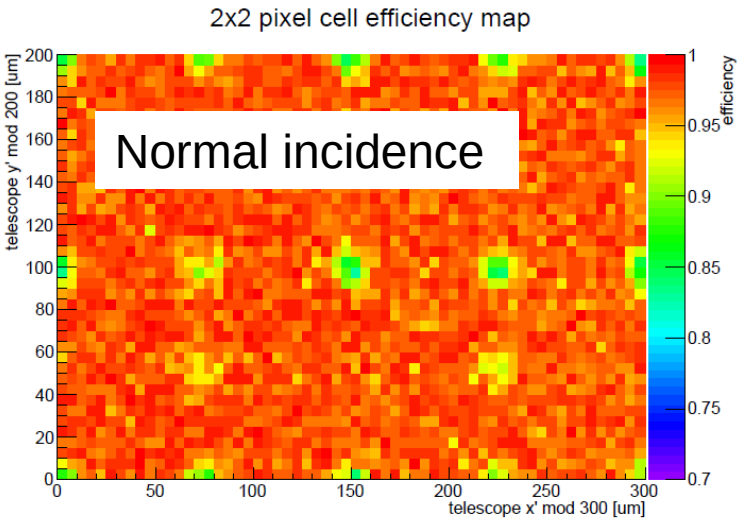
3D Sensors: CNM Run

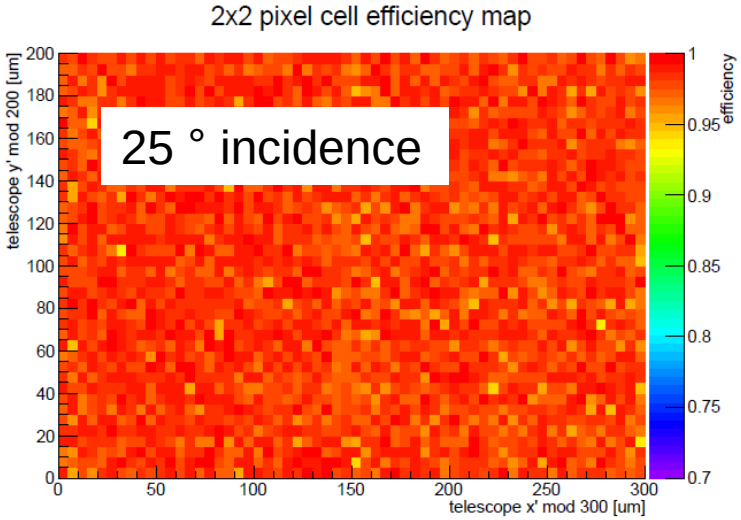
- 3D pixel sensors fabricated by CNM, Spain
- IBL run, read out with CMS PSI46dig ROC
- 100x150 µm²





Double sided 3D process yields good sensors with "standard" pixel size

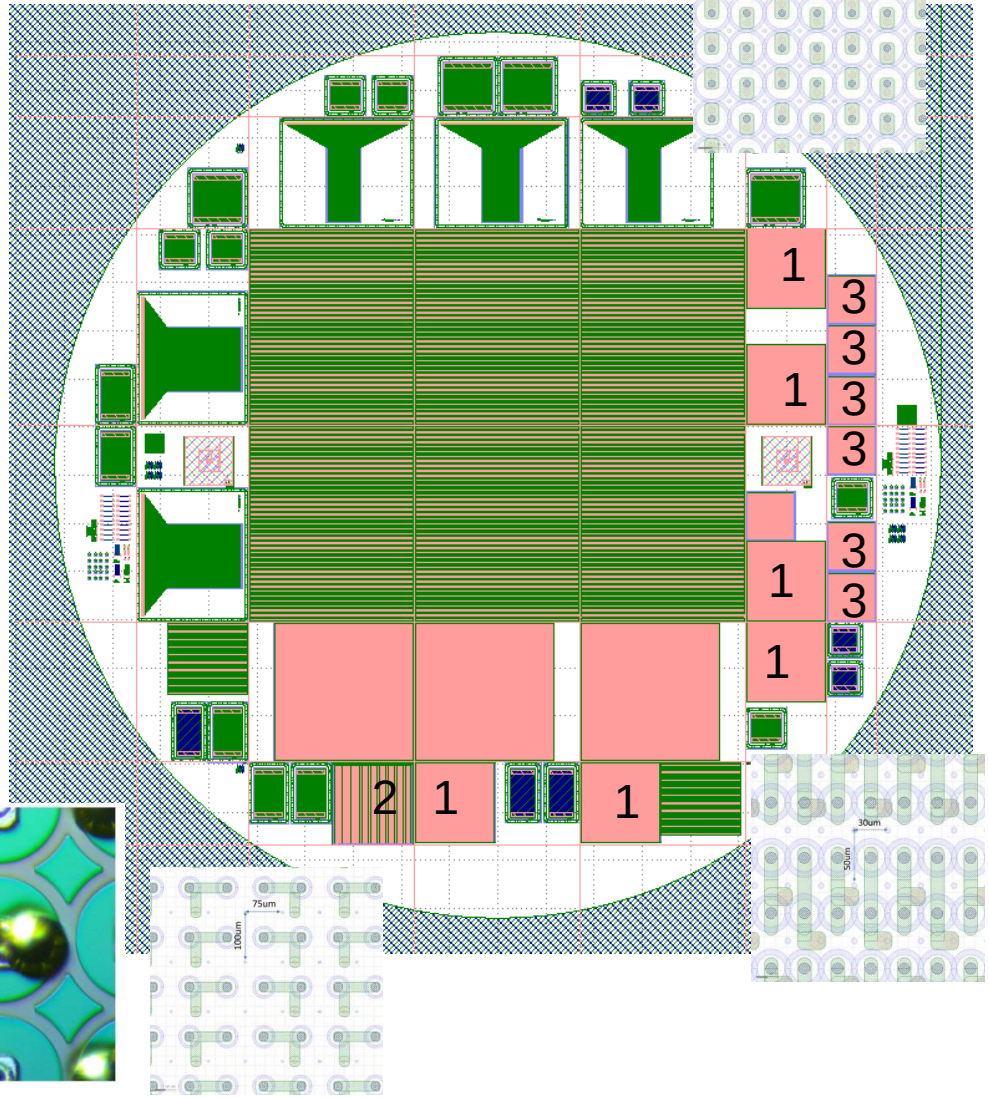




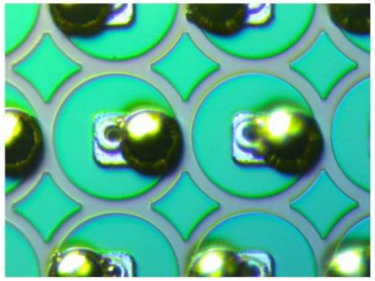
Georg Steinbrück
georg.steinbrueck@desy.de

3D: Small Pitch Run at CNM

- Joint RD50 project: ATLAS, CMS, LHCb
- 230 µm wafer, n-in-p, double sided
- CMS: Sensor designs for 3 chips
  1) ROC4sens 50x50 µm²
  2) PSI46dig 100x150 µm²
  3) Fermilab FCP130 30x100 µm²
- **Aims:**
  - Test small pitches (25x100 and 50x50)
  - **Aspect ratio: 8 µm holes in 230 µm (1:25)**
  - 100 µm and 200 µm slim edges
  - Radiation hardness of different layouts



5 wafers completed December 2015
All diced
Investigating Ni/Au UBM
(electroless and electroplating)
Flip-chip to FE-I4 validation in progress



Status of INFN R&D on 3D Pixel Sensors

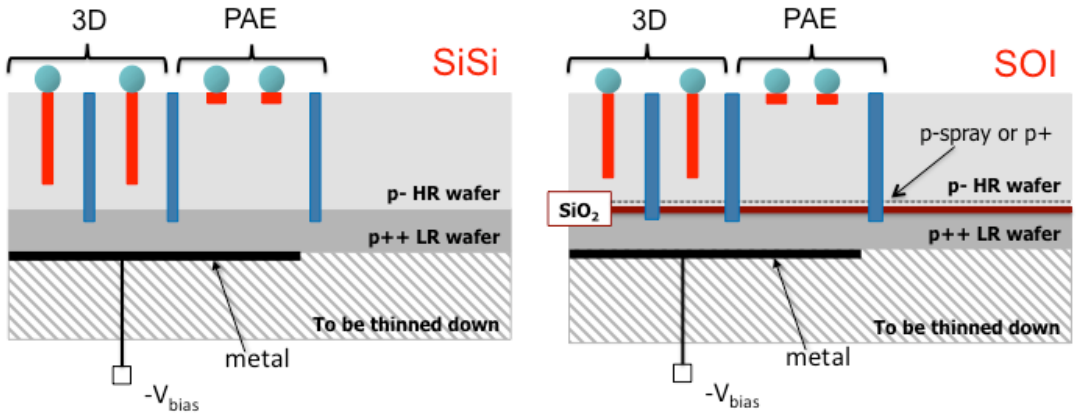
- 3D sensors made with single sided DRIE (deep reactive ion etching) process at FBK Trento, Italy
  - Si-Si Direct Wafer Bond (DWB) **100 µm and 130 µm active FZ**, 500µm handle CZ

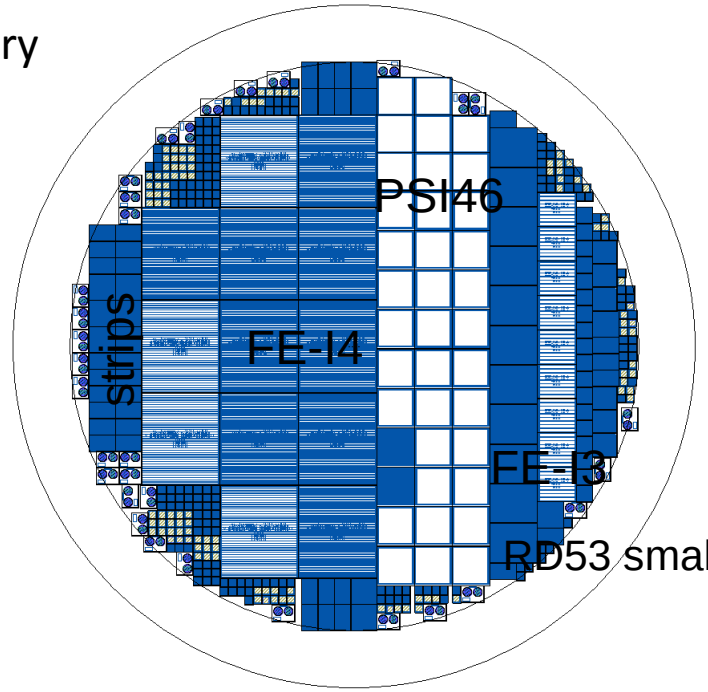
Aims:

- Trying "the technology limit" with many small pitch structures

See also talk by G.-F. Dalla Betta on "*Small pitch 3D devices*" (Thur 9 am)

- Production completed, 3D wafer quality overall satisfactory
- Bump bonding to FE-I4 + PSI46dig at Selex in preparation
  - Investigations of small pitch 3D pixels to come

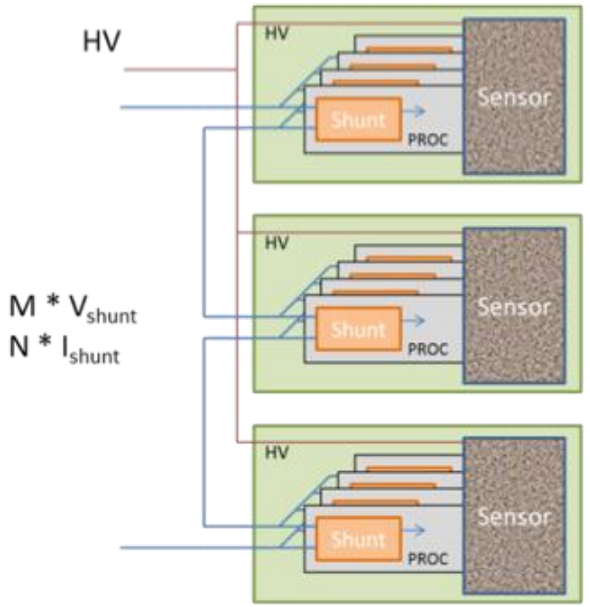


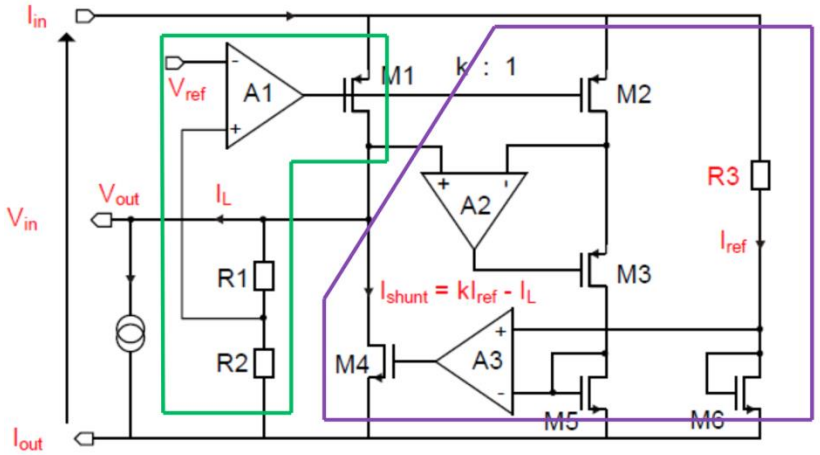


Pixel Phase II Powering Baseline

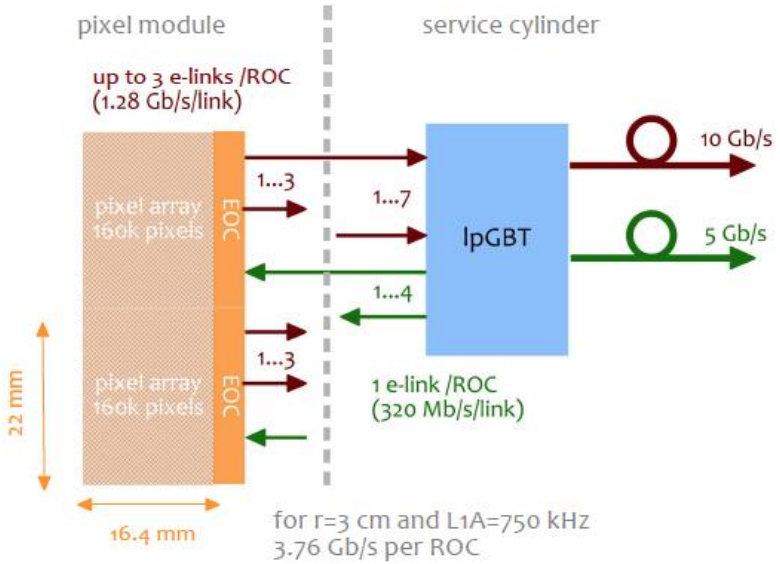
- Required power: ~20 kW for 4.5 m^2
  - Traditional powering schemes (phase-0: direct from PS, phase-I: DC-DC converter) cannot be used due to material and space issues (aggravated by forward extension) and radiation → investigate **serial powering** across modules
  - Material gain factor given by # of modules in series
- Serial powering: current driven (voltage drops ~not relevant) and intrinsically low mass; not very efficient and failure modes needs to be carefully evaluated
- Gain experience with setup based on ATLAS FEI4
- Shunt-LDO* circuit is the heart of SP approach
  - Integrated in the ROC itself
  - Developed for FEI4 chip family, being ported in RD53
  - Provides regulated voltage, shunts the excess current

(*LDO: Low Dropout Regulator)

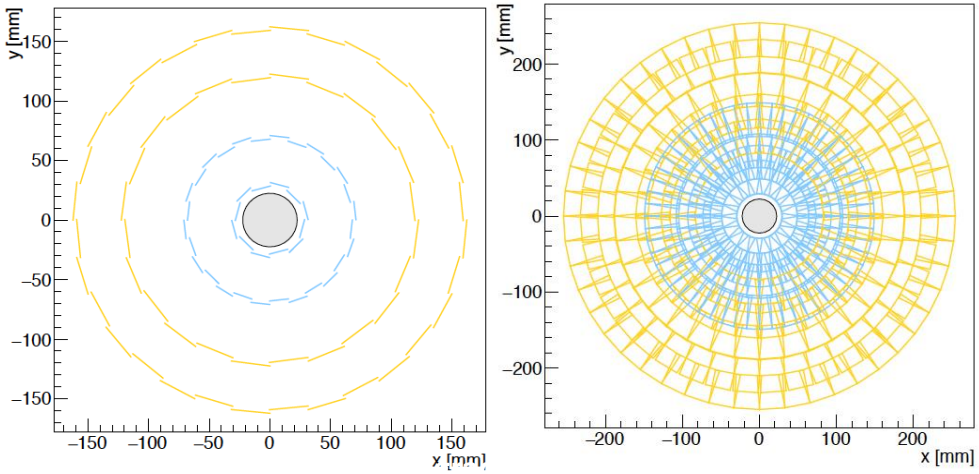




Modularity and Modules



- No opto-electronic device able to withstand the radiation environment of the inner layers.
- Solution: "**remote**" **lpGBT** placed on the pixel service cylinder and connected to the module (readout and control signals) via e-links cables.
- Modularity defined by matching output rates of modules to e-link and lpGBT specs.



- Minimal number of module types e.g. 2x1 or 2x2 ROCs/module with typical size of a ROC 2x2 cm^2.
- No wedge shaped modules.
- Possibly small/large pixels in different layers/discs.

Conclusion

- HL-LHC poses high demands on pixel detector
  - Radiation hardness →thin sensors with radiation hard design
  - Efficient and precise tracking at high rates →small pixel pitches
  - Radiation tolerant, fine pitch, low noise readout chips→RD53
  - Fast links
- R&D programs to develop thin, fine pitch sensors and address pixel design issues
  - Planar: HPK submission, INFN/FBK (together with ATLAS), SINTEF
  - 3D: INFN/FBK (together with ATLAS), CNM
- Fine pitch bump bonding of thin sensors/ROCs challenging and a major cost driver
- Serial Powering baseline, R&D ongoing

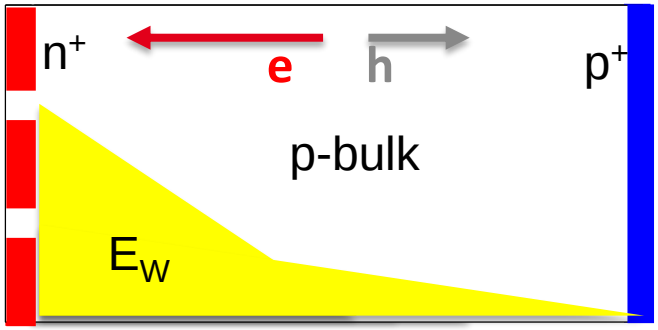
- Tracker Upgrade TDR due next year!

Georg Steinbrück
georg.steinbrueck@desy.de

BACKUP

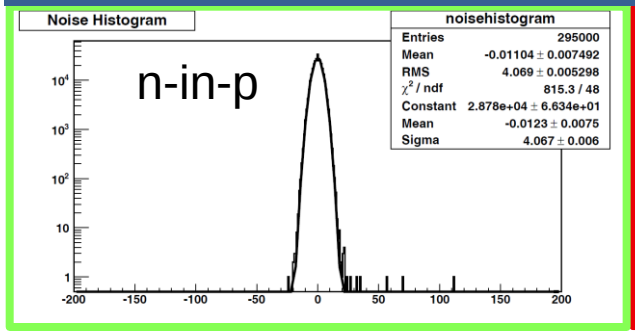
From n-in-n to n-in-p

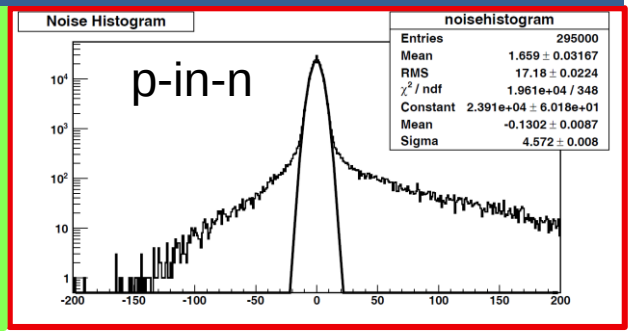
- n-in-p single sided process
  - More vendors, cost effective
- Thin sensors: Especially costly for double sided n-in-n
- n-side readout preferred
  - Electrons: Higher mobility than holes, higher lifetime
    → Advantage to collect electrons at high weighting field (E_w)
  - Excess noise observed in p-in-n strip sensors for Φ>1E15 cm^{-2}
  - T-CAD simulations confirm that p-in-n sensors have the tendency to exhibit high electric fields at the strips due to positive oxide charges (likely curable by careful design)



Charge collection: Illustration

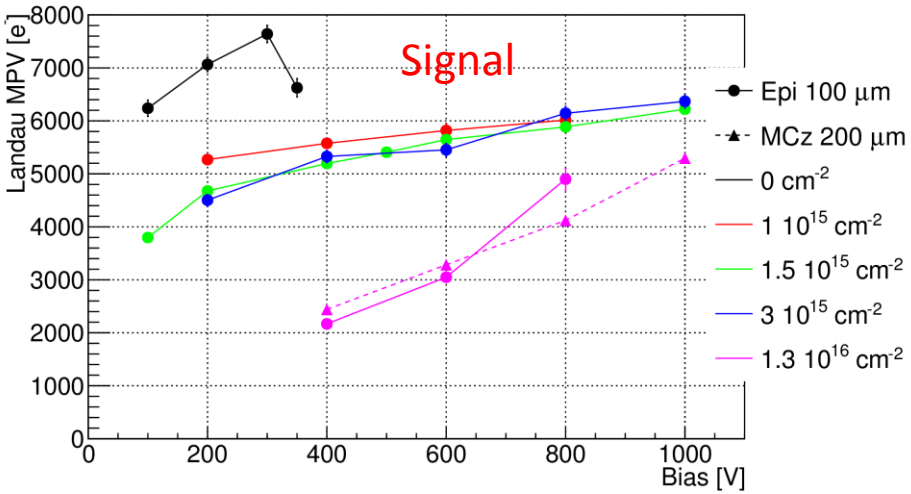
Noise histograms in 80 μm pitch strip sensor

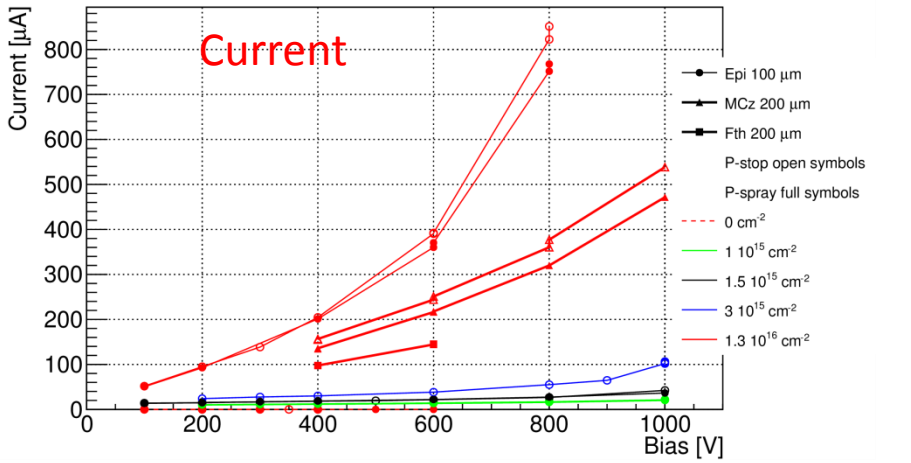


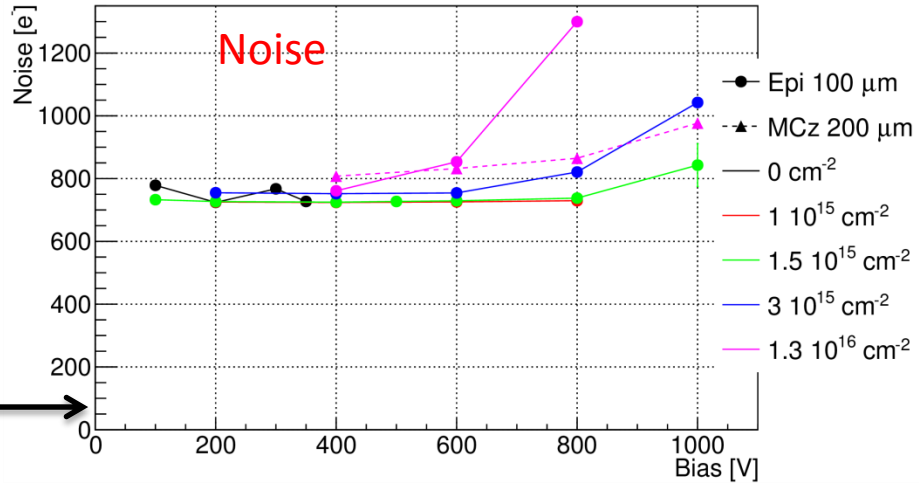


Going Thinner: 100 µm Epi Sensors

- n-in-p mini strip sensors from HPK Outer Tracker campaign in DESY testbeam







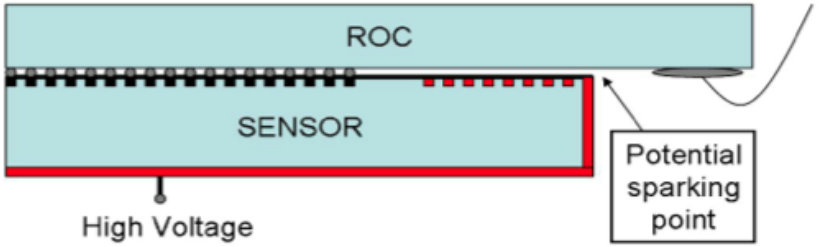
- 5000 e^- at ~800 V
  - Similar collected charge to 200 µm MCZ/FZ!
- However: Strong increase of current and noise with voltage at Φ_{eq} = 1.3x10^{16} cm^{-2}: Signs of soft breakdown/ charge multiplication

Georg Steinbrück
georg.steinbrueck@desy.de

Addressing the Sparking Problem

Sparking between ROC and sensor is a concern for single-sided n-on-p pixel modules. Also of concern for OT modules. Possible solutions:

- Parylene coating of entire module after assembly
- BCB polymer deposition during processing (cut lines exposed?)



Single-sided, n-on-p module

Georg Steinbrück
georg.steinbrueck@desy.de