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CMOS pixel development for HL-LHC

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CMOS pixel detectors with charge collection in an epitaxial layer (10-20 μm thick) have been developed since 2001 and have become realized in the STAR pixel detector at RICH and are also proposed for the ALICE ITS Upgrade. For the rate and radiation environment expected at the HL-LHC new approaches have been developed based on the following enabling technology features: HV add-ons that allow to use high depletion voltages (HV-MAPS); high resistivity wafers for large depletion depths (HR-MAPS); radiation hard processed with multiple nested wells to allow CMOS electronics embedded with sufficient shielding into the sensor substrate and backside processing and thinning for material minimization and backside voltage application.

R&D within for HL-LHC has started about 2010. Currently members of more than 20 groups in ATLAS are actively pursuing CMOS pixel R&D in an ATLAS Demonstrator program (sensor design and characterizations) started in 2014. The program's first goal was to demonstrate that depleted (monolithic) CMOS pixels (DMAPS) are suited for high rate, fast timing and high radiation operation at LHC. For this a number of technologies have been explored and characterized. In this presentation the challenges for the usage of CMOS pixel detectors at HL-LHC are discussed such as fast readout and low power consumption designs as well as fine pitch and large pixel matrices. Different designs of CMOS prototypes are presented with particular emphasis on timing (rate) performance and radiation tolerance.

Author: HUEGGING, Fabian (Universitaet Bonn (DE))

Presenter: HUEGGING, Fabian (Universitaet Bonn (DE))

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