# Radiation Tolerance of 65nm CMOS process

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# Outline

- Introduction
- RD53 collaboration
- Effect of radiation on CMOS devices
- Irradiation test results of 65 nm transistors
  - Irradiation test of digital devices
  - Temperature effects during irradiation
  - Annealing effects
- Radiation effects modeling for SPICE simulation
- DRAD : digital test chip for irradiation tests
- Summary and conclusion

# RD53 collaboration

- Design and develop pixel chips for ATLAS/CMS phase 2 upgrades
- Extremely challenging requirements for HL-LHC
  - Hit rates: 3 GHz/cm² (200 MHz/cm² in the current system)
  - Small pixels: 50 x 50 μm²
  - Radiation : 1 Grad - 2 1016 n/cm² over 10 years
    - 1 Grad seems to be very challenging
    - Target of 500 Mrad. Inner layer to be changed after 5 years
  - Large chips : ~2cm x 2cm
  - Data readout : 4-5 Gbit/s
  - Trigger Latency up to 12.8us (deep storage buffer)
  - Low power - Low mass
- Baseline technology : 65nm CMOS
- Large scale demonstrator pixel chip in March 2017
  - 2cm x 1.18cm - 400x192 pixels of 50 x 50 μm²
- 19 collaborating institutes organized on different working groups

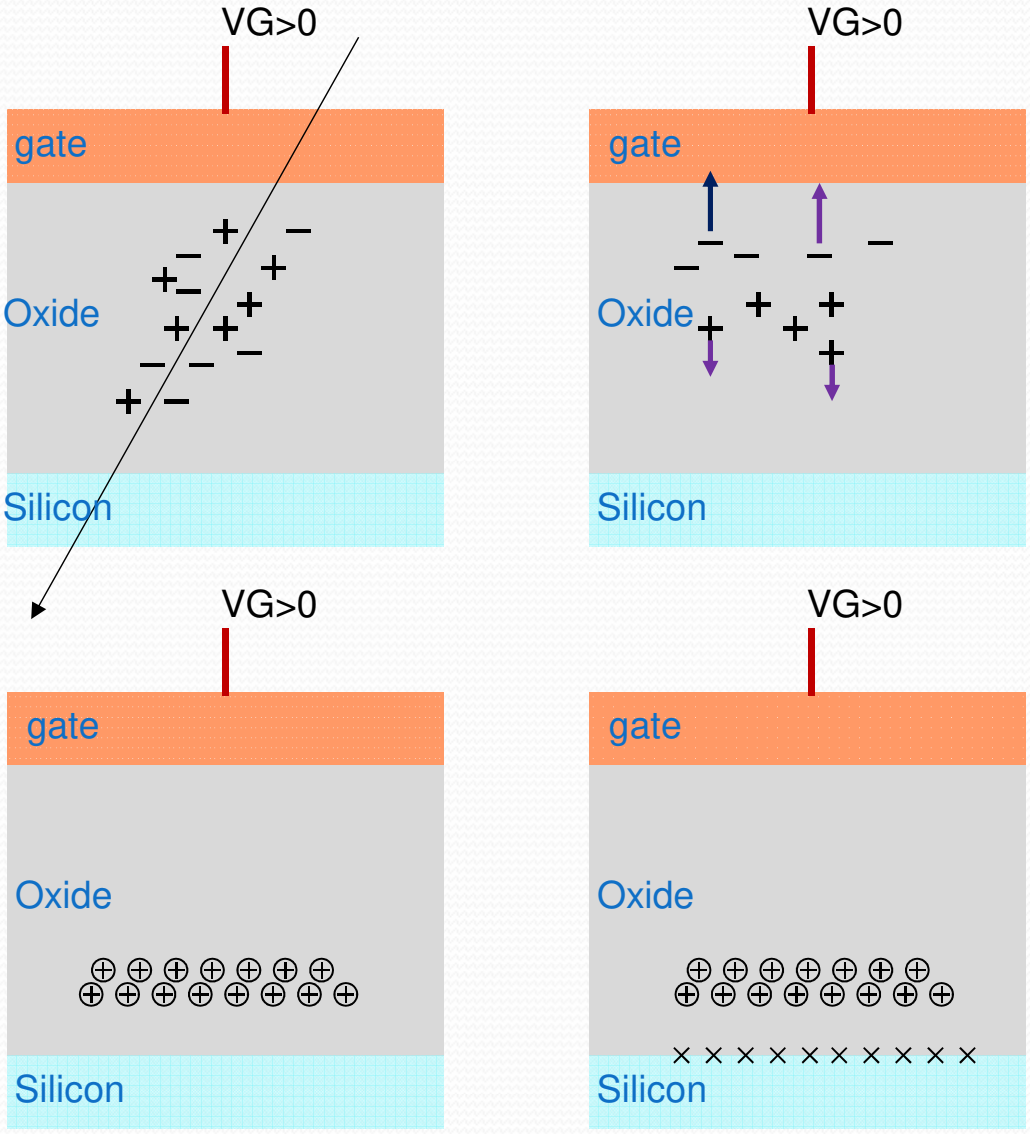
# Radiation effects in CMOS

# Radiation effects in CMOS

$SiO_2$ : $\mu_e \sim 10^6 \times \mu_{hole}$

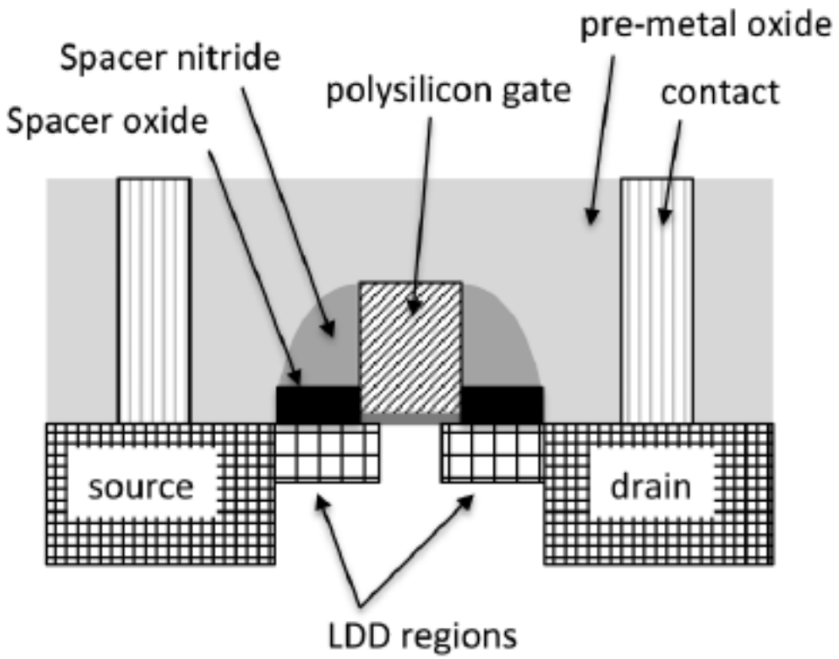
($\mu e \sim 20$ cm²/V.s at room temp)

- 1st step: Ionizing Radiation → electron/hole pairs creation in oxide. Depending on biasing, electrons swept out in ~ps. A fraction of e- / holes recombine
- 2nd step: Hopping hole transport to Si/SiO2 interface
- 3rd step: Holes at interface → long-lived trap states → Qot →ΔVot : <0 for nmos and >0 for pmos
- 4th step: Interface traps build-up : → Qit → ΔVit (>0 for nmos and pmos)
- Reminder:
  - gate thickness tox = 2.6nm
  - ΔVt α tox2 + tunnel annealing
  - The 65 nm is intrinsically very radiation hard



# Radiation effects in CMOS

- In highly scaled processes
  - The thin gate oxide is very tolerant to the TID
  - Thick oxide is used for isolation : Thick Shallow Trench Isolation Oxide (STI)
  - Thick oxide exists everywhere around the device




- For more details :

Radiation Induced Narrow Channel Effect:

F. Faccio and G.Cervelli, IEEE Trans. Nucl. Science, Vol.52, N.6 (2005) pp.2413-2420

http://dx.doi.org/10.1109/TNS.2005.860698

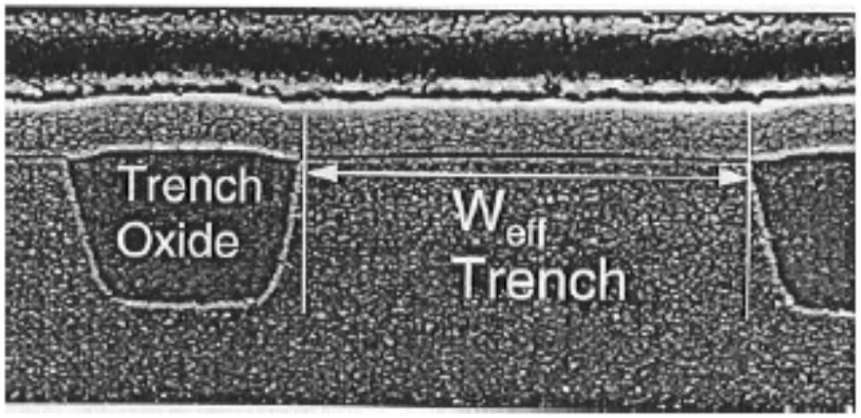
Radiation Induced Short Channel Effect:

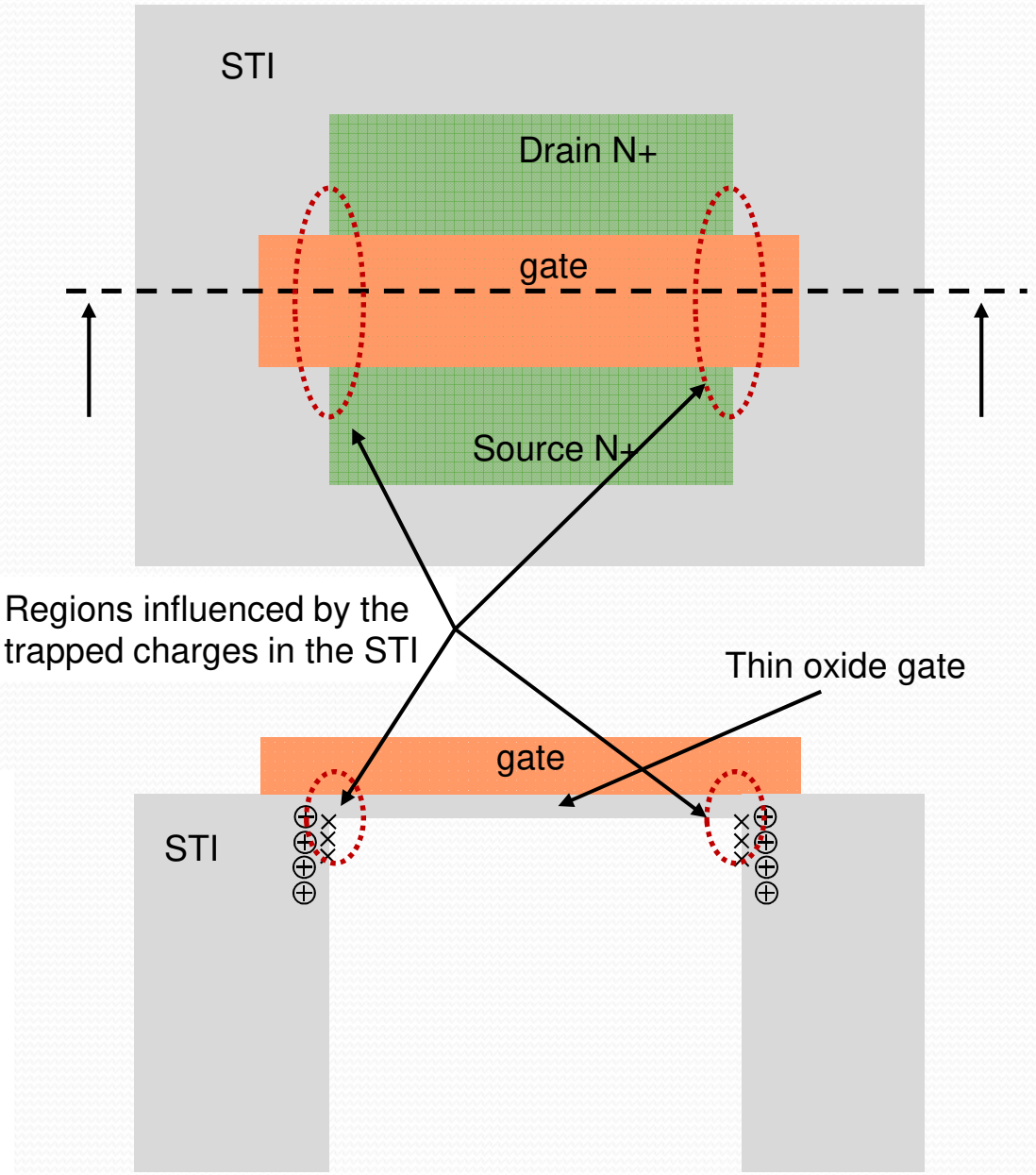
F. Faccio et al., IEEE Trans. Nucl. Science, Vol.62 , N.6 (2015)

http://dx.doi.org/10.1109/TNS.2015.2492778

# Radiation effects in CMOS

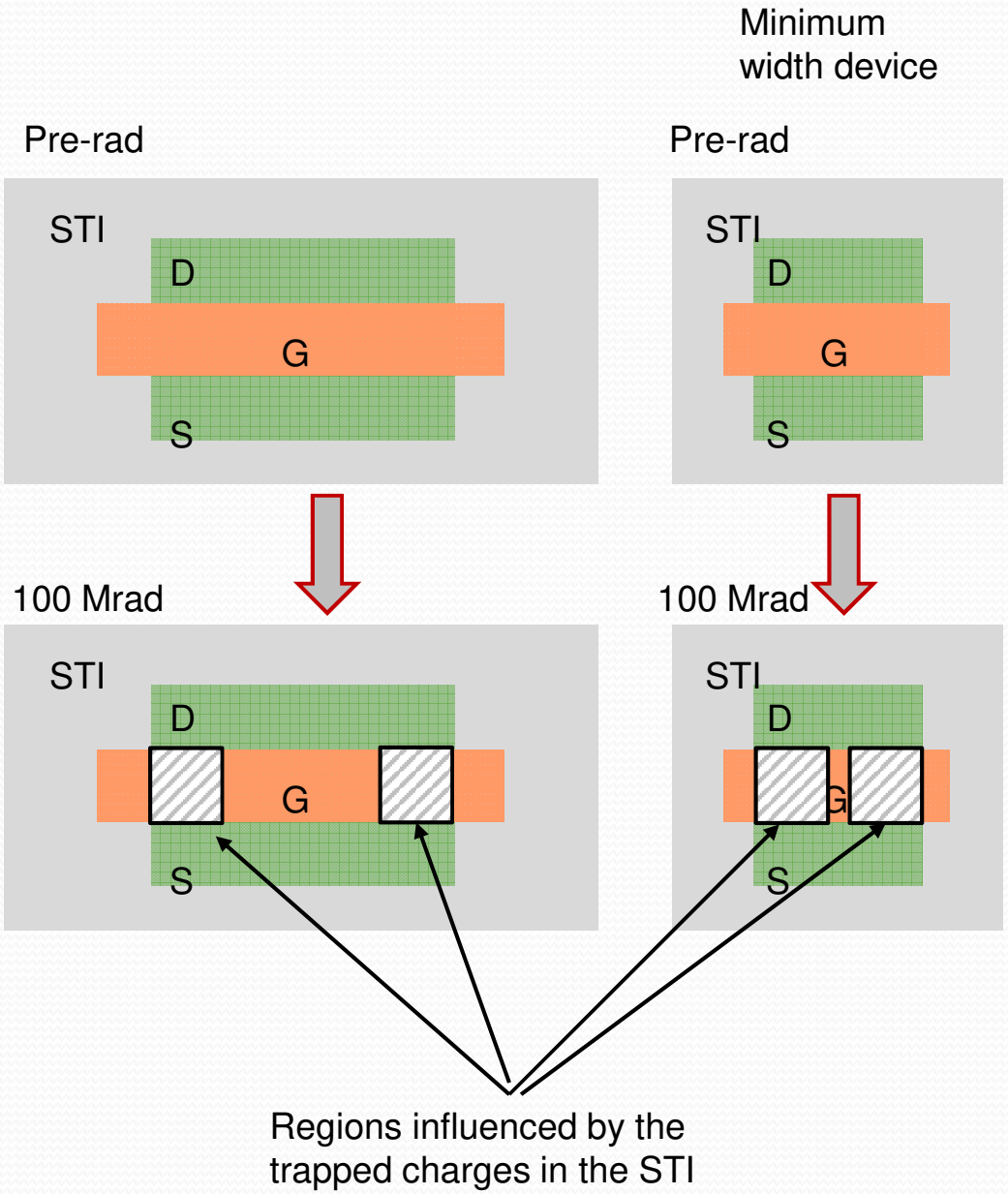
- Thick Shallow Trench Isolation Oxide
  - Used for isolation
  - Depth of ~ 300 nm
  - Radiation-induced charge-buildup
    - Oxide trapping and interface trapping
    - May turn on lateral parasitic transistors -> leakage
    - Affect electric field in the channel : Vth shift, mobility decrease, noise increase
- Doping profile along STI sidewall is critical
  - Doping increases with CMOS scaling
  - Decreases in I/O devices (less tolerant)



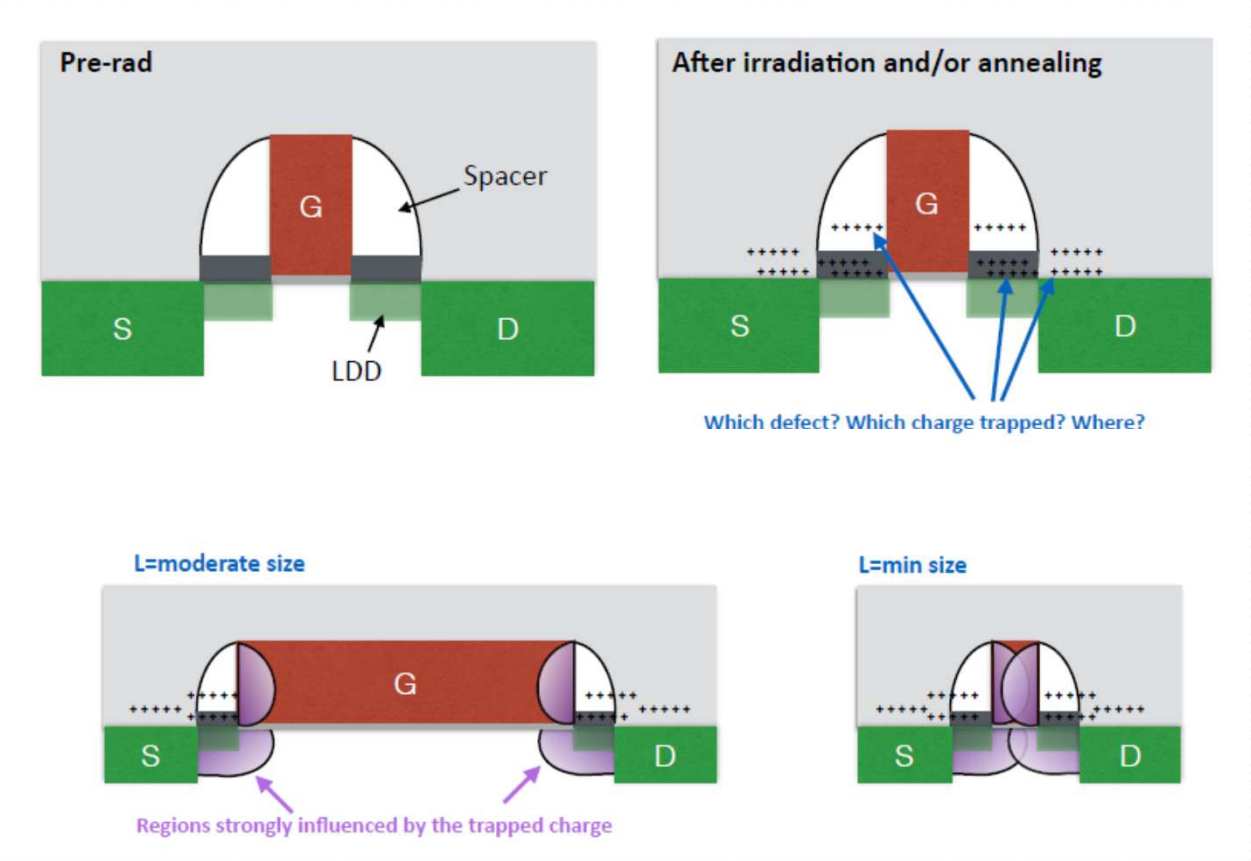



# Radiation Induced Narrow Channel Effect

- RINCE is caused by the charge trapped in the STI
- This charge affects the electric field in the channel and modify the transistor characteristics
- More relevant for narrow transistors



# Radiation Induced Short Channel Effect

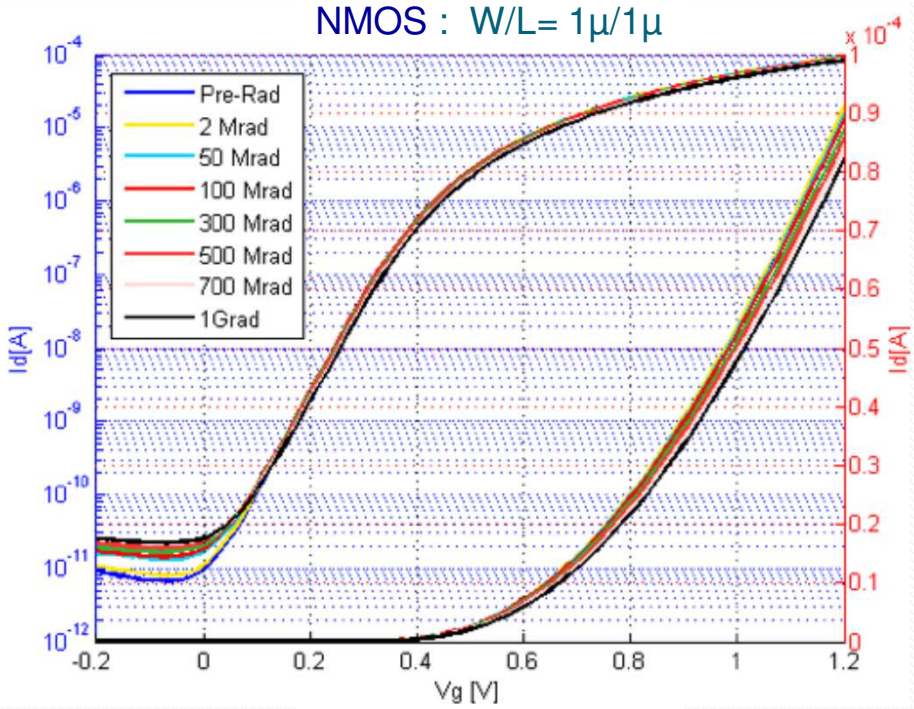


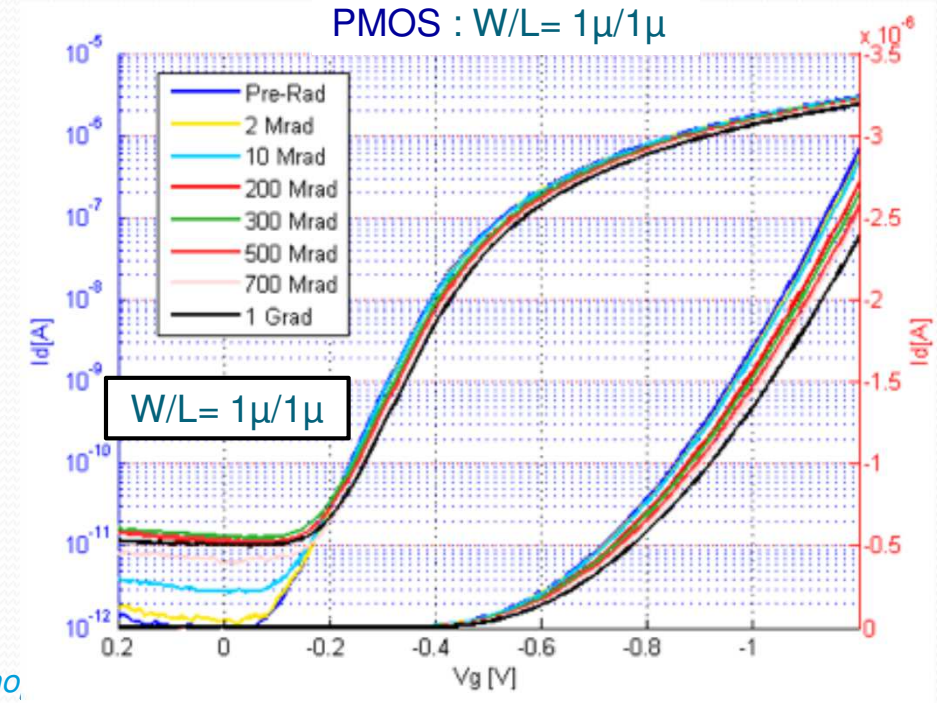

- RISCE is not related to the STI
- May be attributed to the charge induced in the spacer's oxide because of irradiation effects.
- This charge affects the electric field and then the surface potential in the LDD (Lightly Doped Drain)
- More damage for short channel device

# Irradiation Tests

# Large size transistors

- TID effect on large and long devices (NMOS and PMOS) is limited
- The 65 nm is intrinsically very radiation hard
- Analog Design : Avoid the use of narrow or short transistors
  - Analog designs following these rules showed a good radiation tolerance up to 1 Grad
  - Irradiation damage depends on the bias. The matching can become worse with irradiation
- Digital design : Available standard cells are designed with minimum L and narrow devices
  - Are subject to RINCE and RISCE effects
  - Irradiation qualification procedure is needed



# Devices for digital design

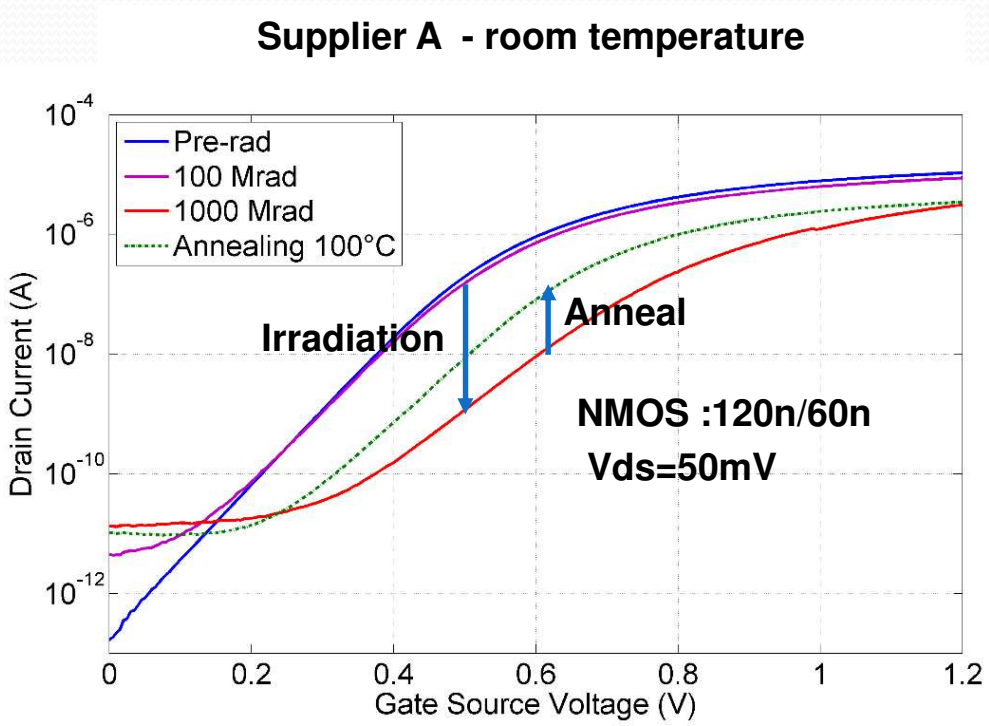
- Devices with different widths were considered in this study
  - All with minimum length of 60 nm
  - Only the Regular VT device (RVT) is considered
- Irradiation effects depend strongly on the bias and the temperature
  - Worst conditions is the diode connected bias : VDS=1.2V and VGS=1.2 V
  - This over-evaluate the damage in the digital circuits
- Help in setting the minimum width for PMOS and NMOS transistors to be used in digital design libraries

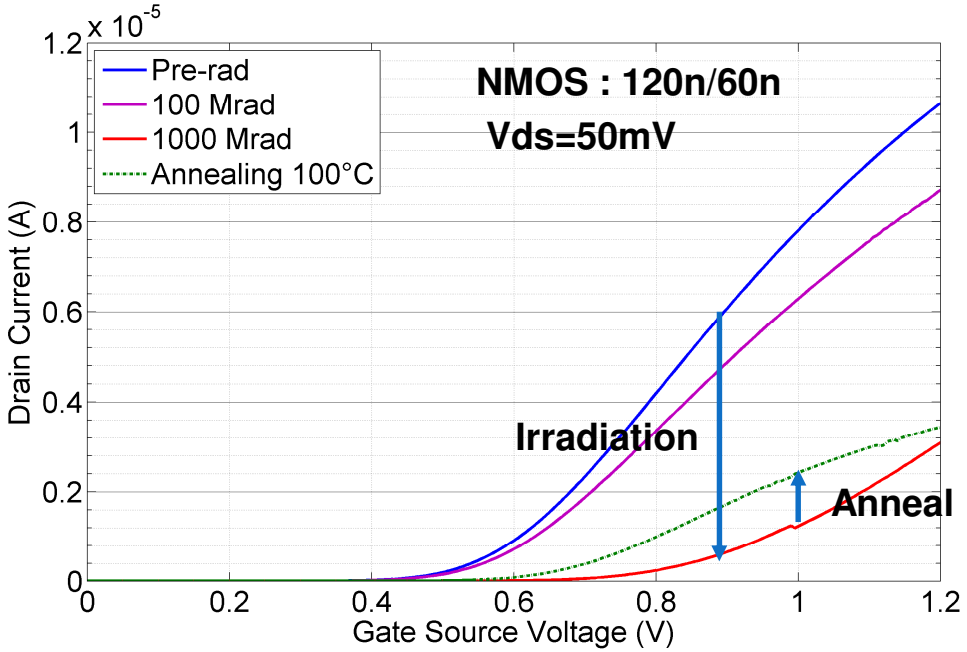
| | NMOS devices | PMOS devices |
|---|---|---|
| | W/L (nm/nm) | W/L (nm/nm) |
| Regular open layout | 120/60 | 120/60 |
| | 240/60 | 240/60 |
| | 480/60 | 480/60 |
| | 1000/60 | 1000/60 |
| ELT | 800/60 | 1480/60 |

1−Grad total dose evaluation of 65 nm CMOS technology for the HL−LHC upgrades"
Journal of Instrumentation 10(05): May 2015

# NMOS devices irradiation

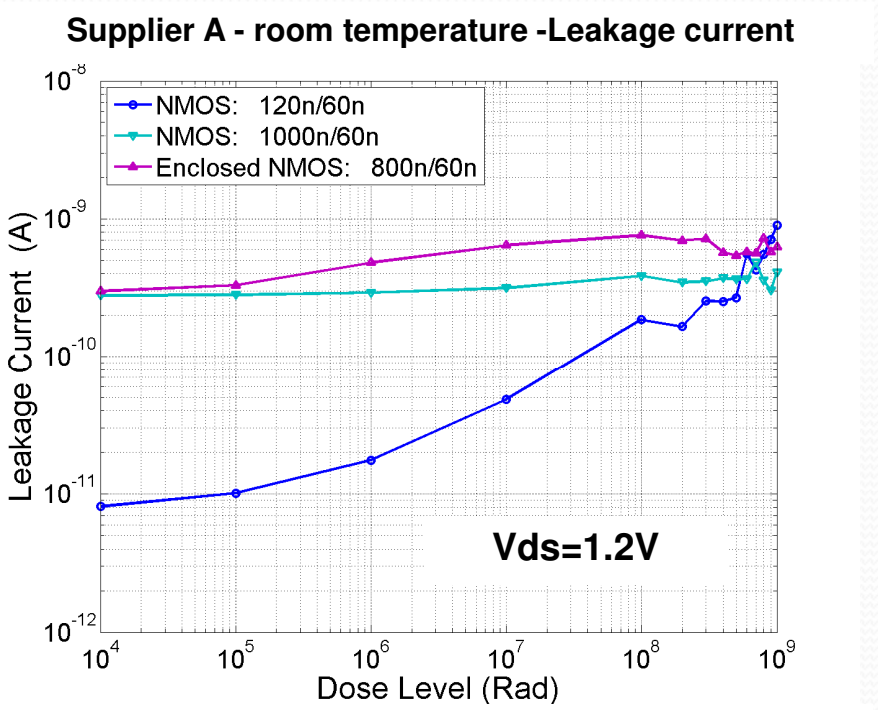
- Test at room Temperature
- Only core transistors (thin oxide) are considered
- Characteristics drawn for :
  - linear region (Vds = 50mV)
  - saturation (Vds =1.2V)
- Leakage current variation
- On state current variation
- Threshold voltage shift
- Transconductance variation
- Sub-threshold slope variation :
  - Identify the effect of oxide traps Not and the effect of the interface traps Nit

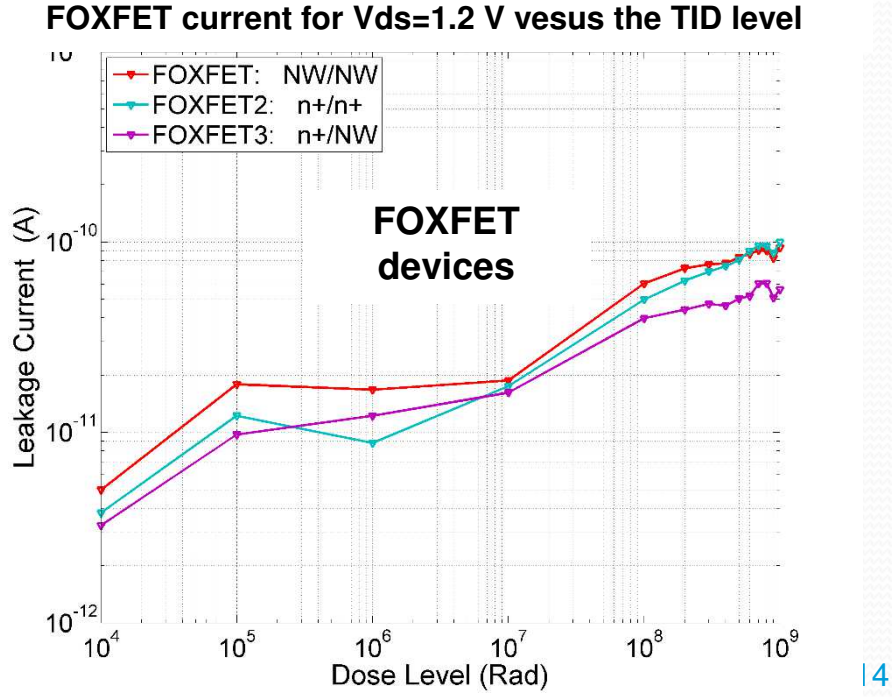


# Leakage current Measurements

- Device with 120nm/60nm (the narrower one) shows the highest increase in leakage :
  - Parasitic device more influent
  - ~ 2 orders of magnitude for the level of 1000 Mrad
  - The leakage value is below 1 nA
- Different FOXFET structures have been tested (NW/NW, n+/n+ and n+/NW)
  - The current increase is low
  - The increase of the Inter-device leakage is also limited
- For this 65nm process, the increase of the leakage current is very limited
- The enclosed layout is not needed



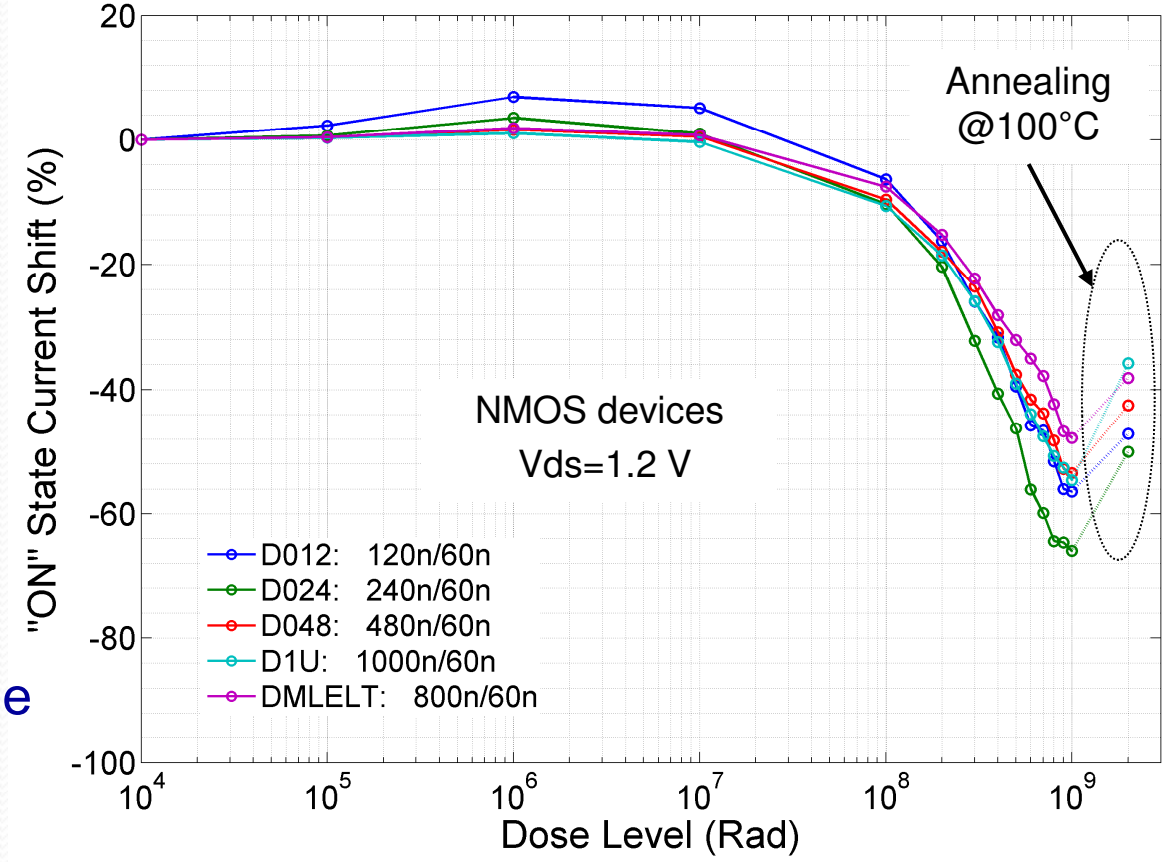



# NMOS devices irradiation

- "ON" state current : Drain current measured for $V_{GS}$ = 1.2 V
- A high loss in the ON state current for all tested devices from a dose level of 100 Mrad
- At 1 Grad, the loss is near 60 % for the "open geometry" devices
  - Related to the threshold shift which reaches a value of 350 mV
  - Damage depends little on the width
  - ELTs degrade as well
  - The RISCE can be considered as the main cause of this degradation
- 100°C annealing allows some recovering

**Supplier A room temperature**

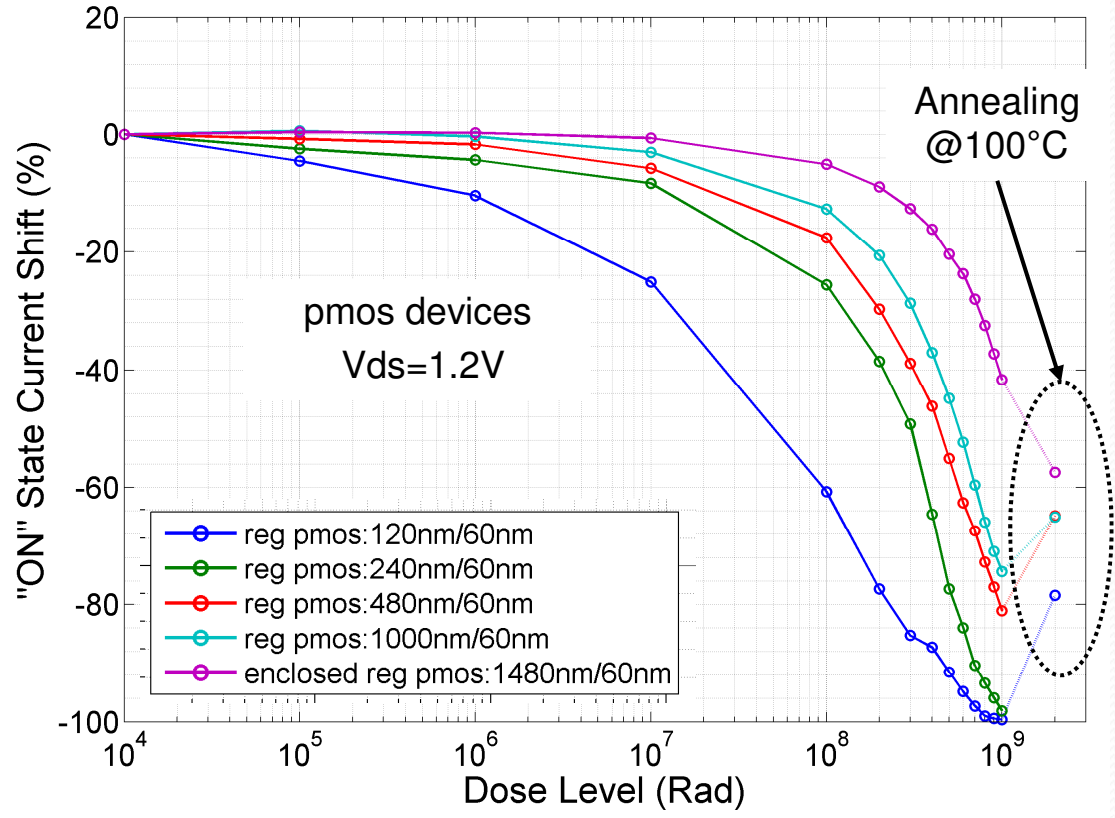
**NMOS devices : ON state current versus the TID for**



# PMOS devices irradiation

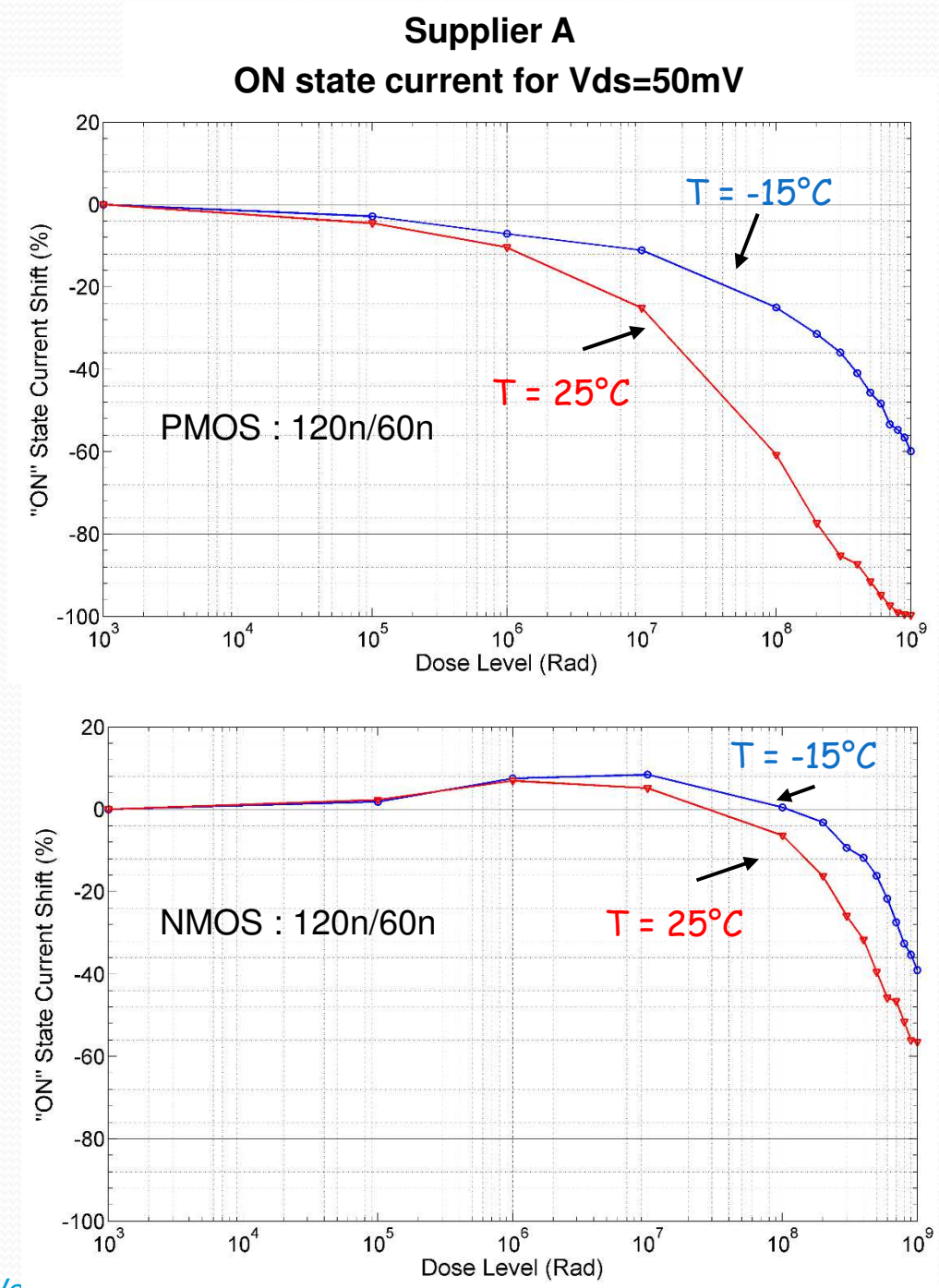
- More degradation than the nmos device
- At 1 Grad : “ION” decreases by ~100% for W=120nm and 240nm . The device becomes ‘OFF’ .
- Mainly because of the decrease of the tranconductance (mobility). No threshold Voltage shift observed
- The effect of the width is clearly visible for PMOS
- ELTs degrades as well but less than the “open geometry” devices
  - Only a part of the degradation can be explained to the charge trapped in the STI device (RINCE)
  - The other part can be explained by spacers oxide trapped charge (RISCE)
- Annealing at room temperature allow a very slow recovery
- Annealing at high temperature (100°C) :
  - The transconductance recovers well but Vth increases
  - The Vth shift is ~ 0.45 V for the narrower device

**Supplier A – room temperature**
**Pmos devices : ON state current versus TID**



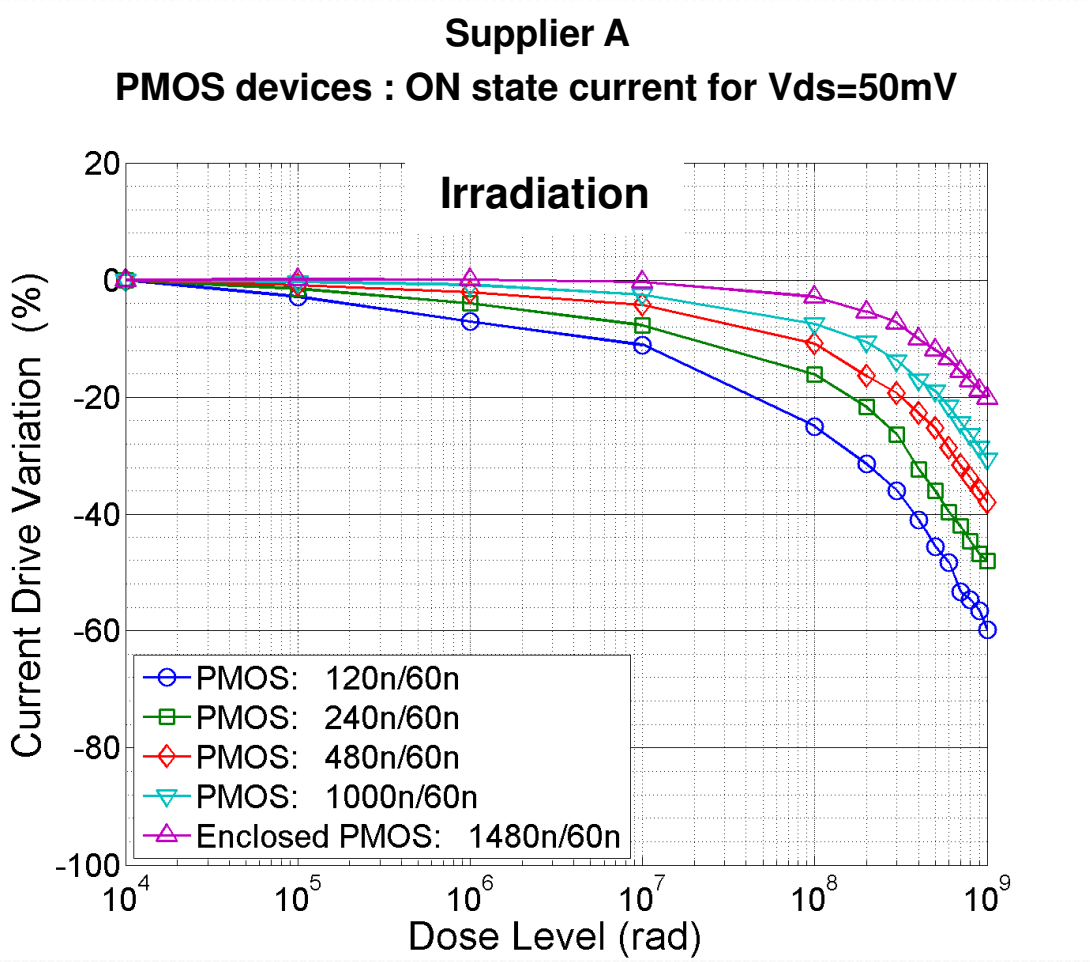
# Temperature effect during the irradiation

- Irradiation were conducted at low temperature (-15°C) for the 65 nm process
  - Less degradation of the PMOS transistors at -15°C than at room temperature
  - NMOS devices show also less degradation at higher doses
- The effect was explored in the temperature range of -30°C to 60°C
  - Radiation damage increases for NMOS and PMOS with temperature in this explored range
  - Applied bias is relevant at room and high temperature but it is negligible at cold temperature

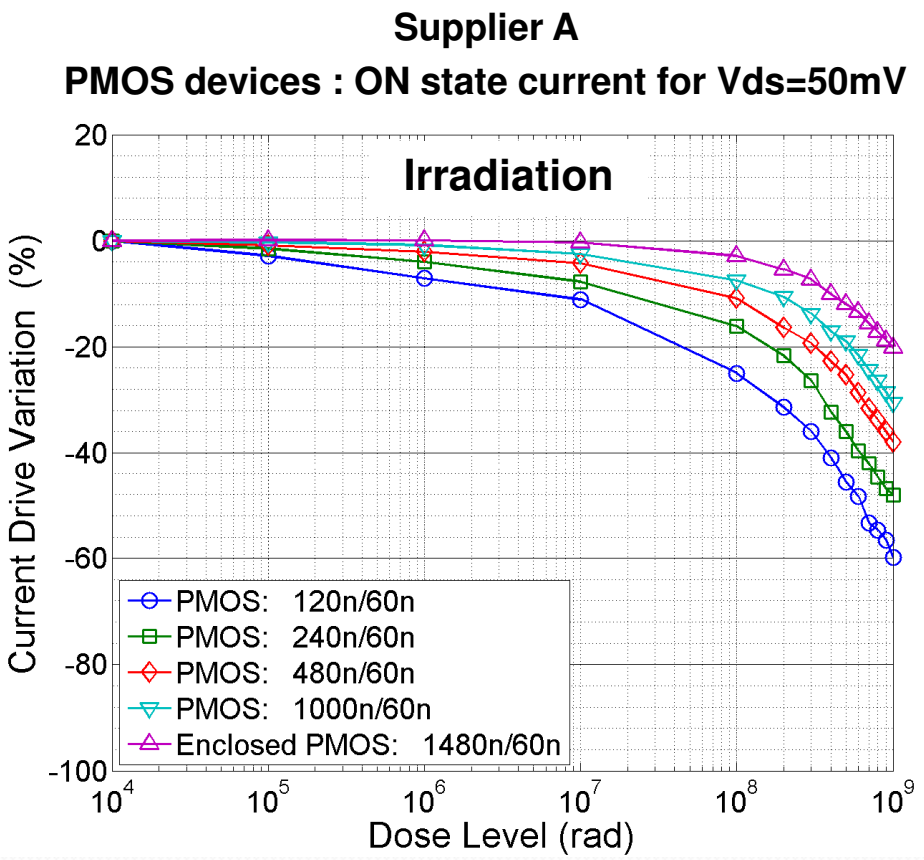


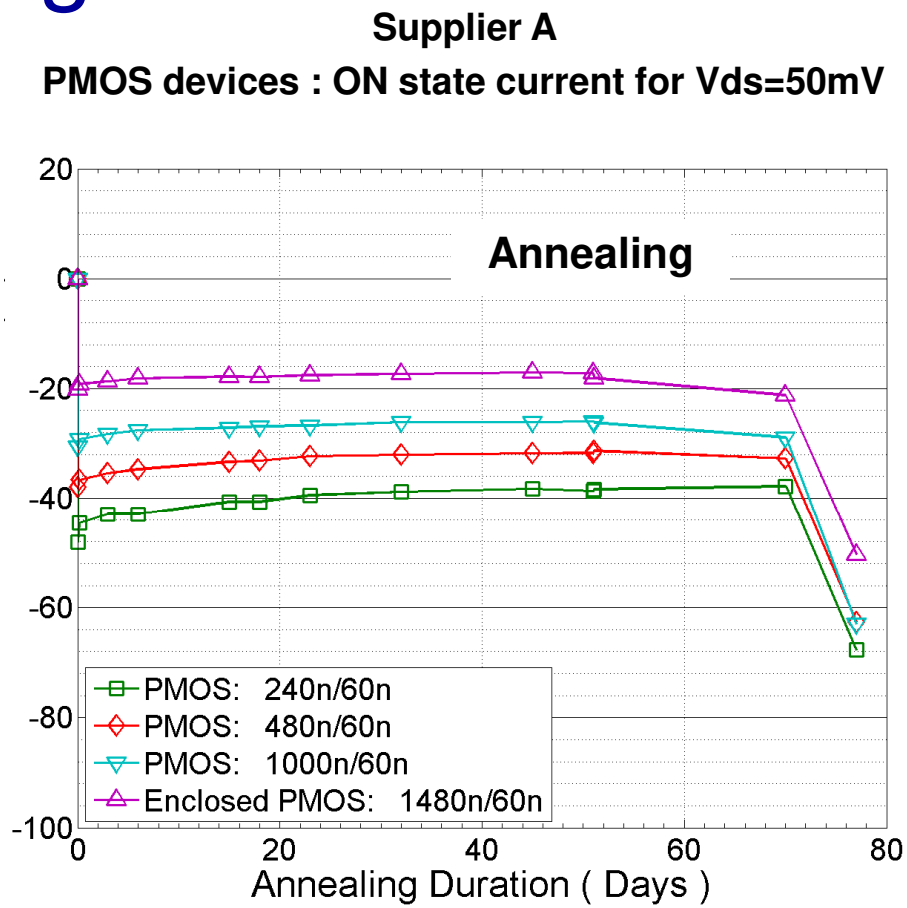
# Annealing Effect

- Less damage for the PMOS device when Irradiation is done at low temperature
  - Parameters shift does not compromise the digital design functionality
- This TID testing and qualification is performed at a High Dose Rate (HDR) of 9 Mrad/hour
- Several orders of magnitude higher than the Low Dose Rate (LDR) expected for the actual HL-LHC environment
- In general, the qualification for LDR consists in performing HDR testing followed by the high temperature annealing under bias



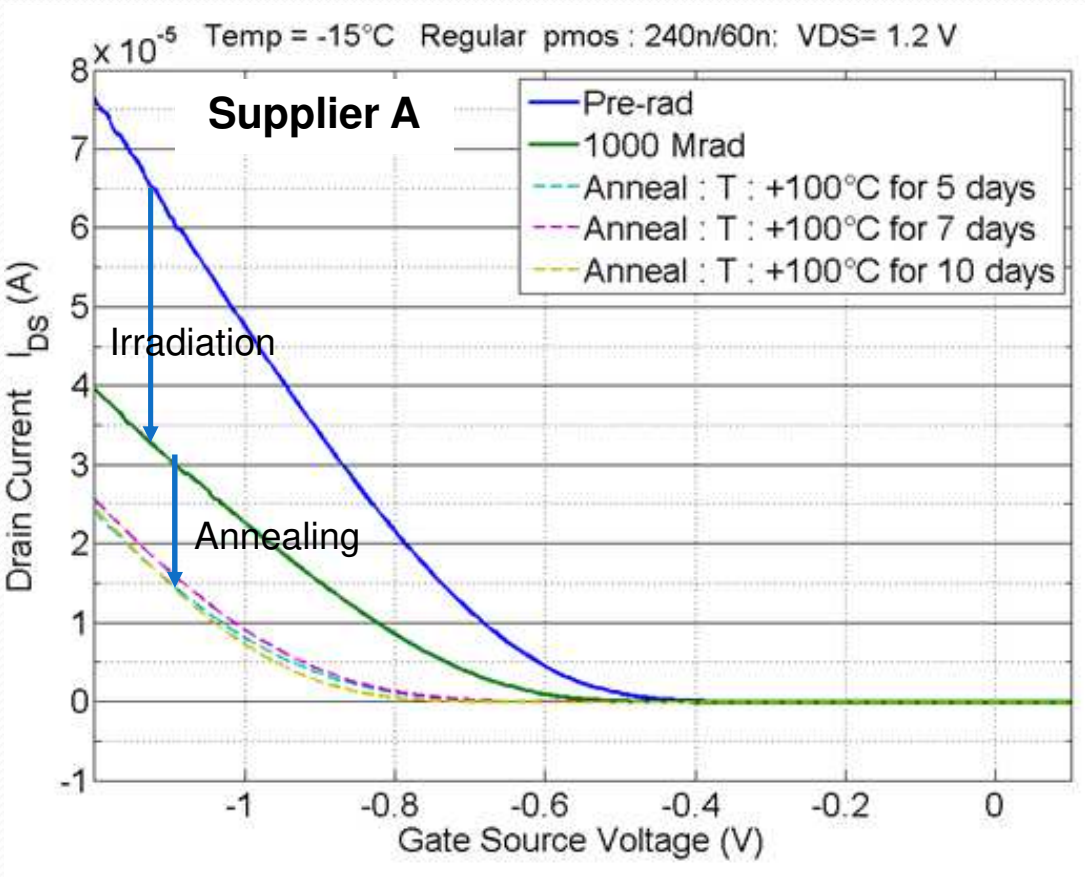
# Annealing Effect

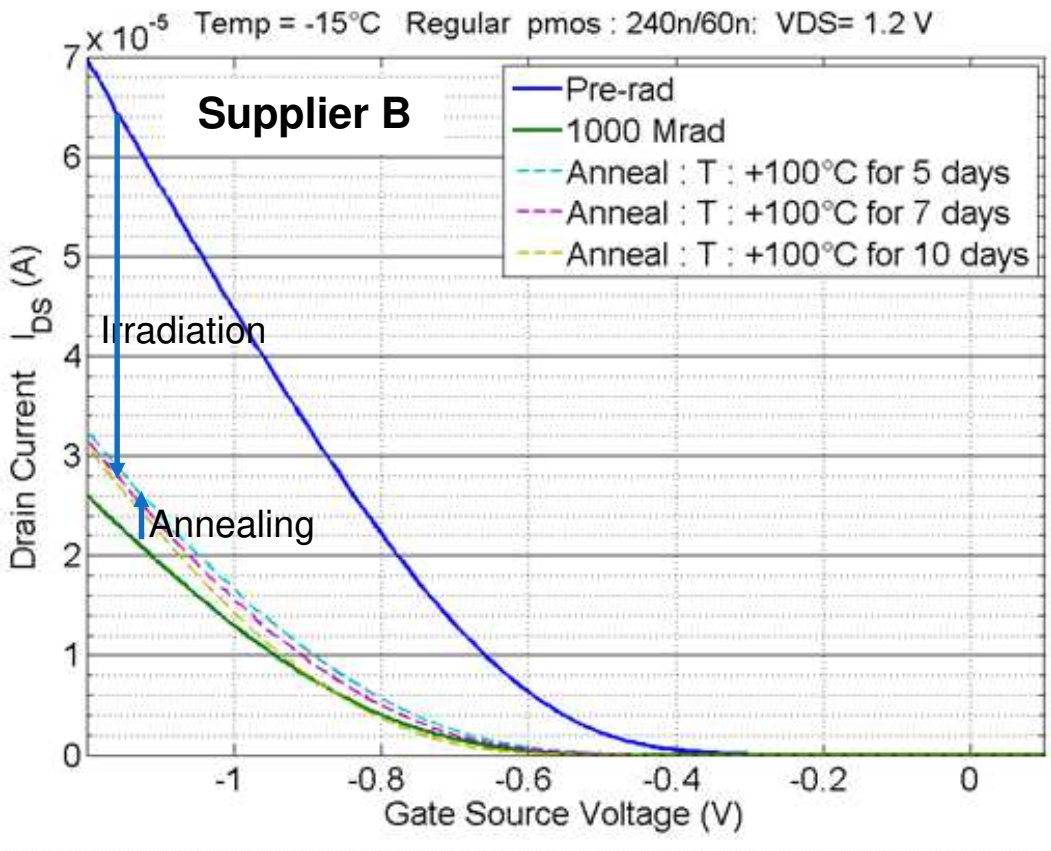



- A slight recovery is observed at low and room temperature annealing
  - The driving current loss improves from 45% to 38% for the 240nm/60nm
- High temperature annealing (100 °C for 7 days) degrades strongly the DC parameters
- This degradation comes from the increase of the threshold voltage
  - An increase of 0.28 V with respect the pre-irradiation value for the 240nm/60nm device

# Other 65 nm process

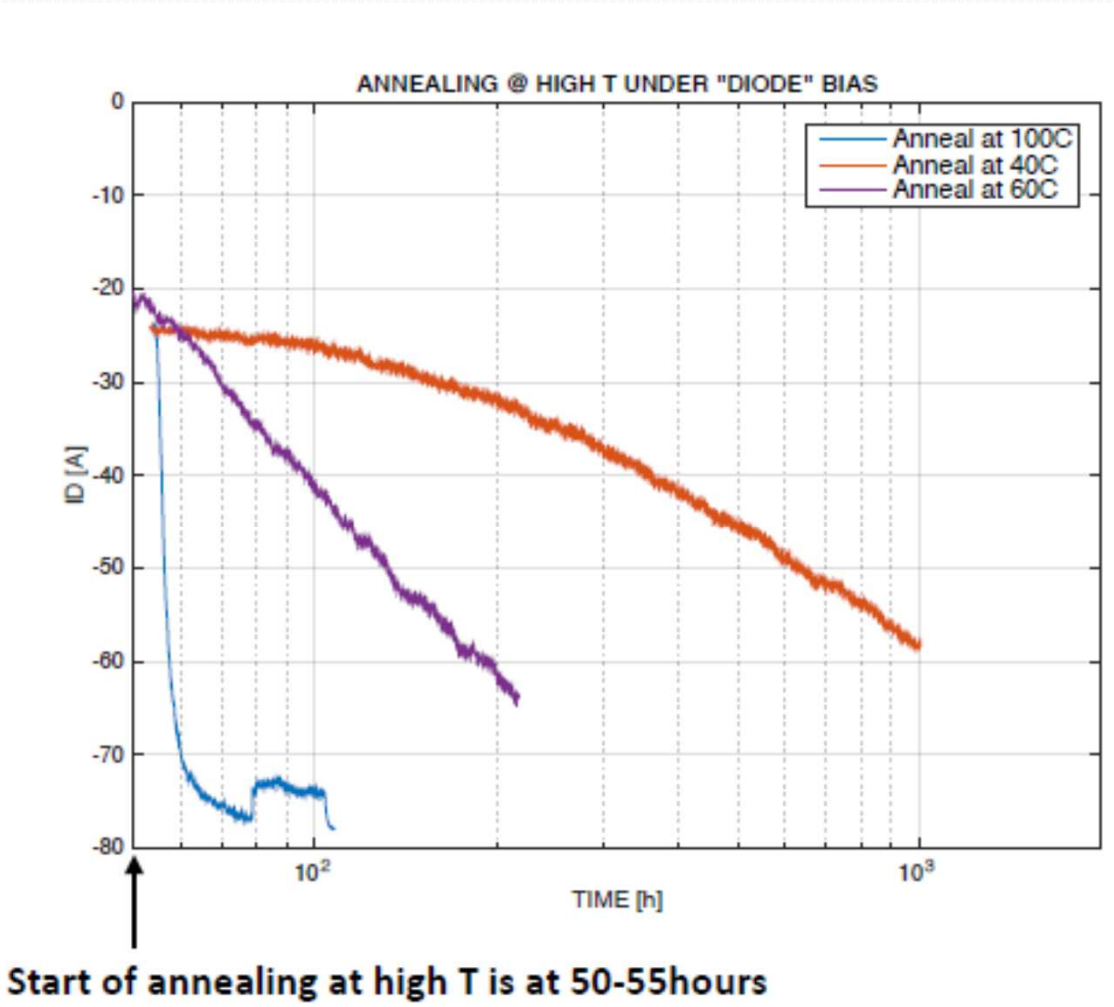



- The same irradiation test was performed on other 65 nm process at -15°C for a TID of 1 Grad
- Irradiation at HDR was followed by annealing at 100°C
- Process B : Similar irradiation results for 1 Grad but no Vth shift observed for annealing at 100°C
- The 65nm process B presents however a very high leakage for NMOS

# The Annealing Effect

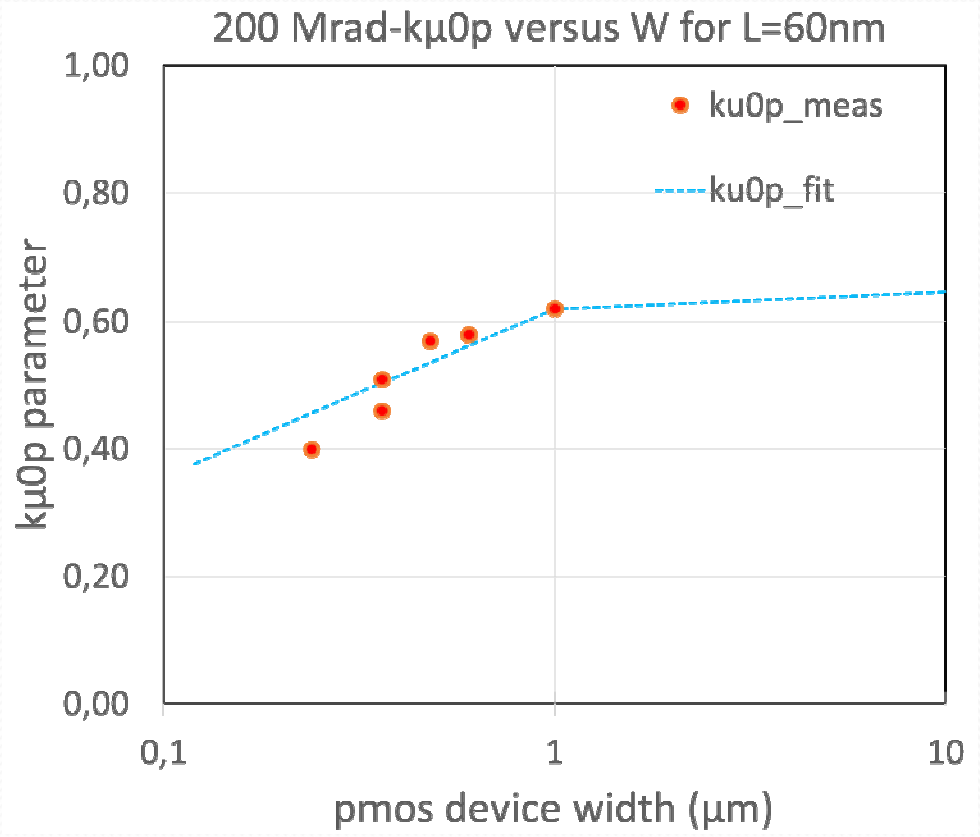
- Qualification and annealing for different temperature were done at CERN
- The Vth shift of the PMOS device is a thermally activated process
- Extrapolation for lower temperatures :
- This bad effect can be avoided or delayed by keeping cold :
  - -20°C for 10years
  - Room temp for few months (if unbiased)
- Irradiations at lower dose rates are ongoing at CERN
  - Check if there is really more damage at LDR
- Need to establish a hardness assurance methodology to guarantee that the devices can work reliably in the HL-LHC environment
- Knowledge of all the mechanisms underlying the radiation response

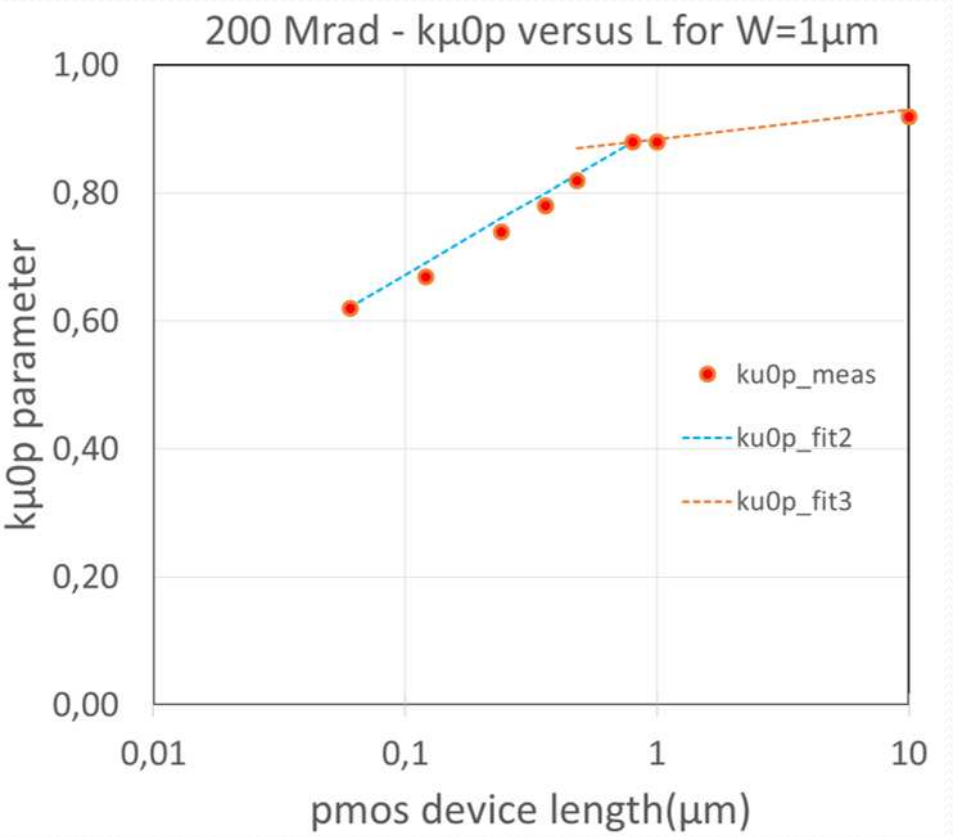



**Start of annealing at high T is at 50-55hours**

# Irradiation effects Modeling

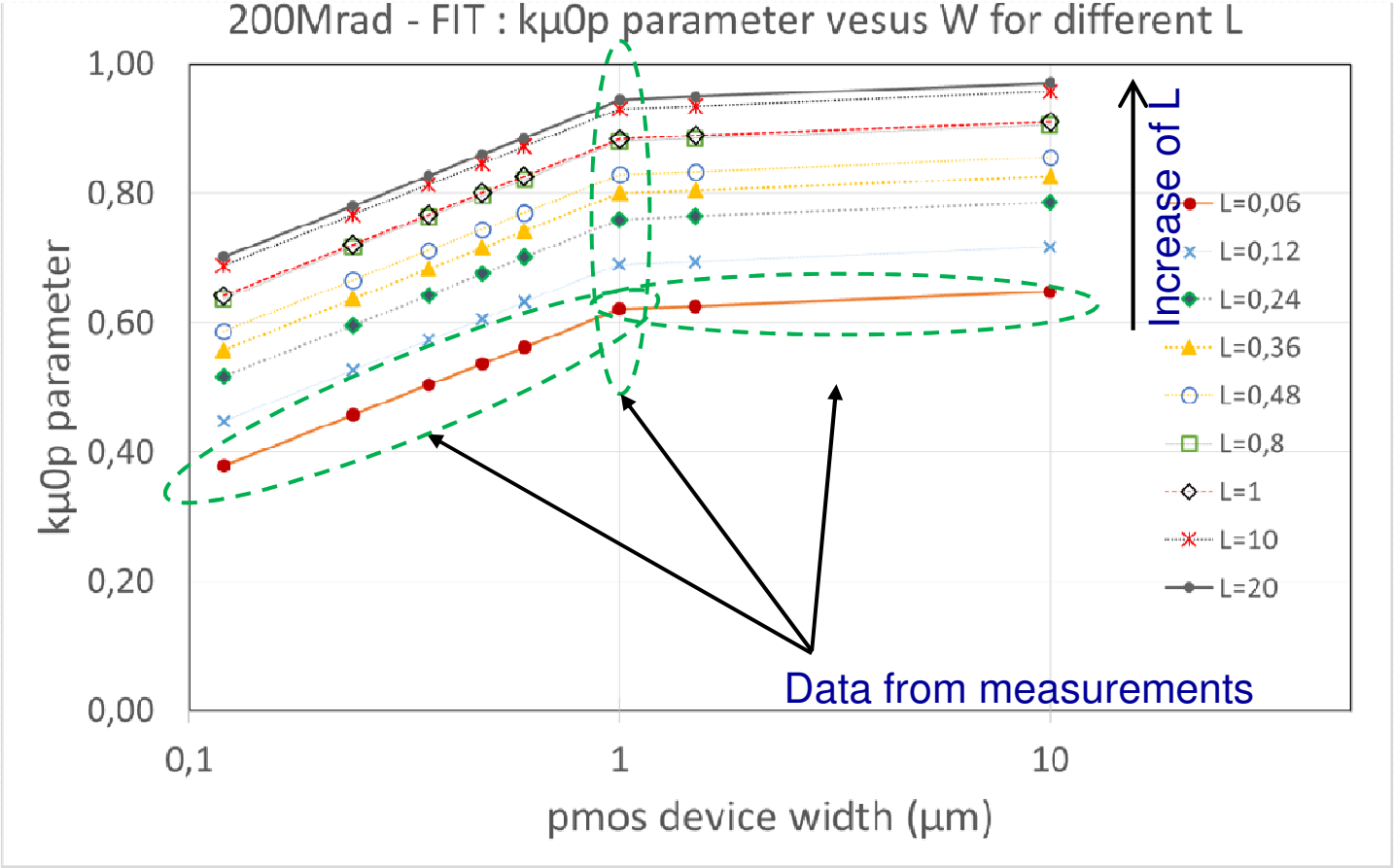
# PMOS fitting parameters




- The current drive loss depends strongly on the device width W and on length L
- A large part of data used in the fit (200 Mrad and 500 Mrad) were provided by Stefano Michelis (CERN)
- For PMOS devices only the transconductance degradation is considered (Annealing is not included)
- The mobility factor kμ0p is defined as the ratio μ0_rad/μ0_prerad
- kμ0p depends on W and on the L

# Pmos fitting parameters



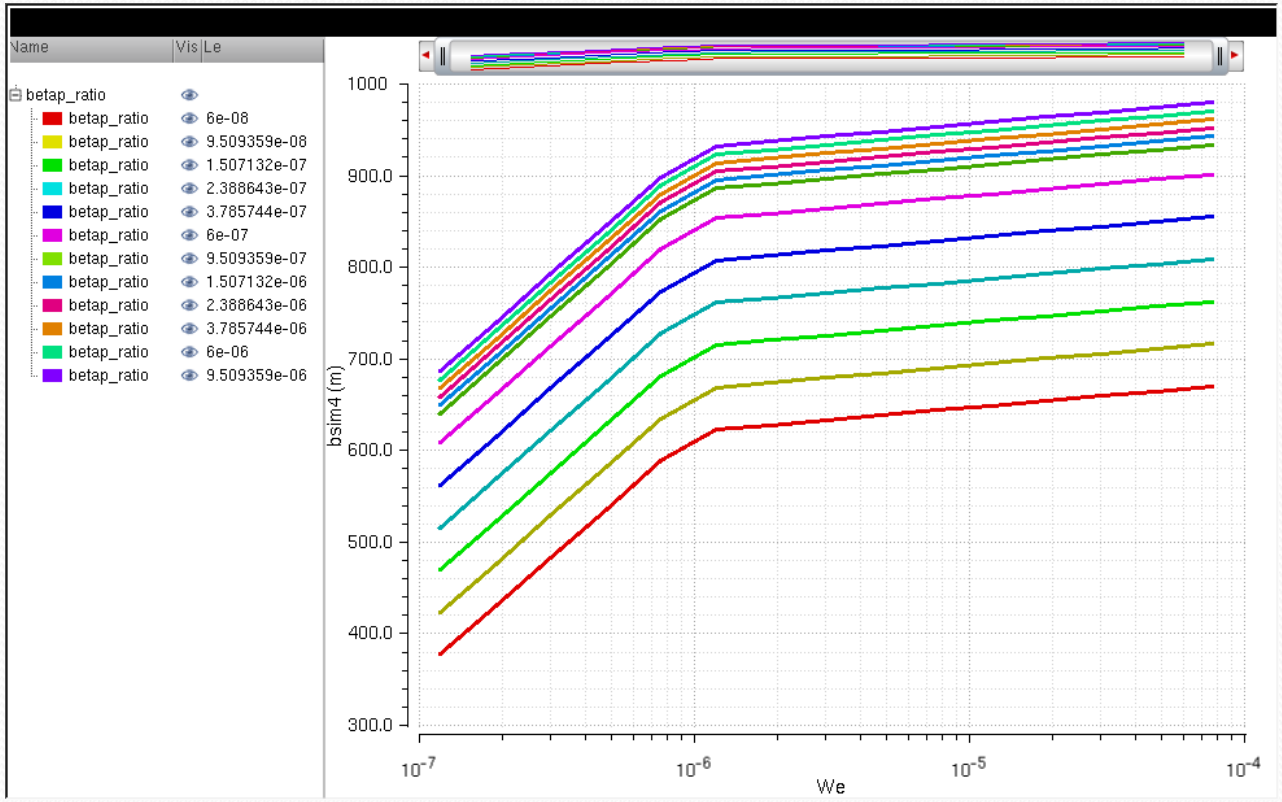

- kμ0p relation to W and L is implemented inside the TSMC spectre model file
- Assumptions :
  - The variation of kμ0p versus L measured only for W=1μm
  - This variation is assumed valid regardless the value W

# Other included effects

- Short channel effect are included for NMOS devices :
  - 60nm<L<240nm
  - Vth dependence on Vds is accentuated by irradiation
- Subthreshold swing change for small size NMOS devices
  - 60nm<L<240nm
- Leakage current is also implemented

- Experimental data exists only for Regular VT devices : RVT
  - HVT and LVT extrapolated from RVT devices measurements
- Assumptions :
  - Room temperature irradiation
  - Worst case biasing (VDS=VGS=1.2V)
  - No annealing (Based on High Dose Rate results only)
- 2 Model Corners were developed : 200 Mrad and 500 Mrad

# Virtuoso spectre simulations

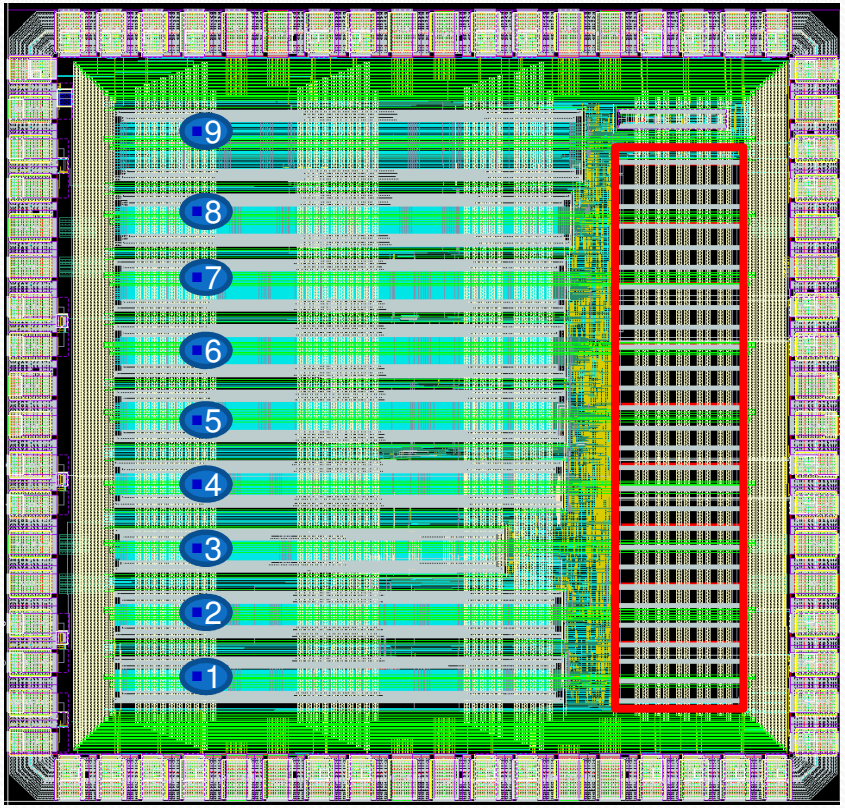



- PMOS devices :
- Simulation of kμ0= beta_irrad/beta_prerad versus W for different values of L
- Variation is as expected

# DRAD : Test chip for digital design

# DRAD Chip : Test chip for digital design

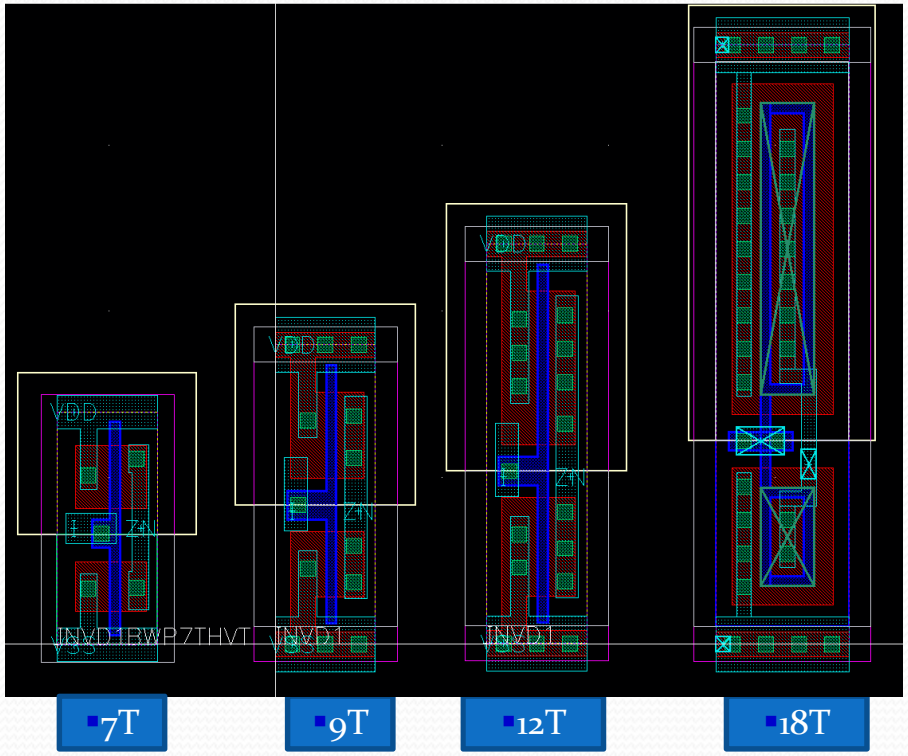
- DRAD chip is designed to study the effect of radiation on digital standard cells for the 65nm TSMC technology
- RD53
  - Dario Gnani, LBNL
  - Sandeep Miryala, NIKHEF
- MPA project
  - Davide Ceresa, CERN
- LPGBT Group (18T LVTELT)
  - Szymon Kulis, CERN
  - Rui Francisco, CERN
- Test Set up and Test Results
  - Luis Miguel Jara Casas, CERN



# Various Digital Libraries

- 7 Track (7T)
  - High Vt (HVT)
- 9 Track (9T)
  - Regular Vt, High Vt
  - Regular Vt with increased width
- 12 Track (12T) (Modified)
  - Regular Vt, Low Vt
  - High Vt
  - Regular Vt with L=130n
- 18 Track (18T) (Custom)
  - Enclosed layout transistors, for LPGBT grp.

FOUNDRY




**CELL HEIGHT**

7 Track: 1.4 uM

9 Track: 1.8 uM

12 Track: 2.4 uM

18 Track: 3.6 uM

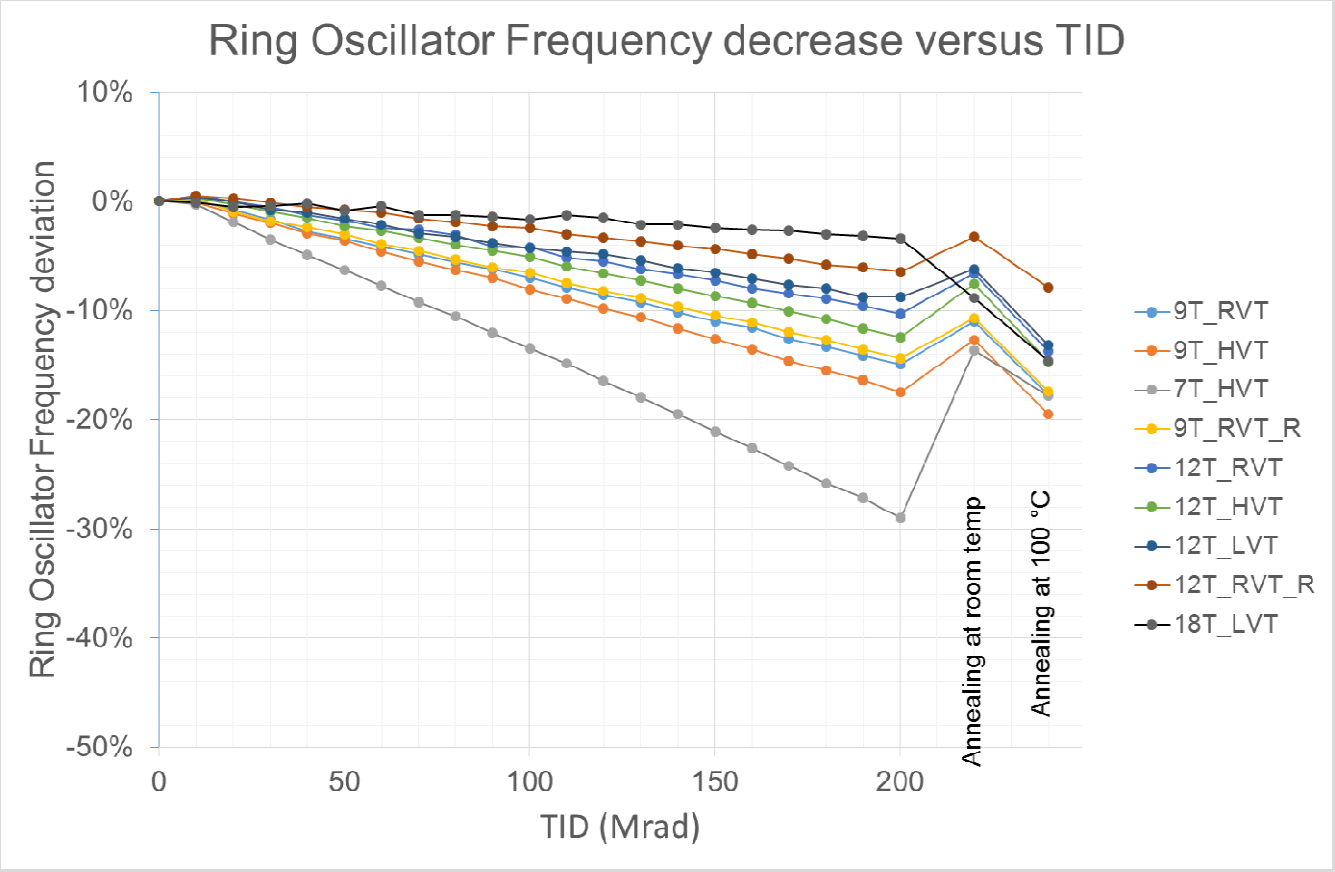
# Digital Library Information

- Library characterization
  - Cadence Liberate based on the spectre model for 200 and 500 Mrad
- Timing
  - Combinational
    - Delay
    - Transition time
  - Sequential
    - Delay & Transition time
    - Hold & Setup
    - Recovery and Removal
- Power
  - Leakage : Static power
  - Internal Power

Different standard cells implemented for each library

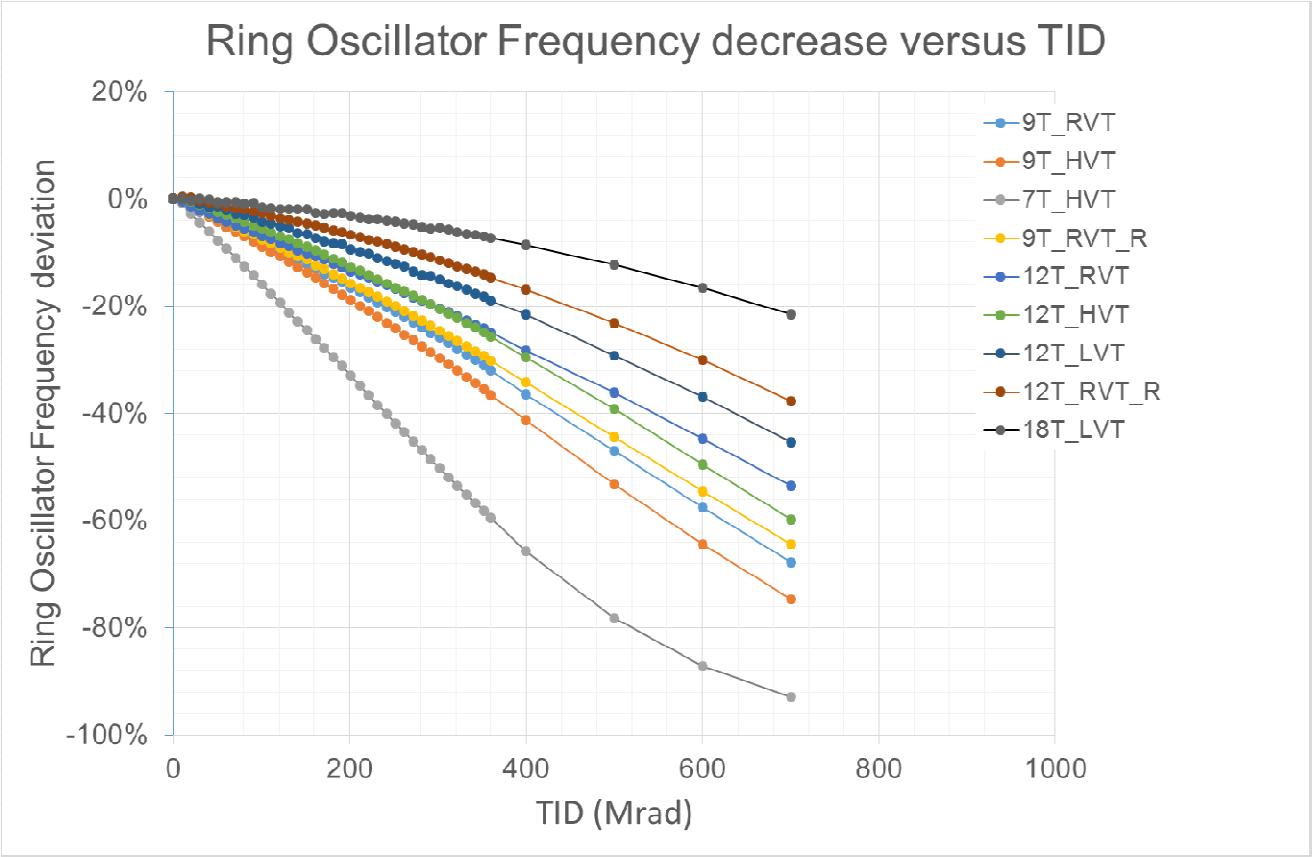
| STANDARD CELL NAME | DESCRIPTION |
|---|---|
| INVD1 | Inverter with driving strength = 1 |
| INVD4 | Inverter with driving strength = 4 |
| ND2D1 | 2-input NAND gate with driving strength = 1 |
| ND4D1 | 4-input NAND gate with driving strength = 1 |
| NOR2D1 | 2-input NOR gate with driving strength = 1 |
| NOR4D1 | 4-input NOR gate with driving strength = 1 |
| XOR2D1 | 2-input XOR gate with driving strength = 1 |
| CKBD1 | Clock buffer with driving strength = 1 |
| CKBD4 | Clock buffer with driving strength = 4 |
| CKBD16 | Clock buffer with driving strength = 16 |
| DFCNQD1 | Flip-Flop with async clear with driving strength = 1 |
| LHCNQD1 | Latch with async clear with driving strength = 1 |

# Results for 200 Mrad




- The relationship of the behavior between libraries is as expected :
  - Libraries with smaller size behave worse than large ones
  - Libraries with higher Vt behave worse than libraries with low Vt.
- High temperature annealing creates more damage
- Different behaviour after room temperature annealing for 18T_LVT library (ELT transistors)
- 7T_HVT more sensitive but recovers better (in %) respect the rest of the libraries.

# Results for 500 Mrad




- Irradiation at 500 Mrad at room temperature
- Results without annealing (HDR)
- Irradiation tests for 500 Mrad with room and high temperature annealing will be done

# Test Results

- Simulation results goes in the same direction than irradiation tests
- In general simulations give worse results than measurements (Models were done for worst case of biasing)
- Digital libraries: Plans for RD53 chip
  - High density digital cells have significant radiation degradation at 500Mrad
    - Dominated by PMOS degradation
  - Choose the library to use for high density Pixel array
  - Choose the library for “High speed” logic in EOC
  - 200 Mrad, 500 Mrad Liberty files for synthesis, timing verification and digital simulation
- DRAD test chip presented as poster at TWEPP by Luis Miguel Jara Casas (CERN)

# Summary

- The 65 nm process tested to 1 Grad
  - Very limited increase of the leakage
  - At ambient temperature, a strong drive loss for narrow pmos devices
  - The irradiation tests at low temperature (pixel chip environment) show less damage
  - High temperature annealing increases the threshold of the PMOS
- Corner Models developed : 200 Mrad and 500 Mrad
  - Based on HDR test results - Room temperature - Worst case biasing
- DRAD chip is designed to study the effect of radiation on digital standard cells :
  - Large devices -> better time margins
  - Choose the appropriate libraries for the RD53 readout chip
  - 200 Mrad and 500 Mrad Liberty files will be used for synthesis, timing verification and digital simulation
- Define a hardness methodology to guarantee that the tested devices can work reliably in the HL-LHC environment
- Radiation tolerance can variate for the same process between different Fabs, and can change over time
  - Qualify and use one Fab - qualify each ASIC during the prototyping and production phases

Thank you for your attention

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