Contribution ID: **72** Type: **Invited Talk**

Radiation Tolerance of 65nm CMOS

Thursday 29 September 2016 16:30 (22 minutes)

The High Luminosity LHC (HL-LHC) is the proposed upgrade to the LHC to be made in a long machine shutdown which should take place in the years 2023 to 2025, according to current schedule and aims increasing the luminosity of the machine up to 5.1034 cm−2s−1. The upgrade will improve statistically marginal measurements and will allow a better chance to see rare processes.
The ATLAS and CMS experiments are planning major detector upgrades to cope with the increase in beam luminosity. Pixel detectors are placed in the innermost part of the experiments and are therefore exposed to the highest fluences and highest ionizing radiation doses. Simulations show that the innermost parts of the new pixel detector will integrate a fluence of about 1016 n/cm2 (1 MeV neutron equivalent) and a Total Ionizing Dose (TID) of 1000 Mrad.
The RD-53 collaboration was established to develop the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC. This development requires extreme rate and radiation tolerance. The 65 nm CMOS process seems to be promising for the future pixel readout chips in terms of high integration density and a first demonstrator chip containing 76 800 pixels of 50μm × 50 μm will be submitted in April 2017 .
The first part of this presentation is dedicated to the TID effects on the 65nm process. A lot of information about the 65 nm process tolerance were obtained by studying radiation effects on individual transistors and used as a way to understand the causes of failure in digital or analog designs. In fact, the radiation tolerance of 65 nm bulk CMOS devices was investigated using 10 keV X-rays up to a Total Ionizing Dose (TID) of 1 Grad and irradiation tests were performed at room temperature (25 ℃) as well as at low temperature (-15 ℃).
In principle, the gate oxides of advanced CMOS technologies are scaled to thinner dimensions, which should make devices highly tolerant to TID effects. However, irradiation tests showed a strong performance degradation for the small size devices. In fact, the Shallow Trench Isolation (STI) used as the field oxide for device isolation and represents the main issue when considering TID effects for scaled down technologies.
We will review the various degradations induced by the STI charge buildup. The first degradation is related to the leakage current in the irradiated NMOS devices and caused by the parasitic STI device. The second type of degradation concerns the threshold voltage shift of narrow channel devices. The effect, intitled "Radiation-Induced Narrow Channel Effect"(RINCE) was already reported for other commercial processes. Furthermore, For this 65 nm process, another effect was observed and designed as Radiation-Induced Short Channel Effect (RISCE). It is realated to the fact that degradation depends not only on the width of the channel but more degradation is observed for short channel than for long channel devices.
The effect of the bias and of the temperature during irradiation and during annealing will be discussed. In particular, high temperature annealing does not help recovering the current drive in irradiated devices. On the contrary, performance degradation is observed after high temperature annealing for PMOS devices. Very often, in irradiation qualification, the Low Dose Rate (LDR) dammage is estimated from the TID effects at a High Dose Rate (HDR) followed by high temperature annealing. For the 65 nm process, testing are carried out in order to estimate the dammage at LDR and to provide a methology for qualification and especially for the pixel detector which will function in a cooled area.
A methology for SPICE parameters extraction for radiation-induced degradation on pmos and nmos transistors is proposed. Comparison of radiation-induced leakage current, threshold shift and mobility degradation in test MOSFETs between total dose irradiation experiments and simulation results exhibits a good agreement.
The second part of this presentation is dedicated to the Single Event Upset (SEU) tolerance for the 65nm process. Indeed, for the future pixel readout chips, local and global memories are implemented to retain respectively the local pixel configuration and the global chip configuration. SEU tolerant memories are used to allow reliable operation at high beam intensities and to avoid reloading frequently the configuration data. A prototype chip has been designed where a different structures of the configuration memories based on Dual Interlocked CElls (DICE) or on Triple Redundancy Latches (TRL) were implemented.
SEU tolerance tests were carried out at CERN-PS facility with the 24 GeV protons beam. SEU measurements show that the DICE latch improves the SEU tolerance by a factor of 10 with only a small increase on the area compared to the standard latch, making the DICE suitable for pixel configuration whereas the TRL allows an improvement by a factor of 2500 but the structure consumes a higher area making it suitable only for global

configuration.

Author: MENOUNI, Mohsine (Centre National de la Recherche Scientifique (FR))

Presenter: MENOUNI, Mohsine (Centre National de la Recherche Scientifique (FR))

Session Classification: B13-Radiation hardness and simulations

Track Classification: Radiation hardness and simulation