# AFP Trigger DAQ and DCS

Krzysztof Korcyl
Institute of Nuclear Physics - Cracow

on behalf of TDAQ and DCS subsystems

# agenda

***LVL1 trigger***

full system project
AFP2+0 installation
current status and development

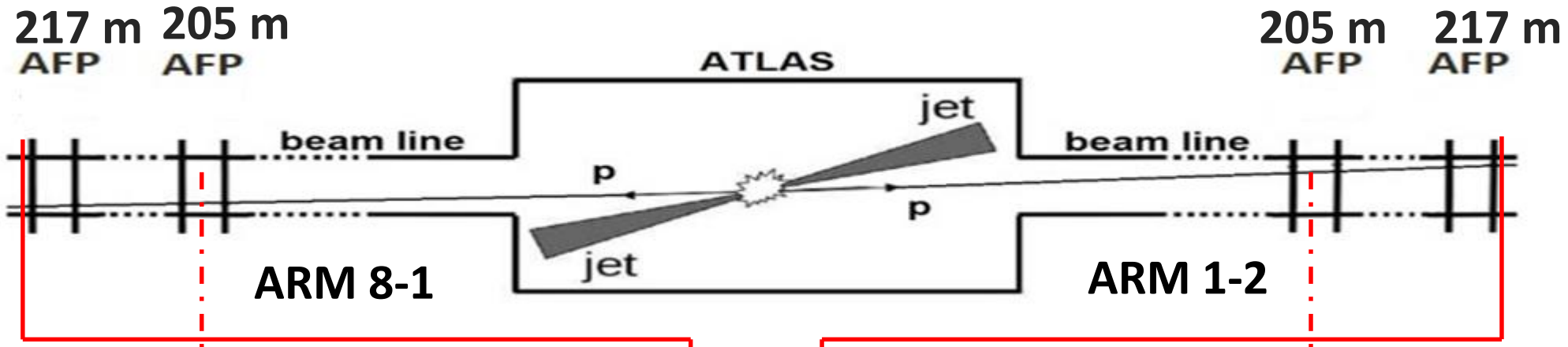
***DAQ***

full system project
AFP2+0 installation
current status and development

***DCS***

full system project
current status and development

# AFP LVL1 trigger




Current ATLAS L1 latency: **84** BCXs

Protons from P1 to 217 m: **29** BCXs

Fast air-core cable (300m): **43** BCXs

ATLAS CTP work: **6** BCXs

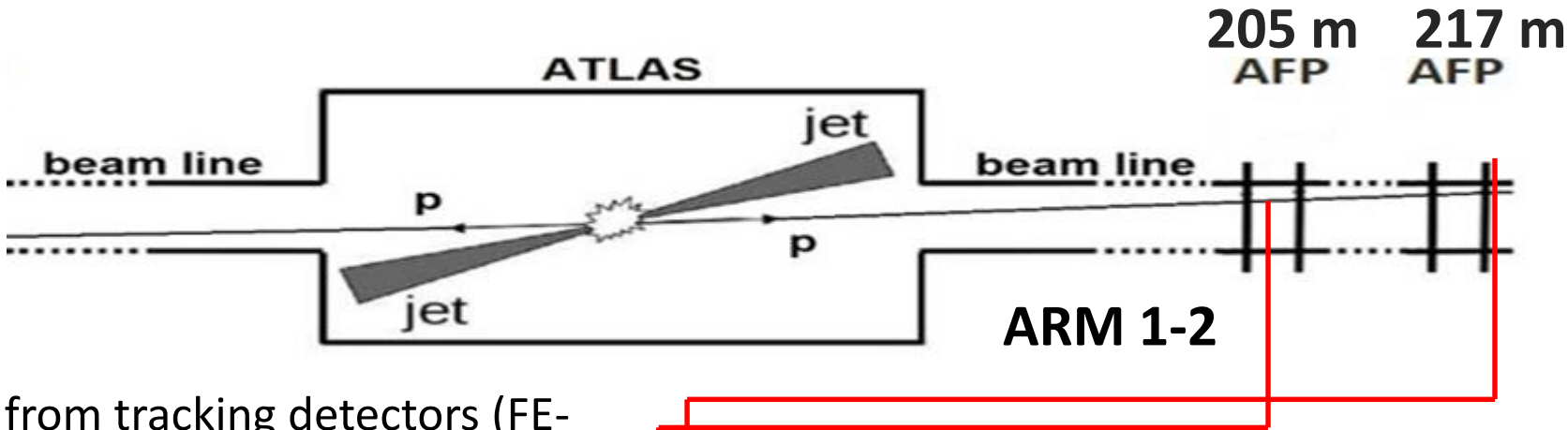
Trigger logic: **6** BCXs

NIM signals with encoded information from timing detectors

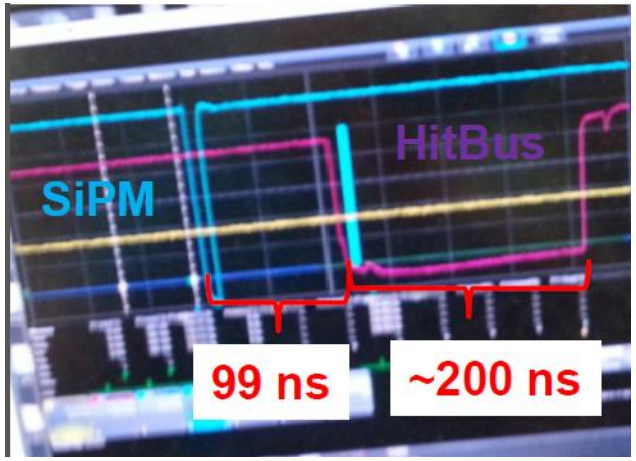
**AFP_CTPIN**

**ATLAS Central Trigger Processor**

# AFP2+0 LVL1 trigger



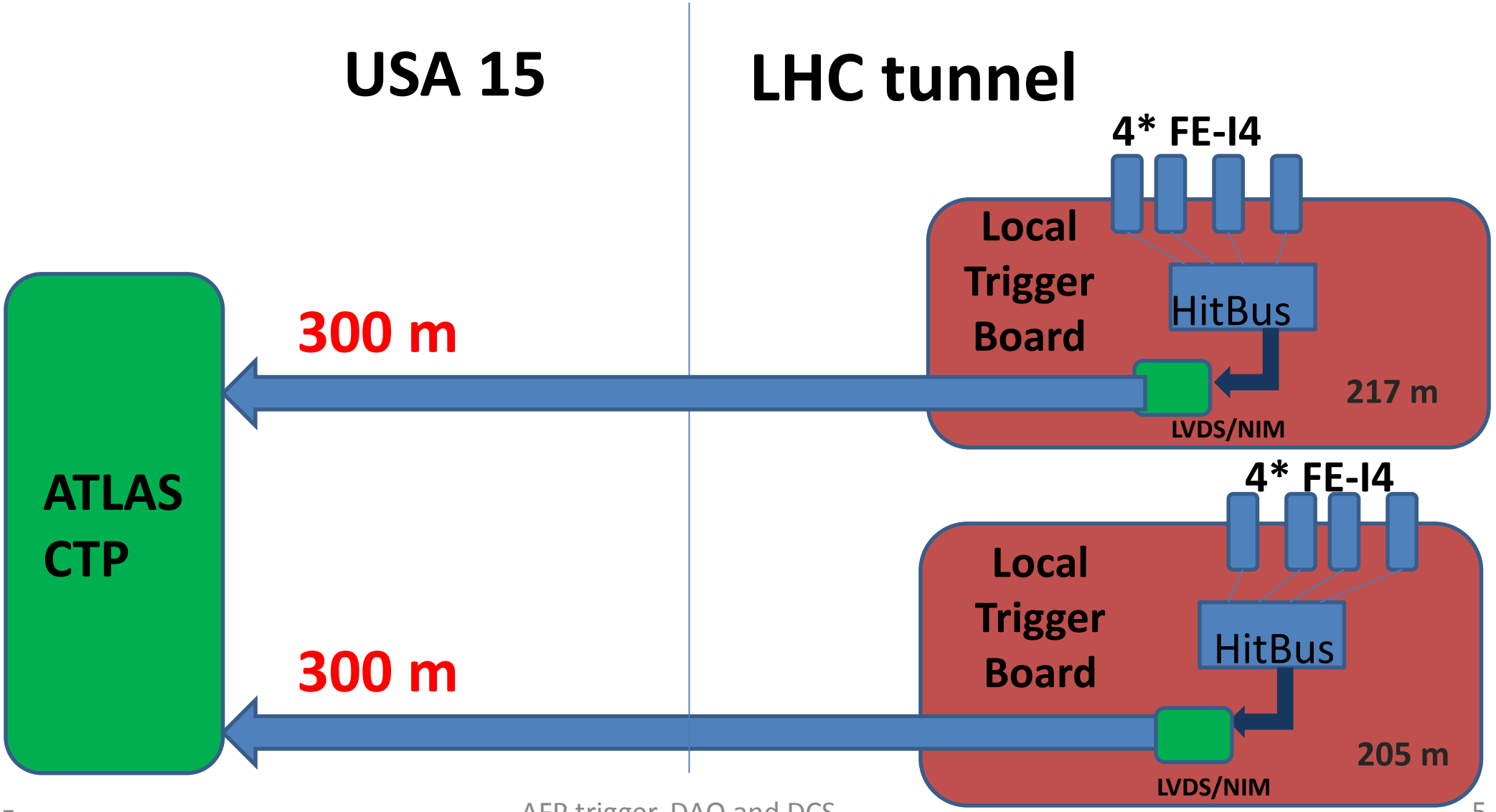

We plan to use signals from tracking detectors (FE-I4 HitOR output) and HitBus chip from DBM to make logic function (AND) from 3 out of 4 FE-I4 HitOR outputs




25 ns NIM signals from tracking detectors

**ATLAS**
**Central Trigger Processor**

# AFP0+2 LVL1 trigger setup

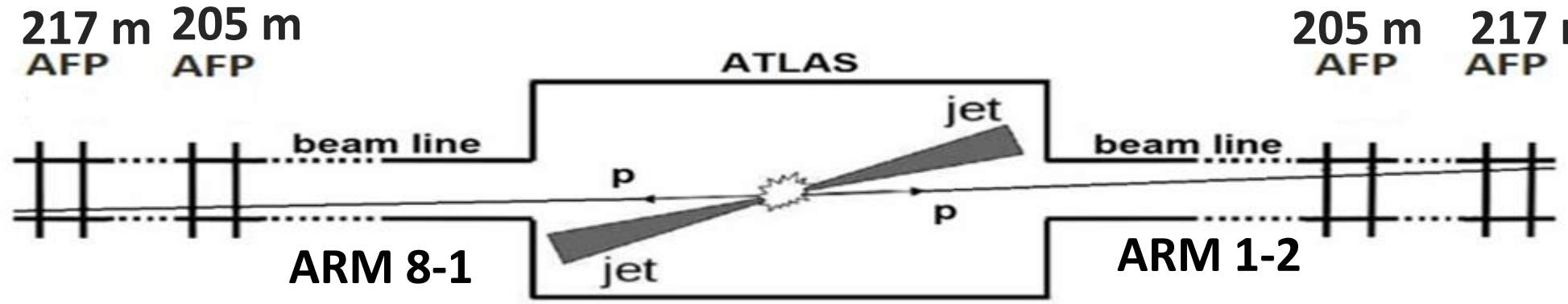


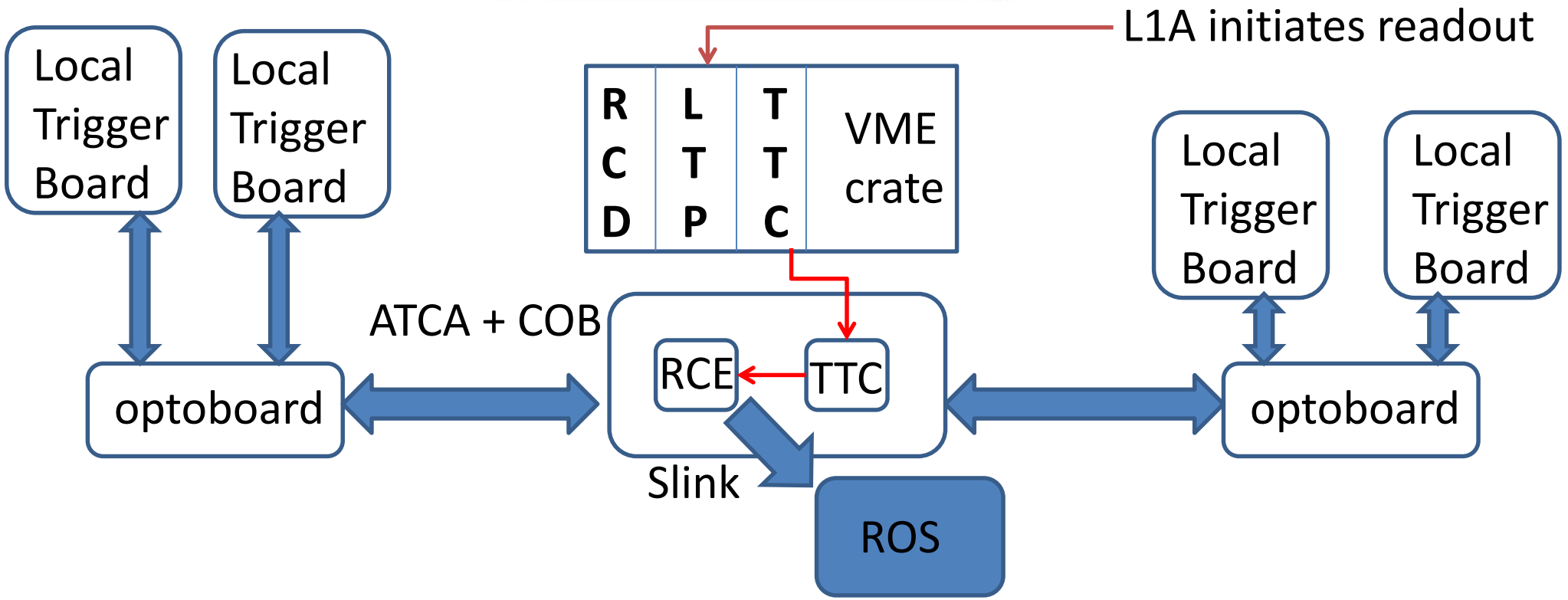
# AFP LVL1 trigger status and development

- during the beam tests we performed standalone runs with prototype of the Local Trigger Board (LTB) and parts of the ATLAS TDAQ system
  - VME crate with LTP and TTCvi
  - NIM output from the LTB was used by the LTP to produce L1A and start readout
    - falling edge of the trigger was used to generate L1A
  - HitOR trigger signal spans over 10 BCXs

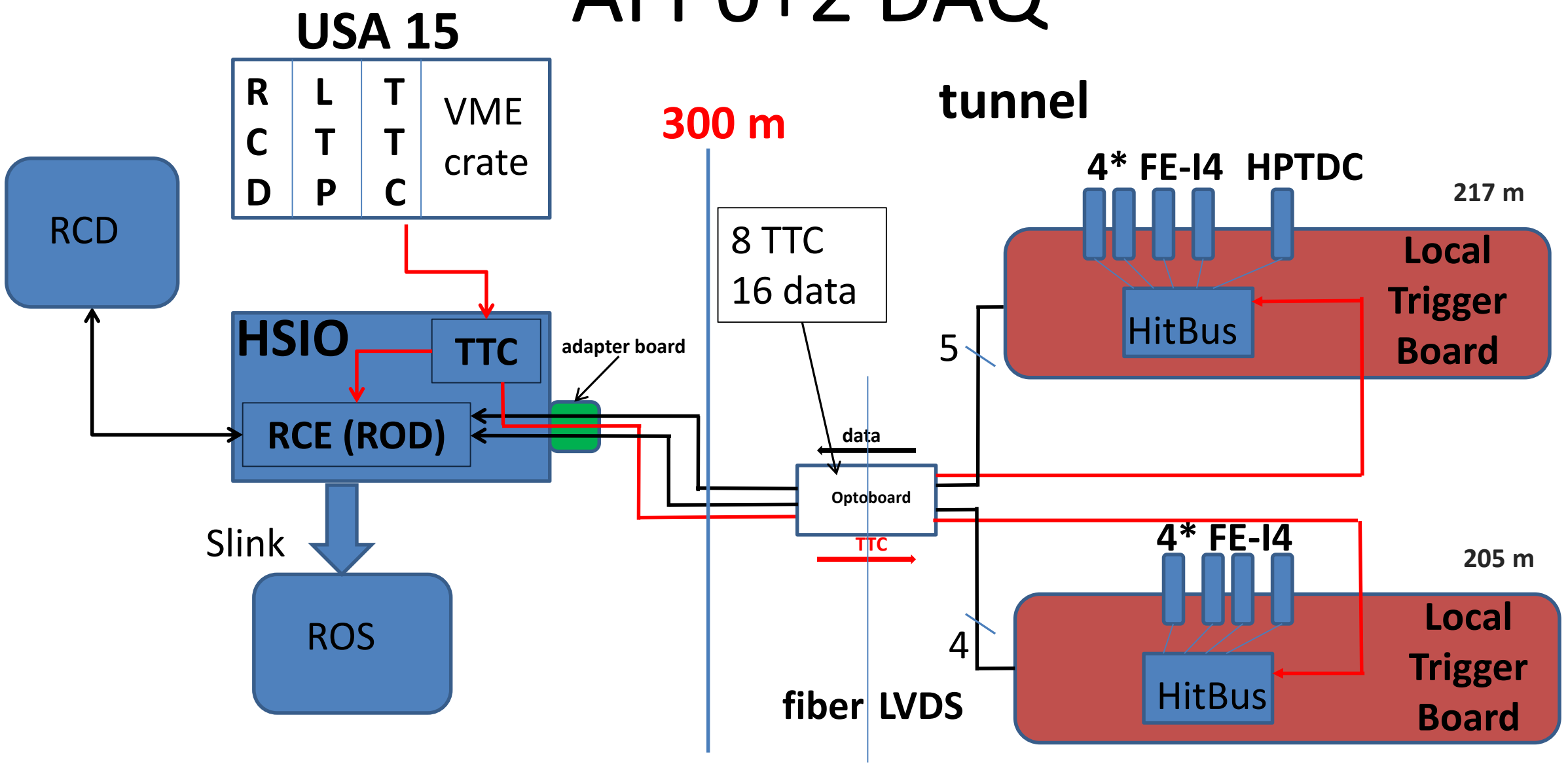
- new version of the LTB is being designed
- before installation of the air-core cables in the LHC tunnel we plan to send 25 ns pulses and verify signal quality at the other end of the cable

# AFP DAQ


217 m
AFP
205 m
AFP
ATLAS
205 m
AFP
217 m
AFP
jet
beam line
beam line
p
p
jet
ARM 8-1
ARM 1-2


L1A initiates readout
Local Trigger Board
Local Trigger Board
R C D
L T P
T T C
VME crate
Local Trigger Board
Local Trigger Board
ATCA + COB
optoboard
RCE
TTC
optoboard
Slink
ROS

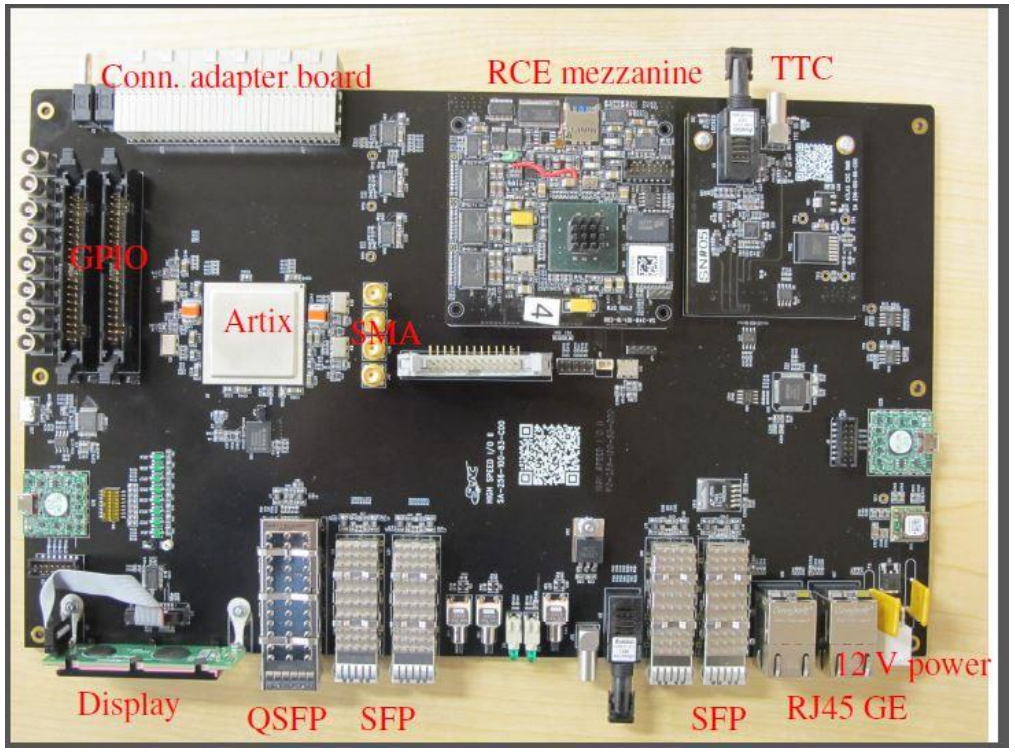
# AFP0+2 DAQ


USA 15
R C D
L T P
T T C
VME crate
RCD
300 m
tunnel
8 TTC
16 data
4* FE-I4 HPTDC
217 m
Local Trigger Board
HitBus
HSIO
TTC
adapter board
RCE (ROD)
5
data
Optoboard
TTC
Slink
ROS
4* FE-I4
205 m
Local Trigger Board
HitBus
4
fiber LVDS

# AFP DAQ status and development

- readout via HSIO:
  - integration with ATLAS TDAQ demonstrated during the beam tests
  - uses HSIO firmware (Artix) to serialize and format data before entering RCE
  - Event Building currently in software – likely will be put in FPGA
  - firmware for S-link (ROS) exists in CSC – needs to be ported to AFP
  - dedicated PC to run RCD controlling and monitoring RCE

HSIO board




- plan to build trigger/DAQ test setup in SR1

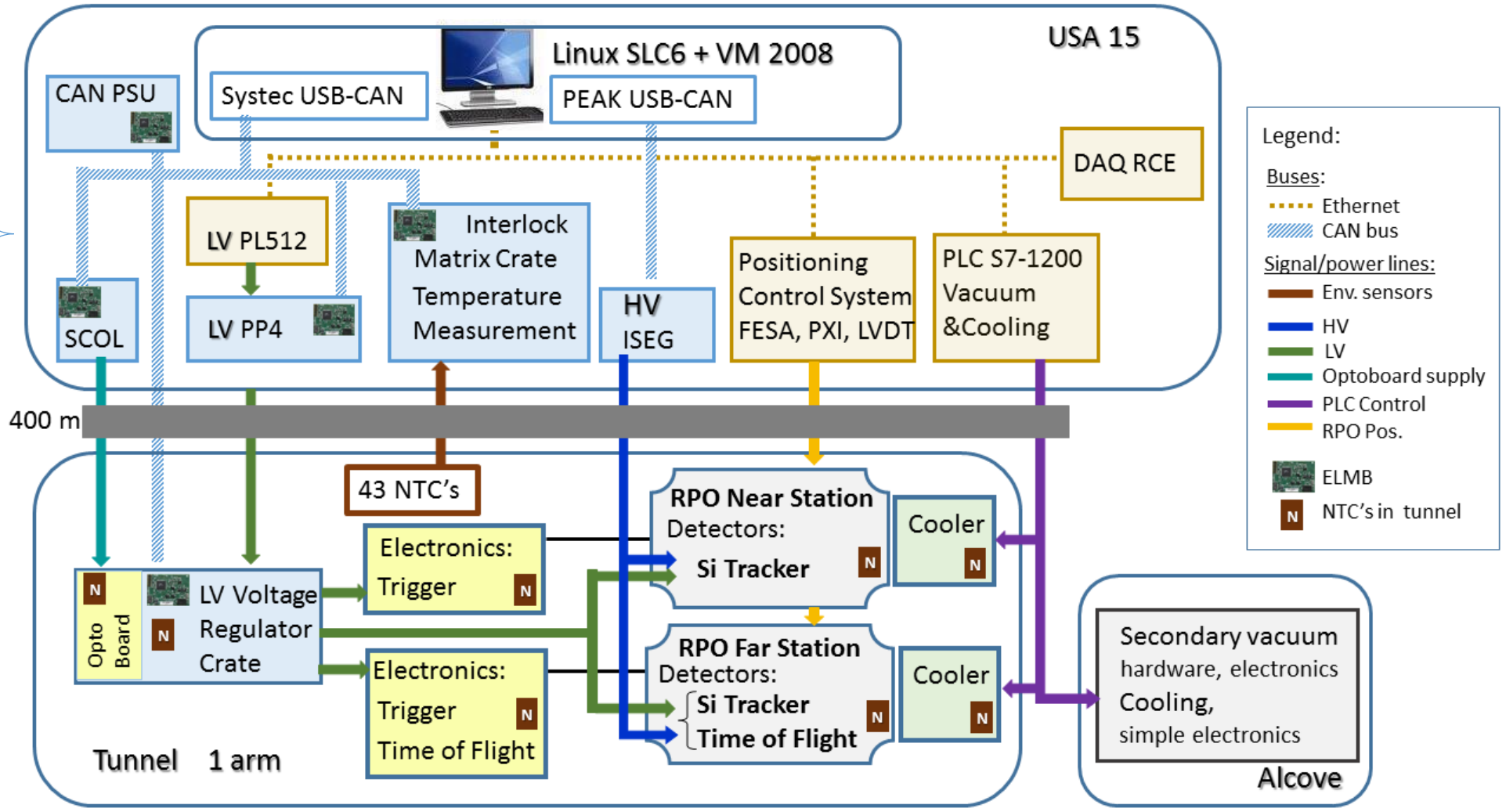
# DCS: overview of AFP Final Hardware Structure

## Hardware for both arms:

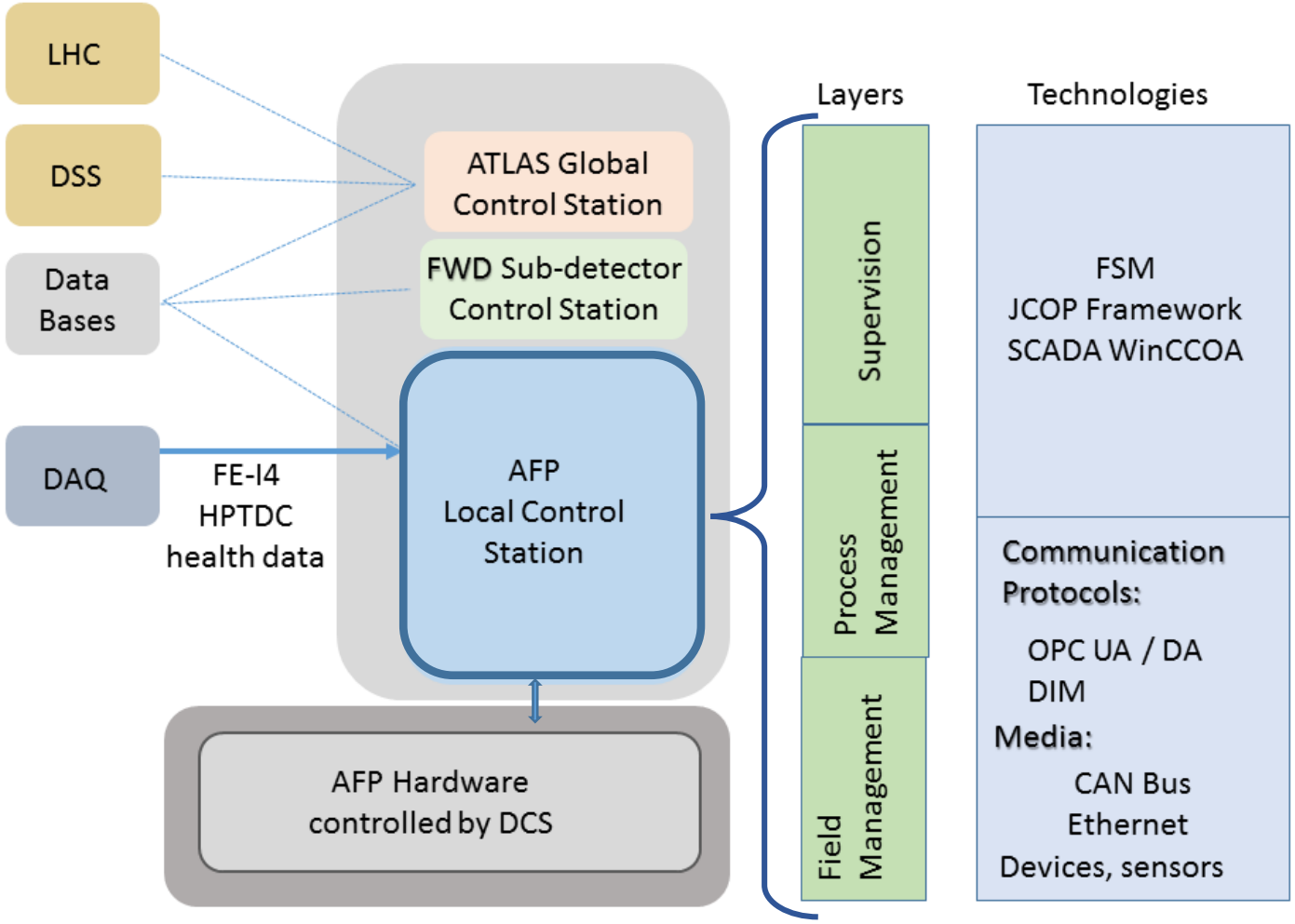
**HV** - ISEG crate with 2 modules
**LV** – 2 Wiener PL512 + 2 LVPP4
**SC-OL** – 1 block
**IMC** – 1 crate
*in total 15 ELMB's*
**Vacuum and Cooling** – PLC Controlled
**Positioning** – similar to TOTEM and ALFA
**DAQ**: final – ATCA RCE
AF0+2 – HSIO RCE

## Hardware for 1 arm

1 optobard
1 Vreg Crate – 1 ELMB
2 Cooler Stations



# DCS software structure and integration in Central DCS




## DCS Software

- WinCCOA 3.11 SCADA
- JCOP Framework Components
- Central ATLAS DCS Framework Components, rules and guidelines
- OPC servers as a middleware communication layer
- FSM for detector hierarchical representation, supervision and visualisation

AFP sub-detector is already defined in the ATLAS Central DCS structure

# Present activity: DCS in SR1 AFP LAB

Goal: design, develop and test DCS software

## DCS Machine Dell 1950:

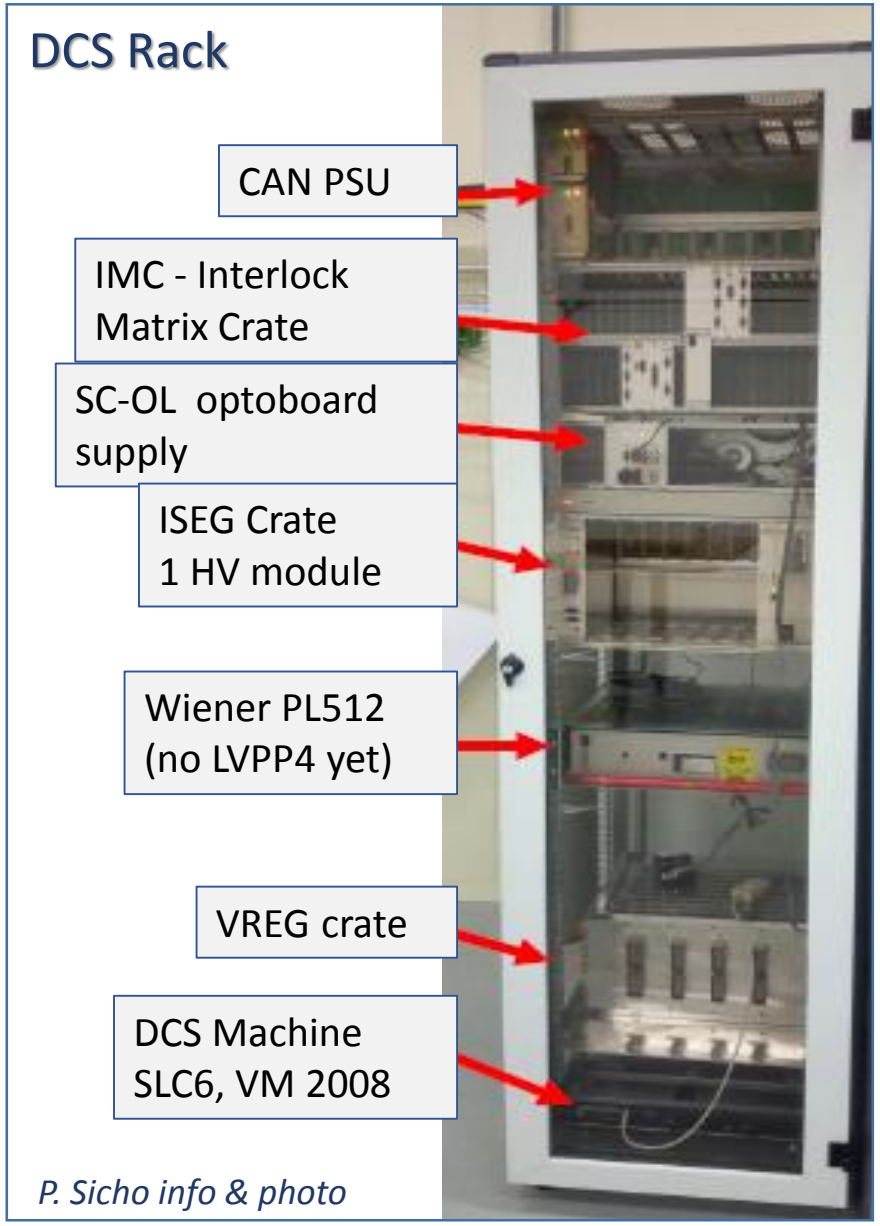
- SLC6 (WinCCOA + OPC UA servers + all DCS software) + VM2008 (WinCCOA + OPC DA servers)
- Will be kept in SR1 AFP LAB as Test Machine

## Hardware in SR1 (as a pool of spare components):

- CAN PSU – power supply for Can bus, crate + 2 modules
- Interlock Matrix Crate – will be completed soon with modules
- VREG Voltage Regulator Crate – cards to be provided
- ISEG HV crate + modules
- Wiener LV PL 512 – will be delivered soon

## RCE in SR1 Rack area:

- Used for development of FE Health Parameters embedded OPC UA server

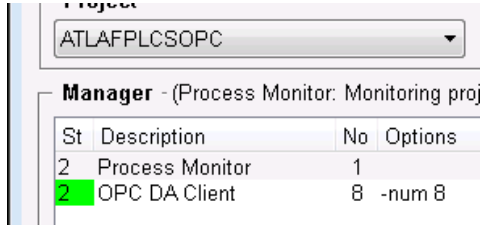


# Status of software development in SR1

## Software development ongoing:

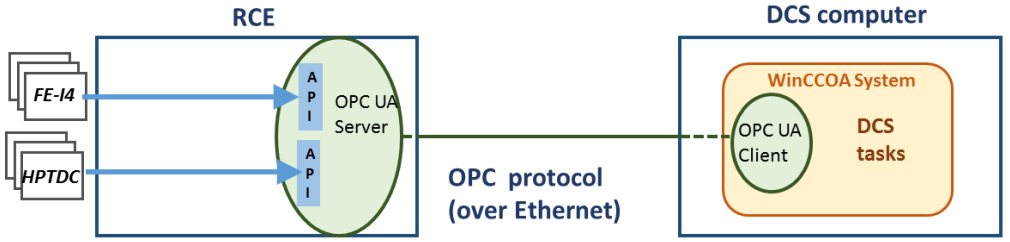
### High Voltage

ISEG OPC DA Server (VM2008) and ISEG Framework component installed and tested, ready for final hardware (from Cracow) and further development




### FE Chips health parameters

OPC UA server embedded in RCE will acquire health parameters via dedicated API's -> OPC UA server framework installed on RCE, ready for development

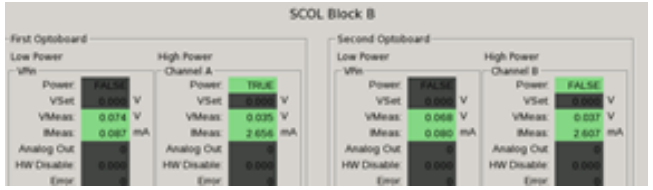



### Secondary Vacuum

Preliminary datapoint structure and panels defined


### ELMB-Controlled Equipment Ilock MC, SCOL, LVPP4, VREG

framework-like software development (based on IBL/Pixel) on-going



# DCS current status and plans

## Status of final hardware:

- HV ISEG crate and modules – tested OK in Cracow, ready to be sent to CERN
- Wiener PL512 power supplies - *still waiting for delivery*
- DCS production machine Dell R620 – ready in USA15
- ELMB controlled equipment: partially ready in SR1
- ELMB's – all needed (17) and some spares (3) available

## Status of software:

- AFP DCS added to Atlas Central DCS environment
- DCS Project in SR1 exists and allows for concurrent developments
- Status of individual software parts is progressing

## Plans:

- Continue software development in SR1: availability of detector parts will be necessary
- Install final production OS + necessary software packages in DCS P1 machine after TS3
- Start moving some parts of hardware and DCS software from SR1 to P1
- First tests in P1