Introduction

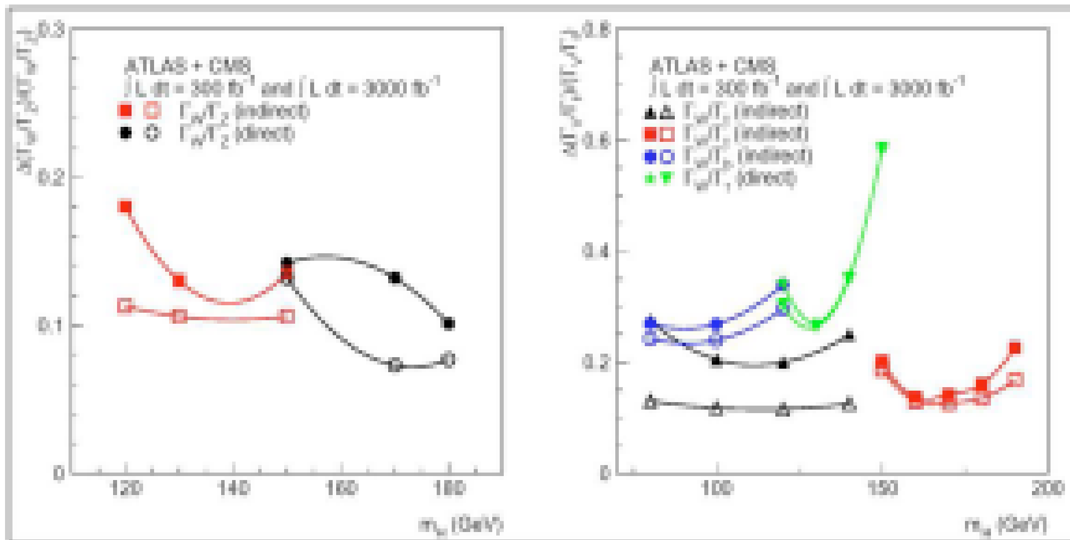
- LHC upgrade
- ATLAS upgrade
- Phase-I: Insertable B-Layer - IBL
- Phase-II: Calorimeters and Muons
- Phase-II: Inner detector

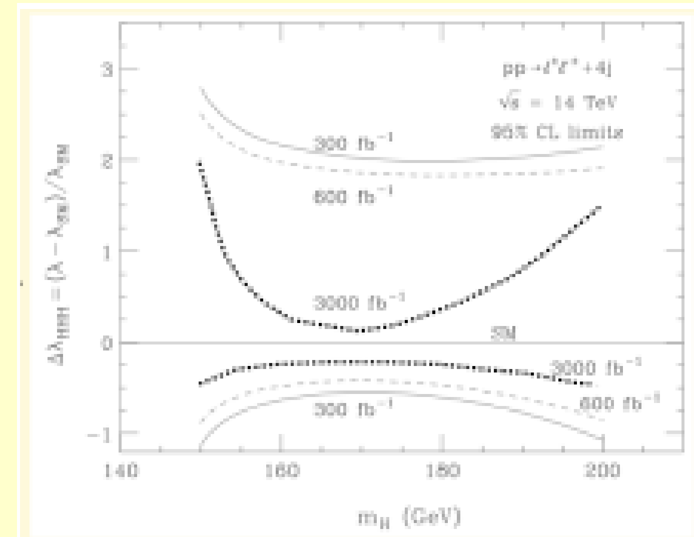
Physics at SLHC

- Extend reach in super partner mass
- Precision measurements of SUSY couplings and mass spectrum
- Extend the reach of quarks substructure
- Extend reach of Z' and W' gauge bosons
- Probing rare decay of top quark
- Extending reach for smaller extra dimensions

Physics at SLHC

- **Rare decays of Higgs boson**
- **Precision measurements of Higgs coupling and Higgs self coupling**
- **Complete physics program to be formulated after first LHC results**





	600 fb^{-1}	6000 fb^{-1}
$H \to Z\gamma$	3.5 σ	11 σ
$H \to \mu^+\mu^-$	< 3.5 σ	~ 7 σ

m[H] ~ [110-140] GeV

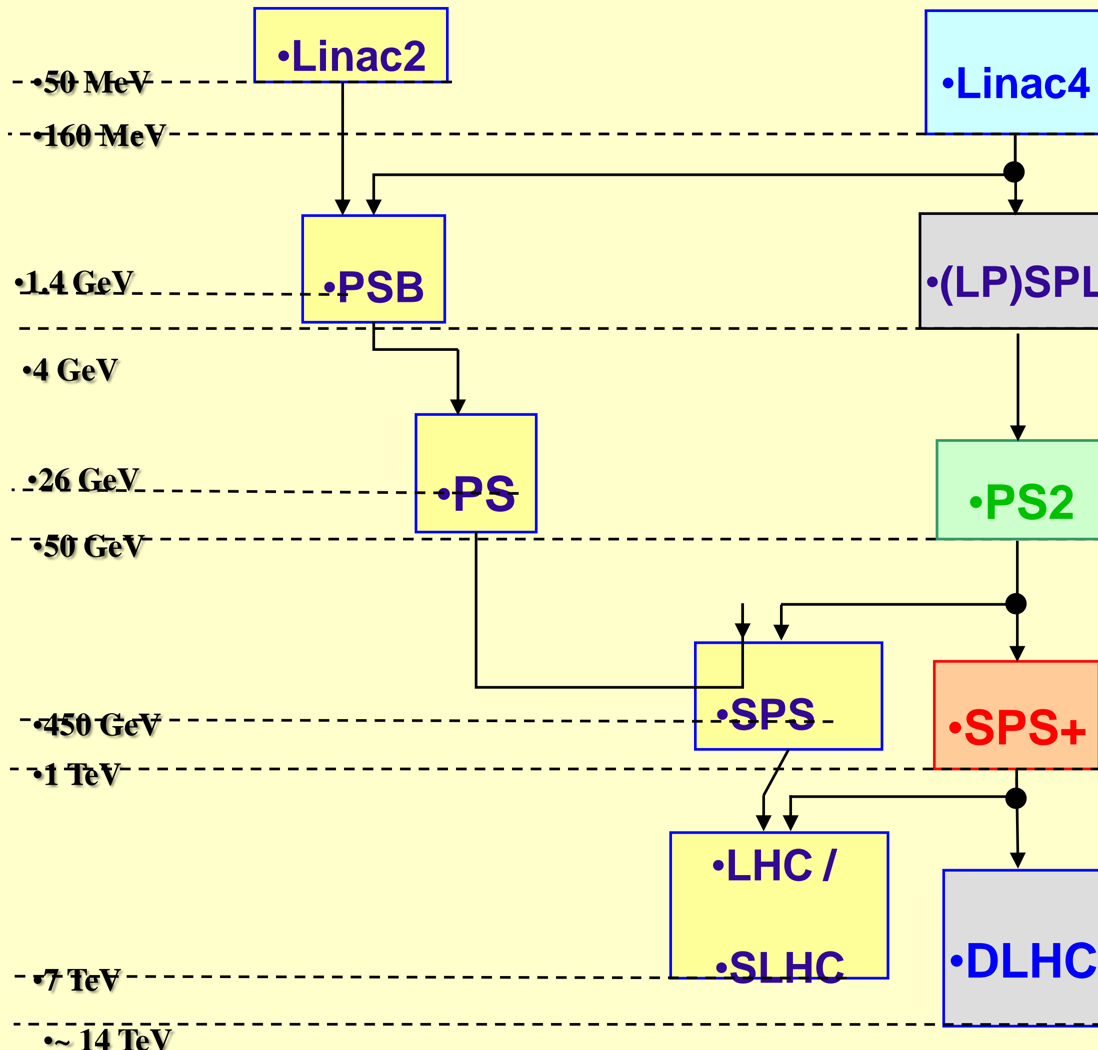
Han, McElrath, hep-ph/0201023

LHC upgrade stages

- **Phase 1 ~2013-2014, 3x10^{34} cm^{-2}s^{-1}:**
  new NbTi triplets, D1, TAS,
  β*~0.25-0.3 m in IP1 & 5,
  beam from new Linac4
- **Phase 2 ~2017, ~10^{35} cm^{-2}s^{-1} :**
  possibly Nb_3Sn triplet & β*~0.15 m
  injectors
  Old injectors (PS has 50 years !!!) needs investment anyhow.
  Complementary programs: hadron, neutrino, nuclear, ISOLDE
- **Complementary measures 2010-2017:**
  e.g. long-range beam-beam compensation,
  crab cavities, advanced collimators, crab waist?
  [, coherent e- cooling??, e- lenses??]

- **Longer term (2020?): energy upgrade, LHeC,…**

present and future injectors

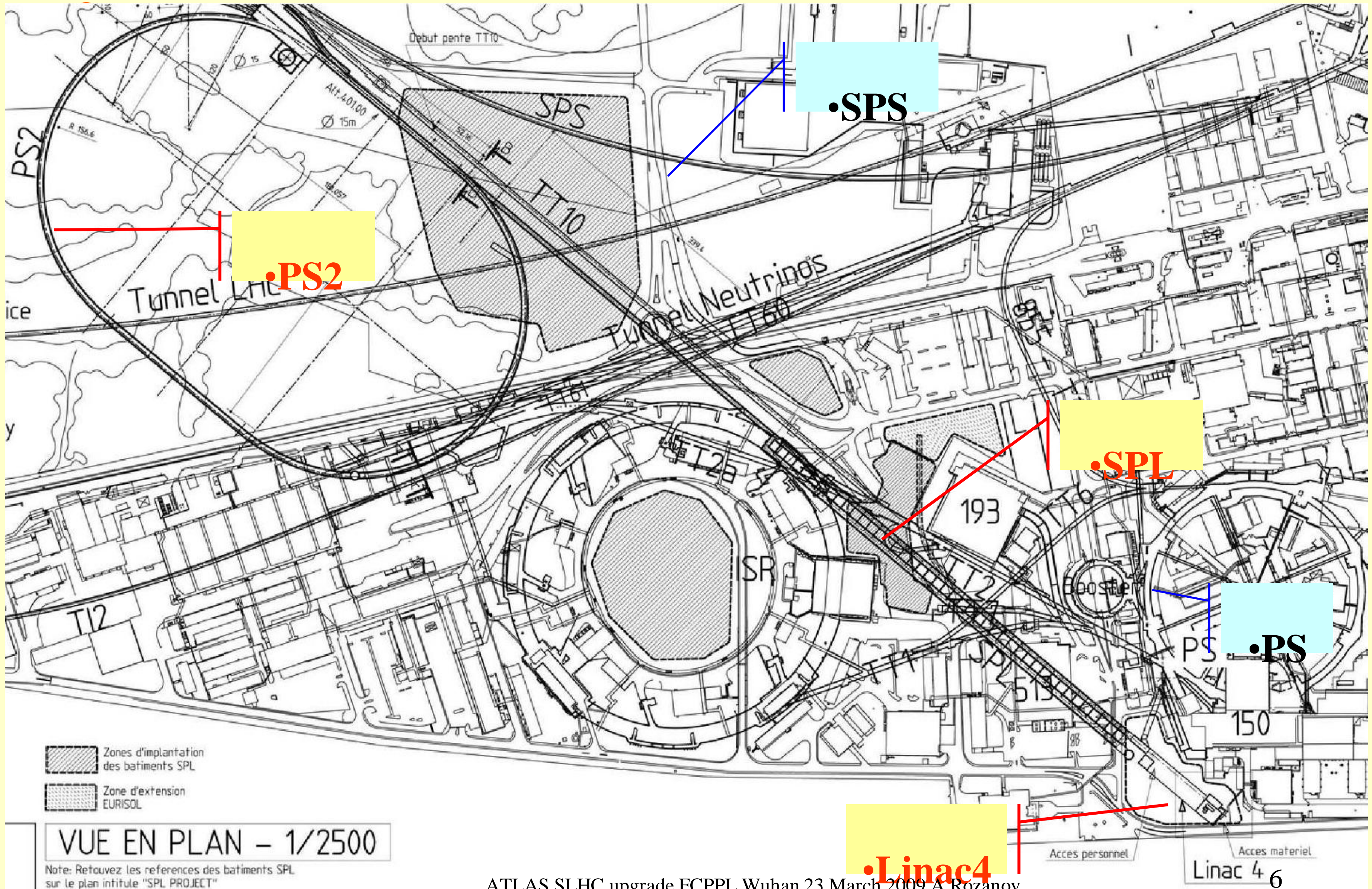


- (LP)SPL: (Low Power) Superconducting Proton Linac (4-5 GeV)
- PS2: High Energy PS (~ 5 to 50 GeV – 0.3 Hz)
- SPS+: Superconducting SPS (50 to1000 GeV)
- SLHC:“Superluminosity” LHC

(up to 1035 cm-2s-1)

- DLHC: “Double energy” LHC(1 to ~14 TeV)

Layout of the new injectors



ATLAS SLHC Upgrade

- **Phase-I : 6 months shutdown in 2014 (LHC accident, delay in Linac-4 CE)**

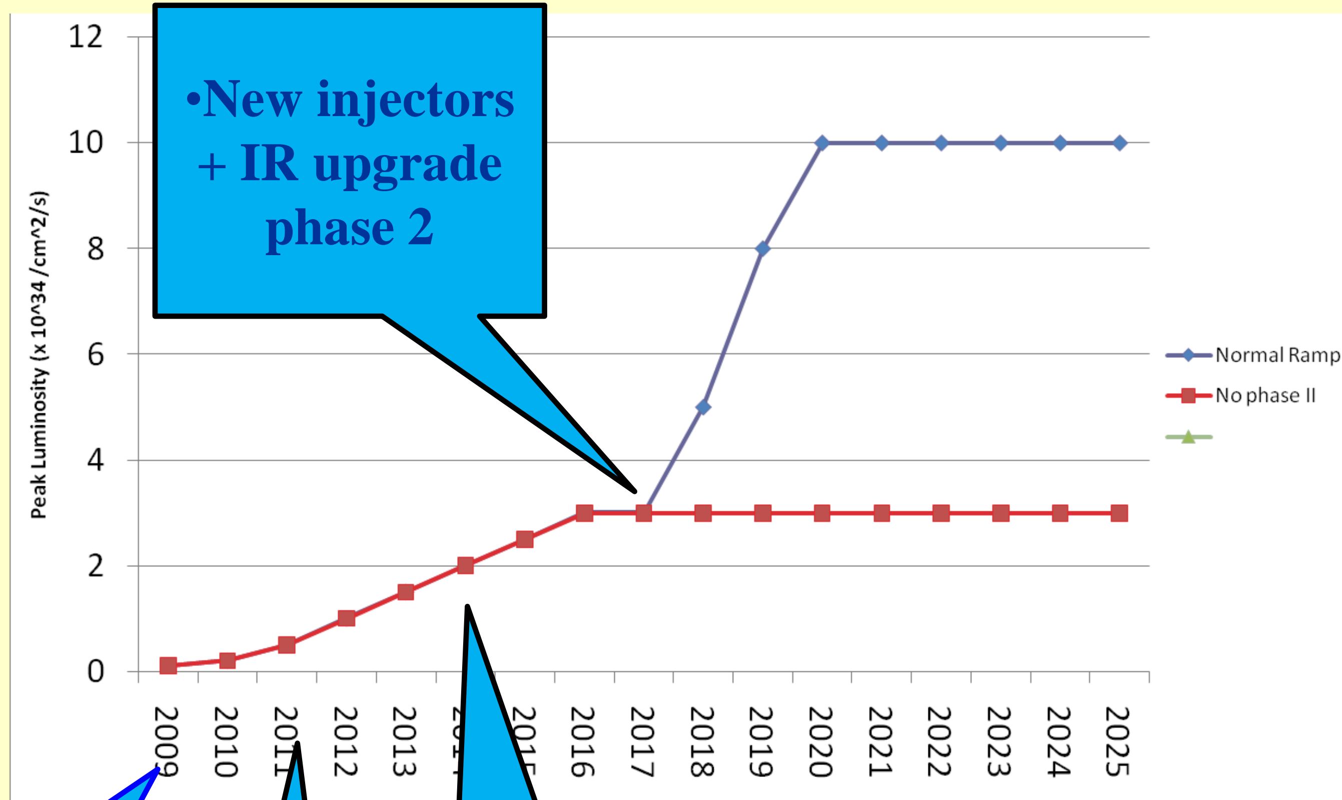
luminosity $3x10^{34}$ cm^{-2} s^{-1} ~75 events pile-up and 550 fb^{-1} delivered

- **Phase-II: 18 months shutdown in 2017-2018 luminosity 10^{35} cm^{-2} s^{-1} , 300 – 400**

events pile-up - very challenging for detectors

- **Luminosity leveling ? ~75 events pile-up …**

Peak luminosity

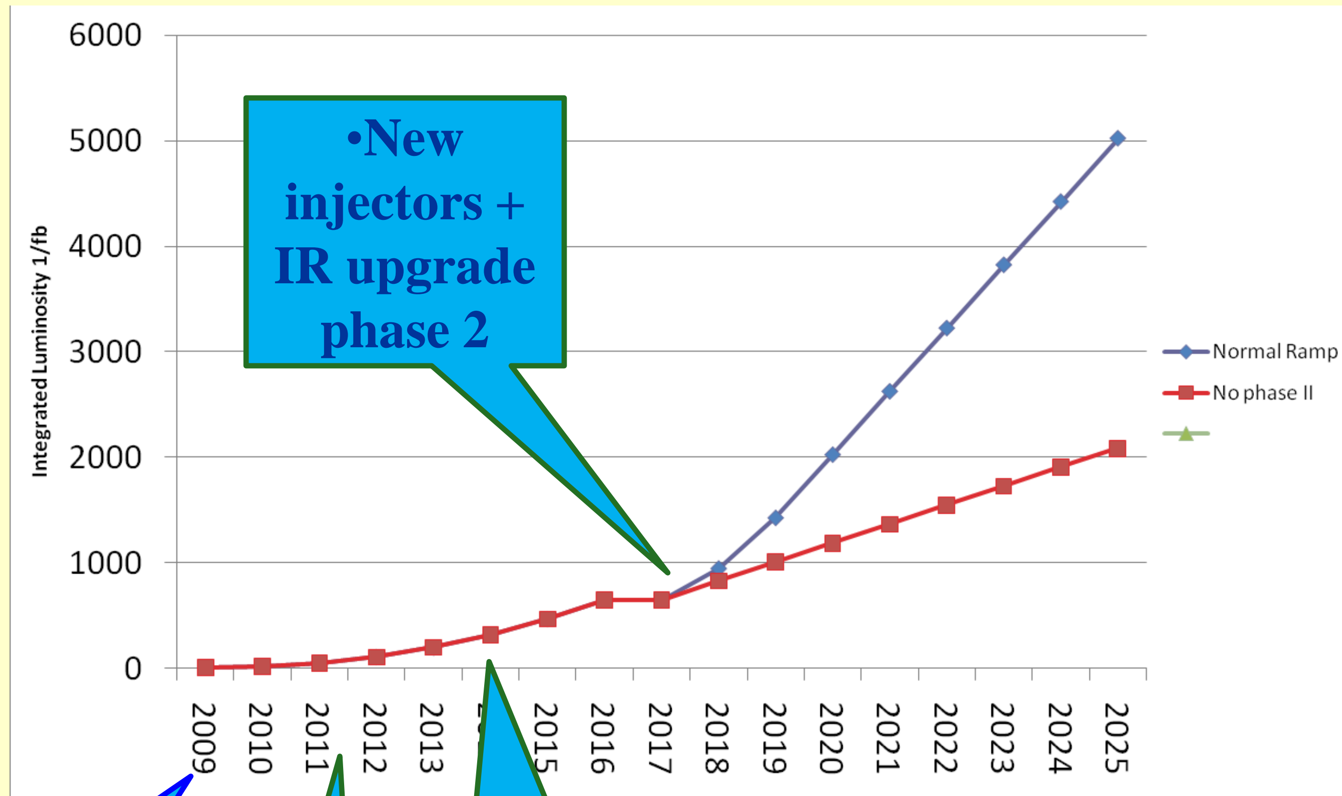


•Early operation

•Collimation phase 2

•Linac4 + IR upgrade phase 1

Integrated luminosity



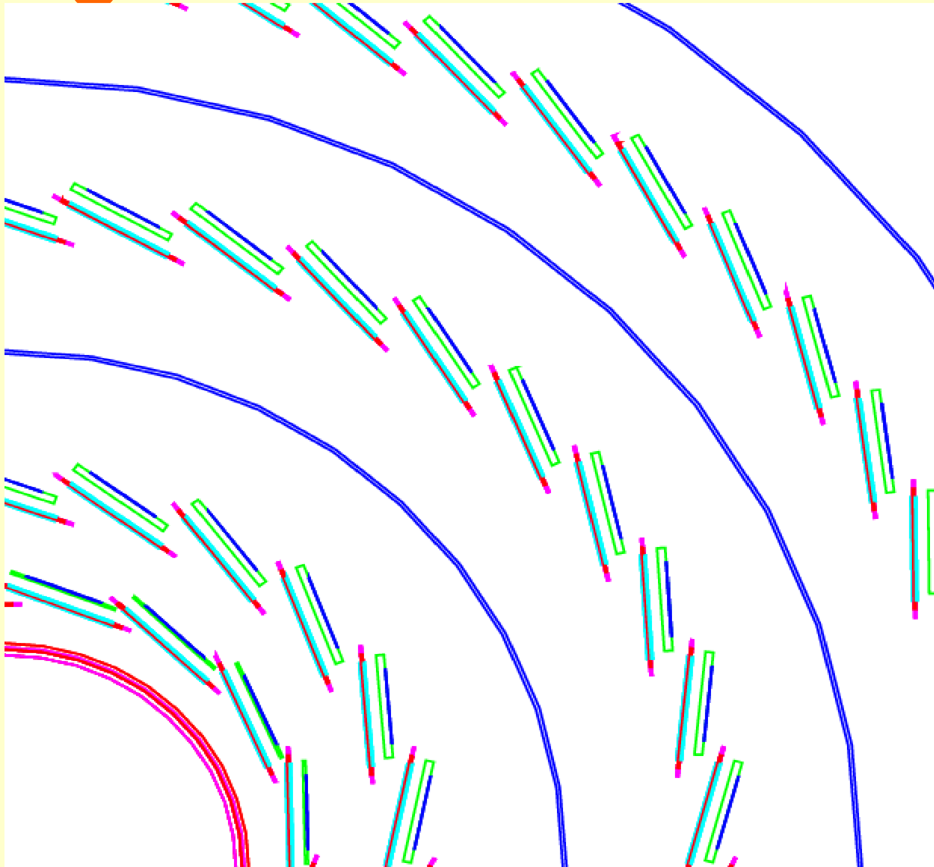
Phase-I ATLAS SLHC Upgrade

- **Insertable B-Layer (IBL) project – change Be beam-pipe with new light pixel b-layer at R=3.5 cm**

Four scenarios of b-layer upgrade

- 1) **Extract only old beam pipe and put new light beam pipe with new light b-layer at R=3.7 cm**
- **2) Exchange full pixel package with new minimal pixel package including new beam pipe, new b-layer at R=3.7 cm, one barrel layer at R=8.9 cm, one disk**
- **3) Replace beam-pipe and old b-layer by new beam-pipe and new b-layer at R=3.7 cm**
- **4) Exchange full pixel package with new minimal pixel package including new beam pipe, old type of b-layer at R=5.05 cm, one barrel layer at R=8.9 cm, one disk**

Insert new b-layer

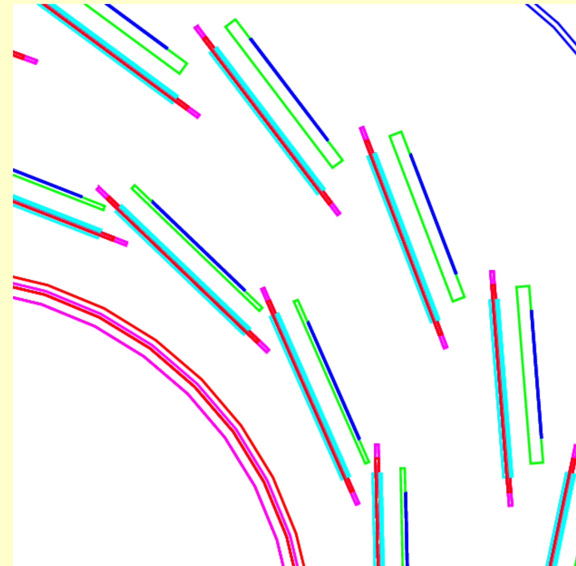


- R_{b1} = 37.0mm

R_{b2} = 50.5mm

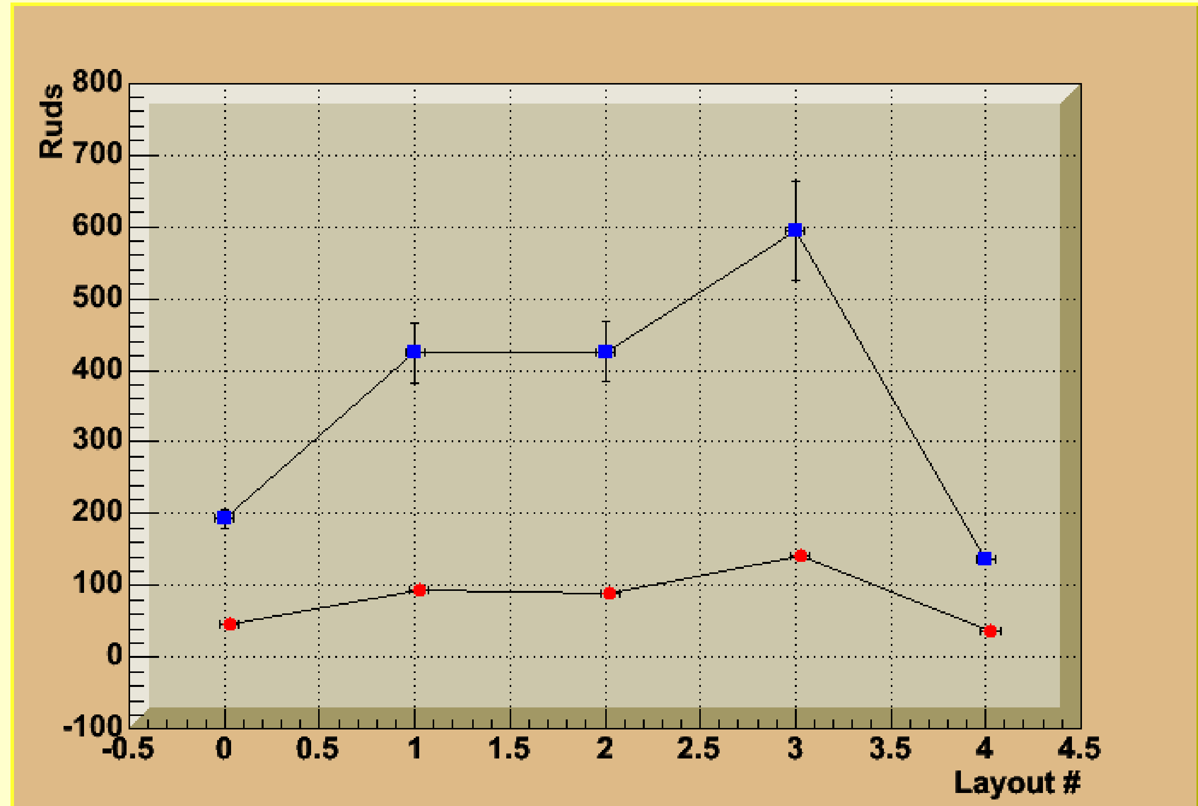
R_1 = 88.5mm

R_2 = 122.5mm



Four replacement scenarios

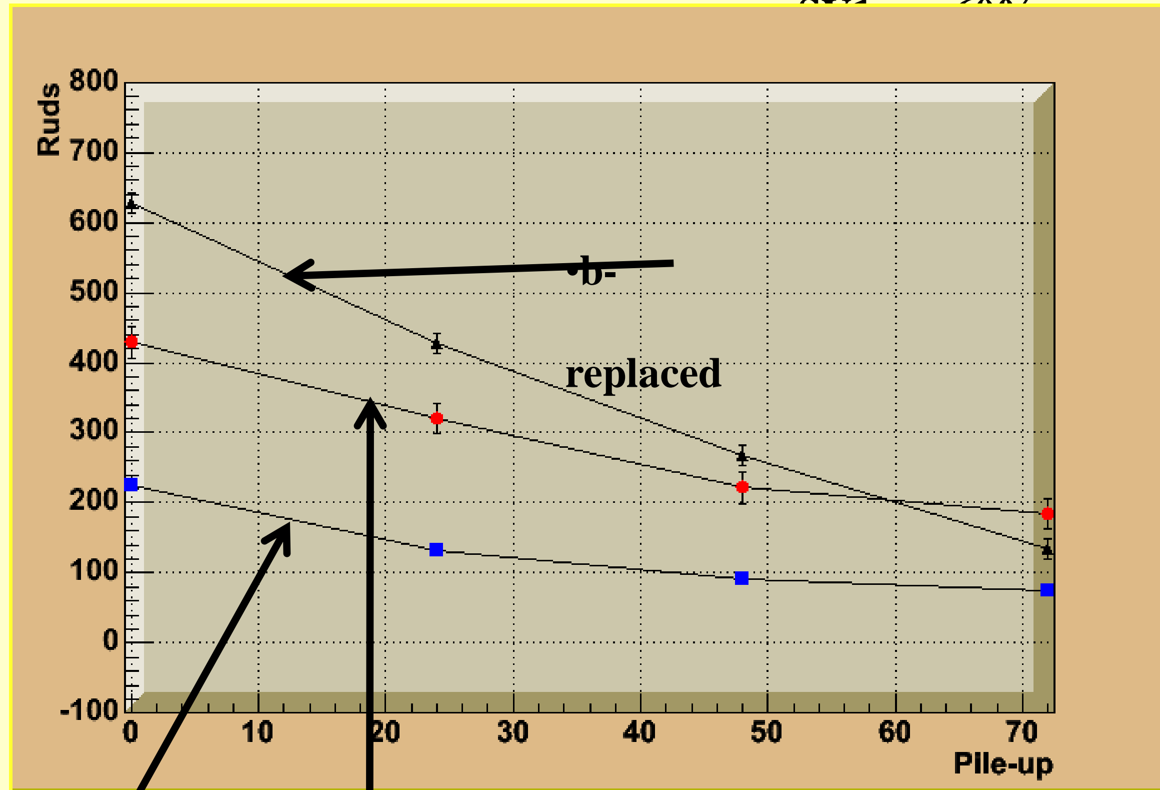
- WH(120 GeV)->bb
- low luminosity
  - SV1 ε_b=60%
  - SV1 ε_b=70%



- ATLAS
- b-inserted as 4-layer R=3.5 cm
- 2-layers R=3.5 cm and 8 cm
- b-replaced
- 2-old layers

Performance versus pile-up

- **WH(120 GeV)**



- **ATLAS**

- **b-**
inserted
as 4-layer
R=3.5 cm

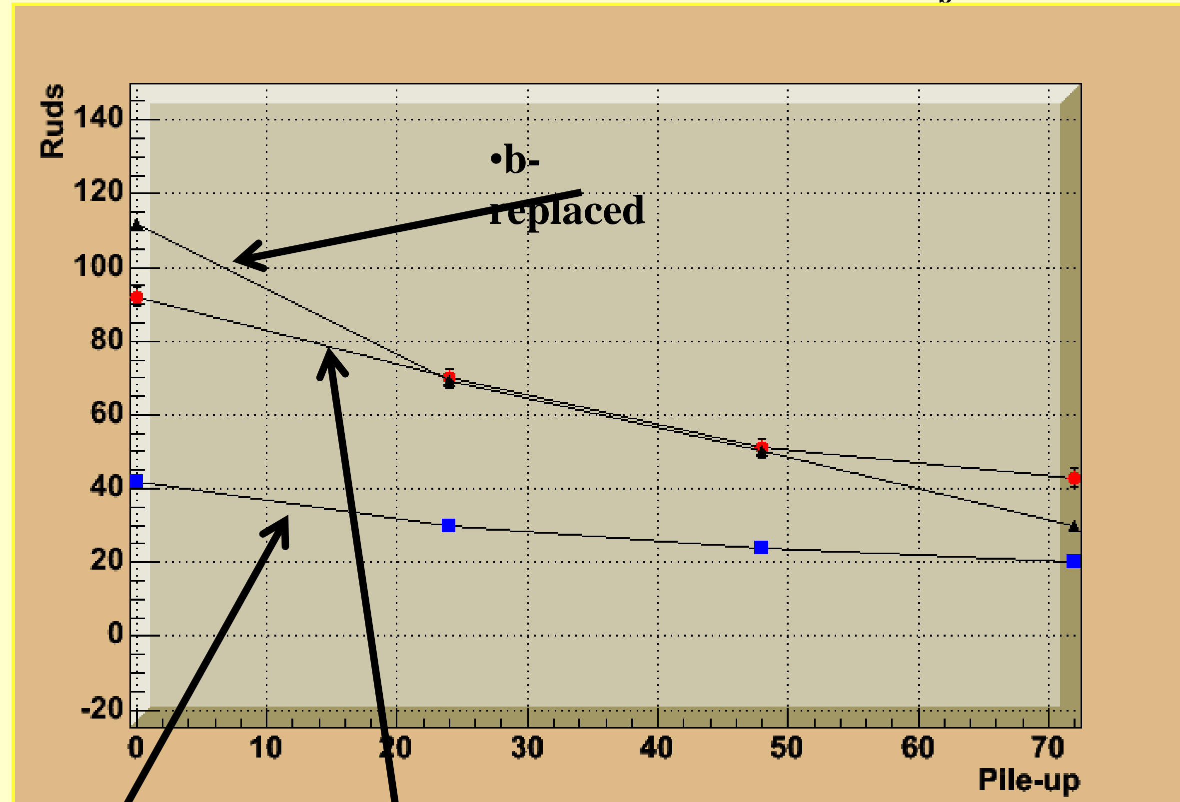
Performance versus pile-up

•SV1 ε_b=70%

•WH(120 GeV)

•Conclusions:

- IBL with 4 pixel layers is more robust to pile-up

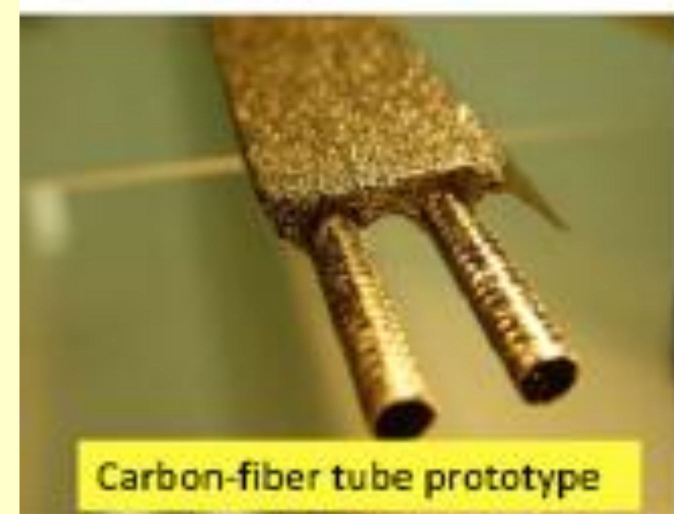


•ATLAS

•b-
inserted
as 4-layer
R=3.5 cm

Phase-I IBL Mechanics

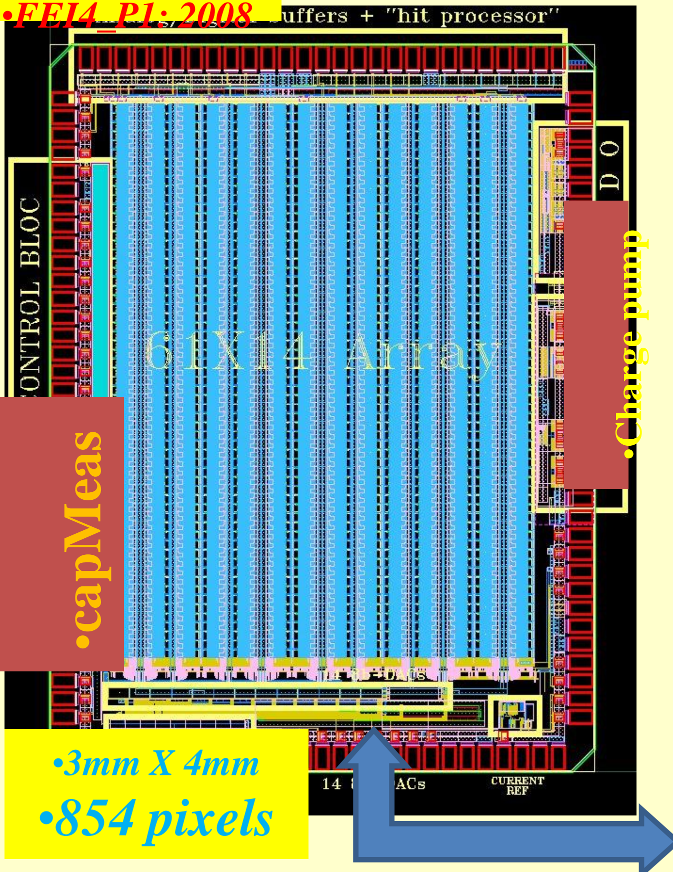
- **Pixel cooling options: CO_2 cooling vs C3F8 cooling. Test of prototypes with C3F8 or C3F8/C2F6 mixtures started at CPPM by Greg Hallewell**
- **Stave pipe options: carbon pipe, Ti pipe(100 um wall) , hybrid Ti/carbon. Eric Vigeolas producing Ti pipes and laser welding to Ti connectors at CPPM**
- **Ti tube connectors: Annecy/Marseille common design**
- **Prototypes of carbon foam staves with Ti pipes: Milano-Wuppertal-Marseille.**



- **Characterization, pressure and thermal stave tests at CPPM.**
- **CPPM/Annecy thermal calculations of staves**
- **Module loading methods and robot at CPPM**
- **LPNHE(Paris) material thermal tests, CAD X0 calculations**

ATLAS SLHC Upgrade

•FEI4_P1: 2008



•capMeas

•Charge pump

•3mm X 4mm
•854 pixels

•FEI4: 09/2009

80 cols X 336 rows
(~ 19mm X 20mm)
IBM kerf review and approval may be needed)

<— columns —>

<— rows —>

END OF CHIP (~ 2mm X 20mm) including pad frame

•19mm X 20mm
•26880 pixels

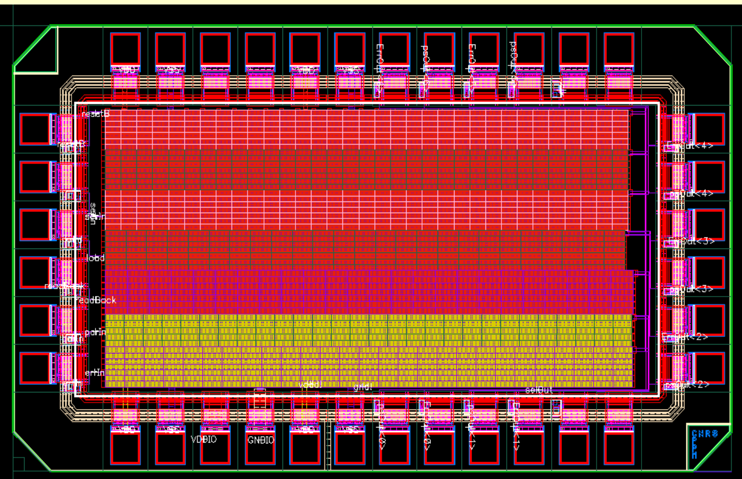
•(50μ X 250μ)

•FEI3:
•2880 pixels

•(50μ X 400μ)

Phase-I IBL Electronics

- from FE-I3 to FE-I4-P1 to FE-I4
- FE-I4 130nm IBM CMOS technology
- FE-I4 collaboration: Berkley-Bonn-Marseille-Genova-Amsterdam
- design of SEU hard registers at CPPM
- SEU-2 chip in July 2008, participation of Wang Zheng (IHEP) in tests
- SEU-3 chip in March 2009
- Test of SEU-2 40 Mhz and SEU-3 in may-october 2009 at CERN PS
- CPPM develop low consumption discriminators in FE-I4-P2 in march 2009
- test of FE-I4-P2 in summer 2009
- FE-I4 review in March 2009, submission in

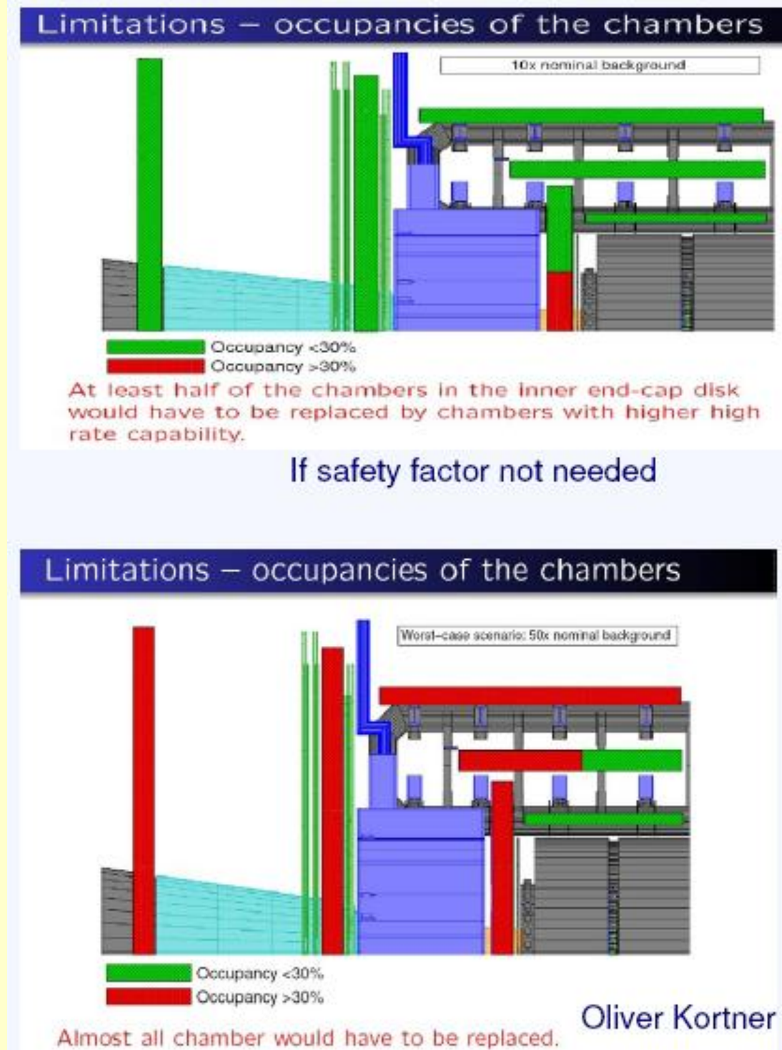


•Conclusions:

- IBL Project endorsed by ATLAS
- IBL TDR in 2010
- Preliminary cost estimate 8 Mchf

Phase-II ATLAS Muon Upgrade

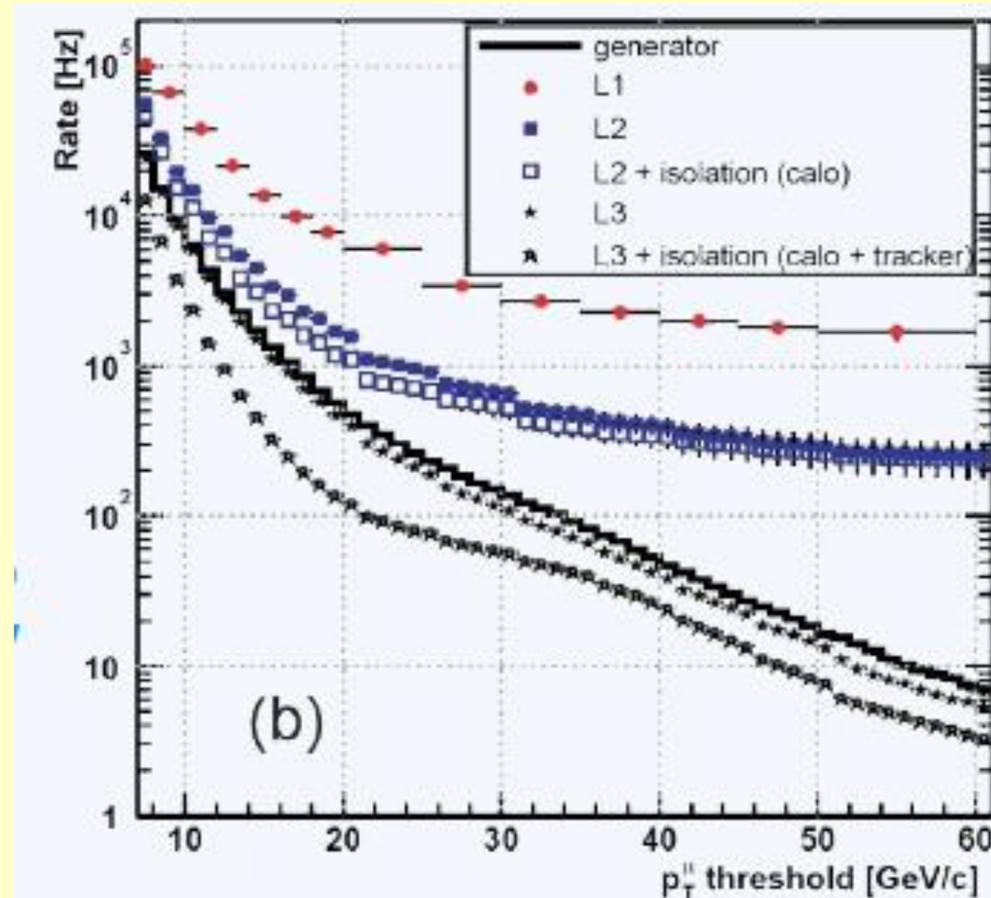
- Complete exchange of Inner Detector, partial upgrade of Muons and Calorimeters



- Big uncertainties (~ factor 5) in muon occupancy, real LHC measurements needed
- RD work on micromegas (contact Bruno Mansoulie (CEA)), small diameter MDT etc

Phase-II ATLAS Trigger Upgrade

- **Problem with constant muon LVL1 trigger rate above pT~ 20 GeV/c**



• Increase muon trigger thresholds: reduce physics reach, e.g SUSY decay channels

•Solutions; higher resolution trigger chambers ? Additional muon chambers ?

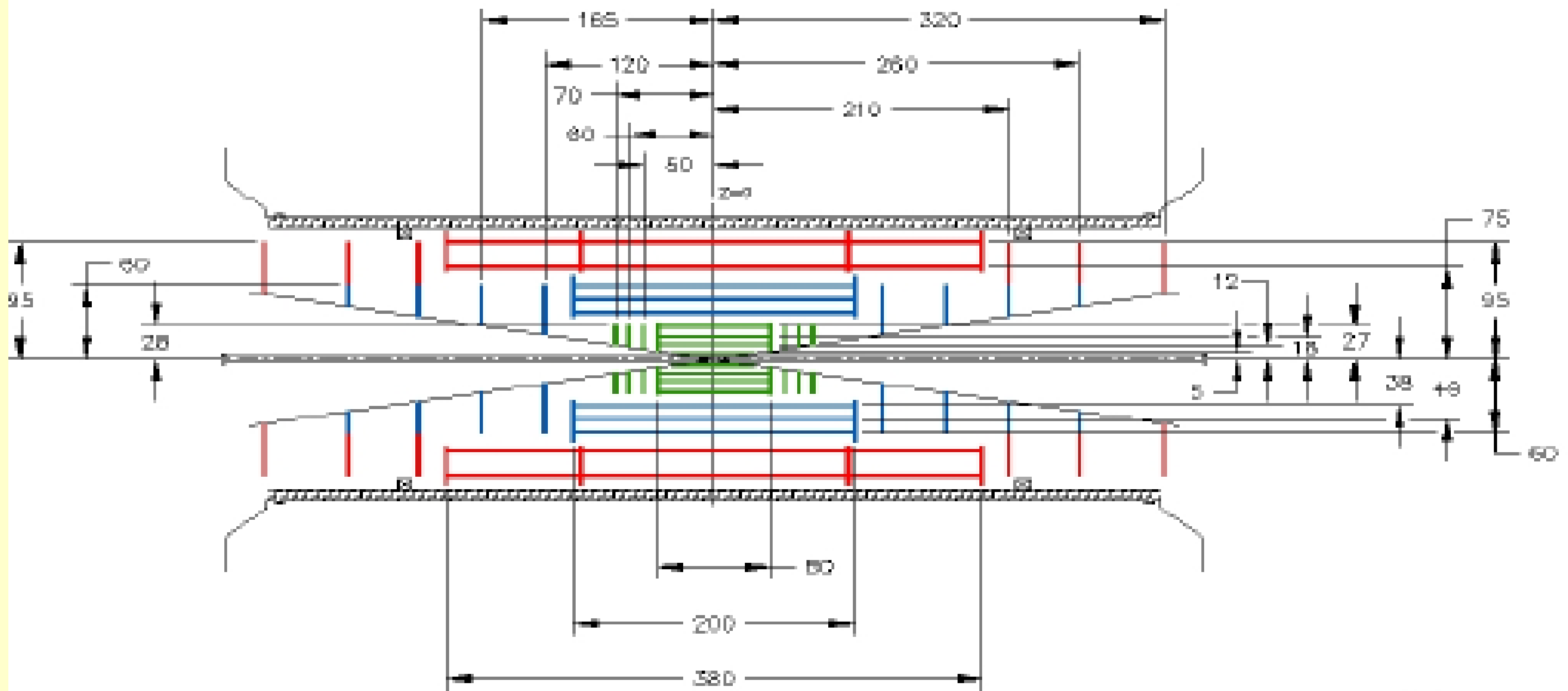
• Tracker trigger in Inner detector as studied in CMS ?

Phase-II ATLAS Calorimeter Upgrade

- **Tile and LAr should perform well at SLHC. Readout and trigger electronics will need upgrade (Orsay, Annecy, Grenoble, Clermont)**
- **Problems with FCAL: HP drops, Ion build up in gaps, heating and boiling**
- **Solutions: additional mini-FCAL in front, or new FCAL**
- **Studies at Protvino test beam**

Phase-II ATLAS ID Upgrade

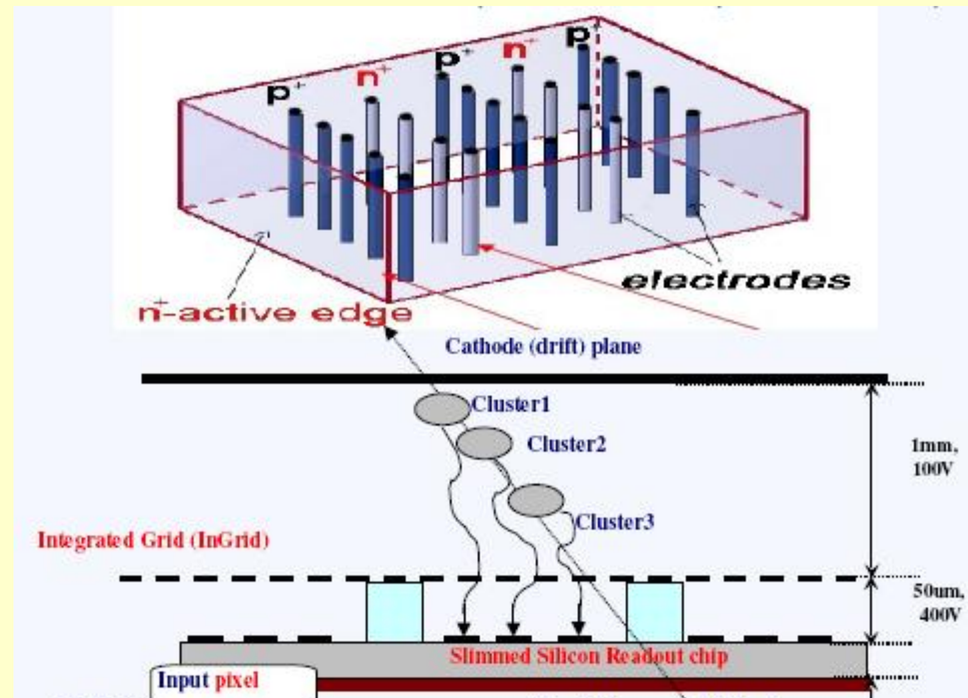
- New All silicon Tracker: 4-5 layers of pixels, short strips, long strips



Phase-II ATLAS ID Upgrade

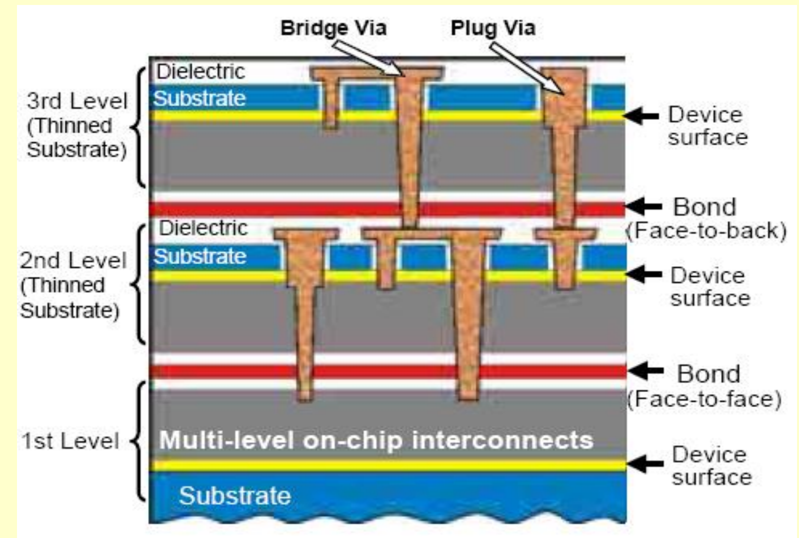
- But some challenging RD are gong on: 3D silicon sensors, diamond detectors, low mass micromegas at vertex, track trigger micromegas at high radius

- b-layer sensor candidates: 3D Si sensors, diamond, micromegas, thin Si sensors (Orsay,LPNHE)
- Track triggers with micromegas/gem high radius gas tracker
- 3D pixel electronics
- Tracker trigger with Si 3D interconnection stacking - tracklets

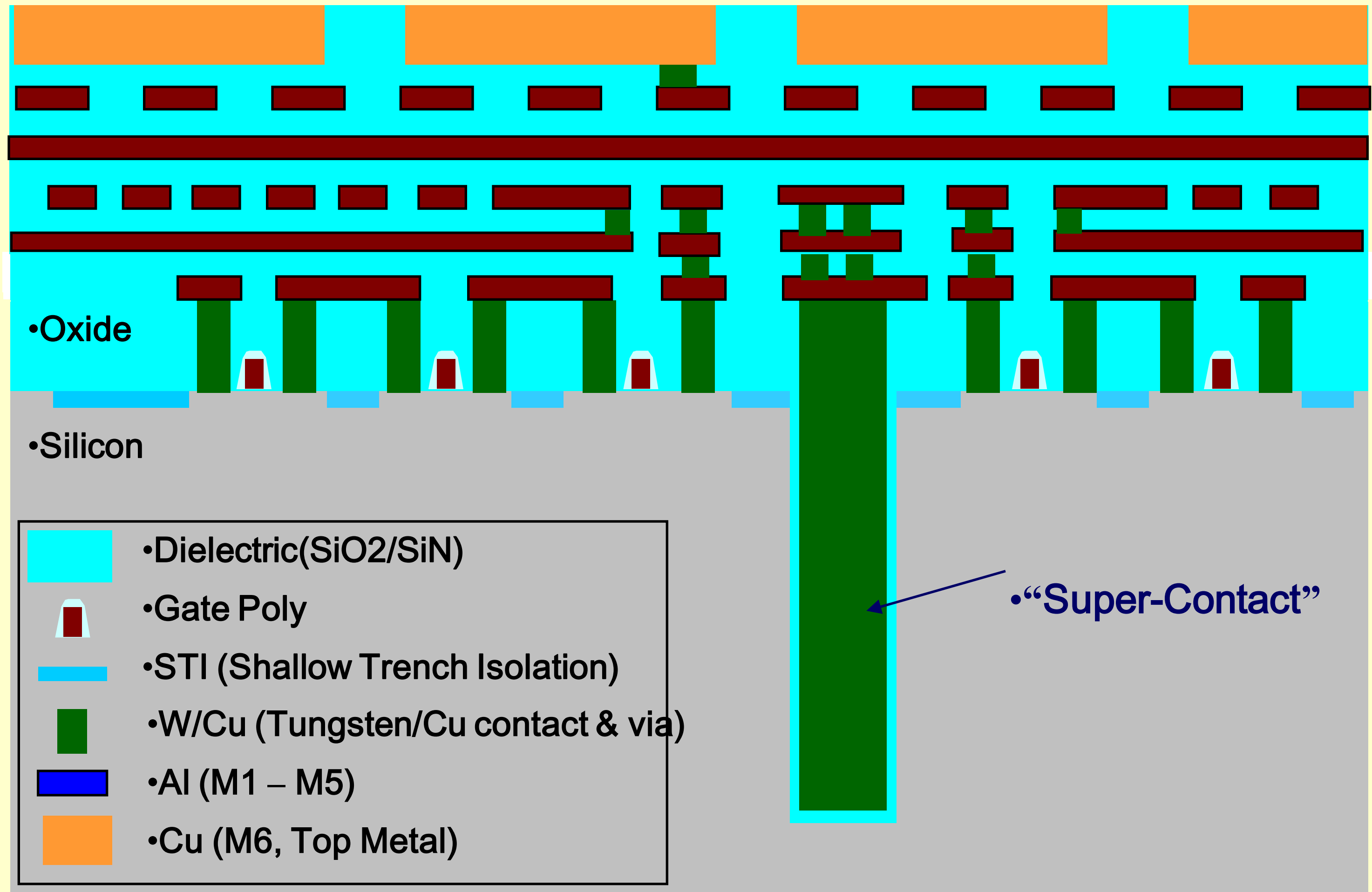


Why 3D ?

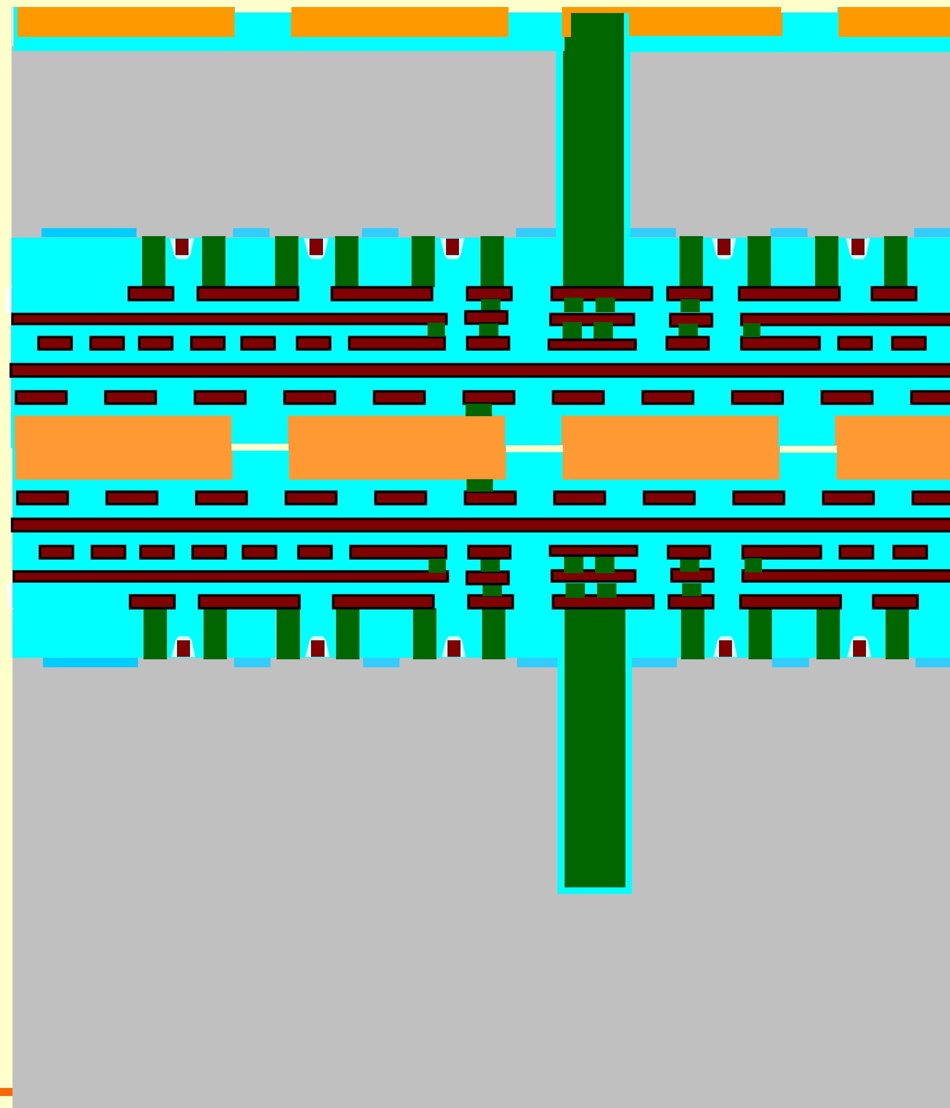
- Dense (several vertically integrated tiers on the same surface)
- Faster (shorter lines)
- Lower power (shorter lines)
- Lower cost (reuse of previous design in one tier)
- Mixture of different `technologies
- Device accessible from both sides



A Closer Look at Wafer-Level Stacking



Next, Stack a Second Wafer Thin:

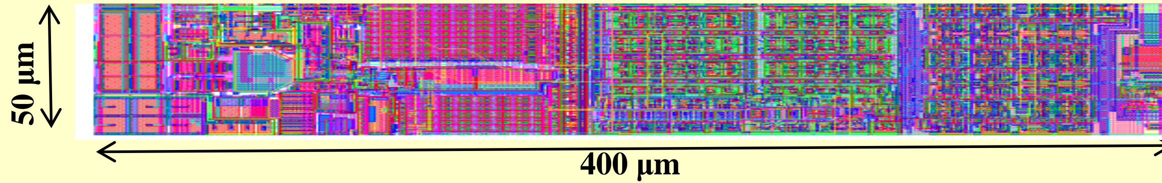


Organization of 3D electronics RD for SLHC

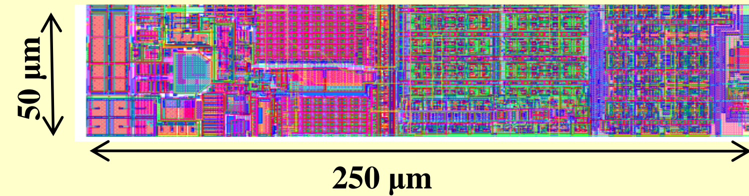
- **Workshop on 3D detectors LHC-ILC, Paris, 29-30 November 2007 by CNRS-IN2P3.**
- **CPPM-IPHC-IRFU-LAL-Paris 3D collaboration formed, IN2P3 finance of 200K Euros for (coordinator J.C.Clemens)**
- **CPPM-LAL-Paris ANR "Vitesse" 3D RD (coordinator L.Abdenour)**
- **3D will be part of Pixel FE electronics RD proposal**
- **Vertical Integration Technologies for HEP, workshop, Ringberg castle, 6-9 April 2008, Max Plank institute (H.G.Moser)**
- **Planar Si detectors for 3D electronics under production in Munich**
- **3D collaboration organized by Fermilab (coordinator R.Yarema) through Tezzaron (FNAL-Italy-France)**
- **Rare example where LHC and ILC communities are working on RD projects together both on the French and international levels**

ATLAS SLHC Upgrade

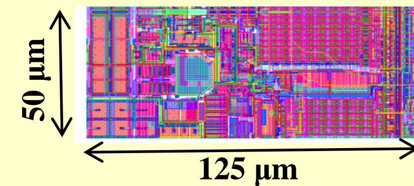
ATLAS Pixel Front End size



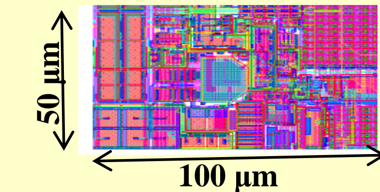
FE-I3 CMOS 250 nm



FE-I4 CMOS 130 nm



FE-I4-3D-2 CMOS 130 nm 2 layers

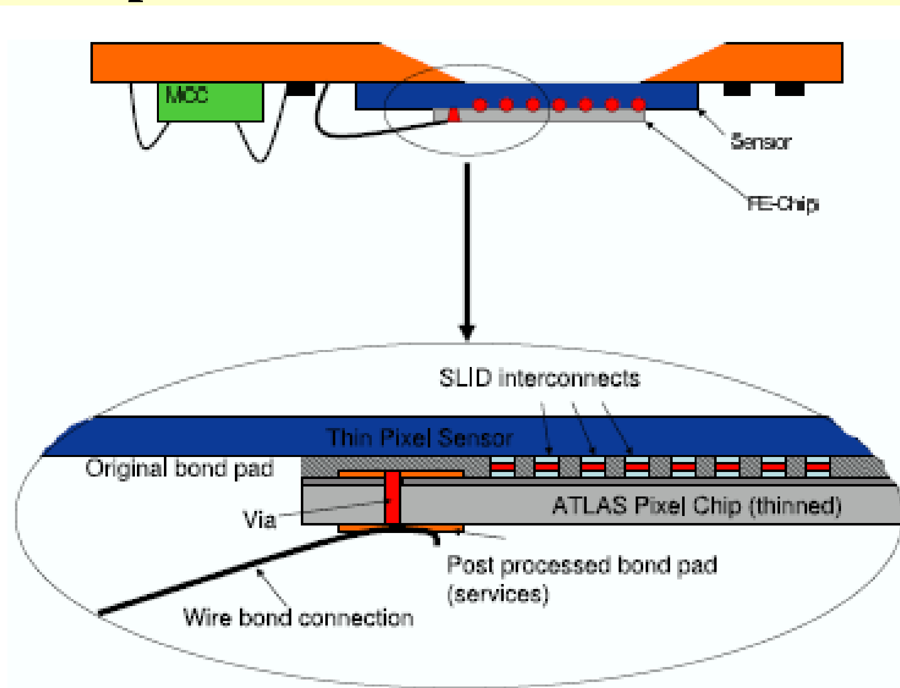


FE-I4-3D-3 CMOS 130 nm 3 layers

ATLAS R&D on 3D and thin Si

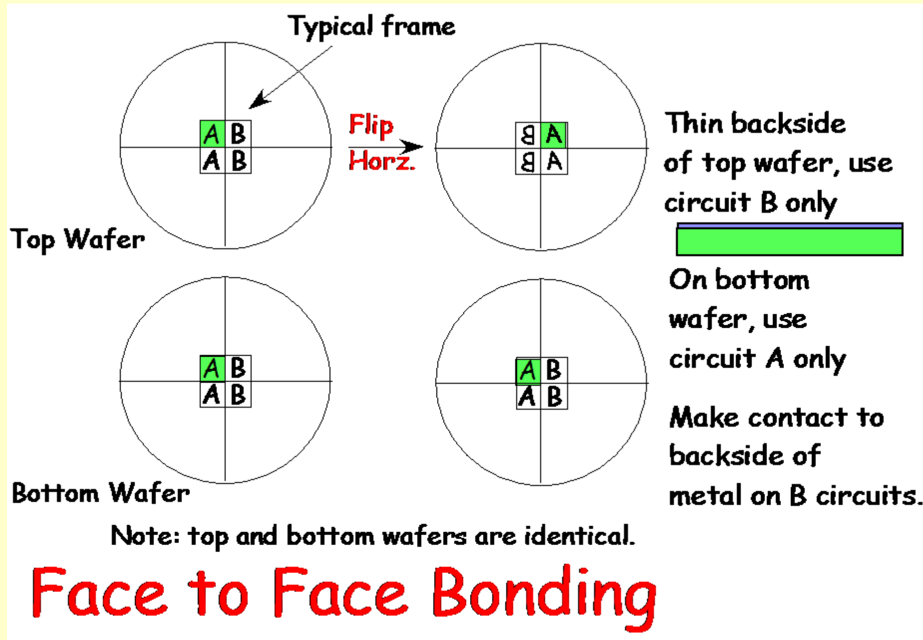
- Bonn-Dortmund-Oslo-Interon- MPI_Munich RD proposal
- Prototype module expected in 2009
- Thinned ATLAS FE-I3 chip bonded with SLID to thin 75 µm Si sensor
- Via last through FE-I3 for wire-bond pad

- LAL(Orsay) and LPNHE(Paris) participate in planar sensor RD
- LAL(Orsay) design low threshold FE chip suitable for thin sensors
- first proto with 50umx50um pixels size in May 2009 Tezzaron-Chartered 3D multiproject run run



Fermilab 3D Multi-Project Run

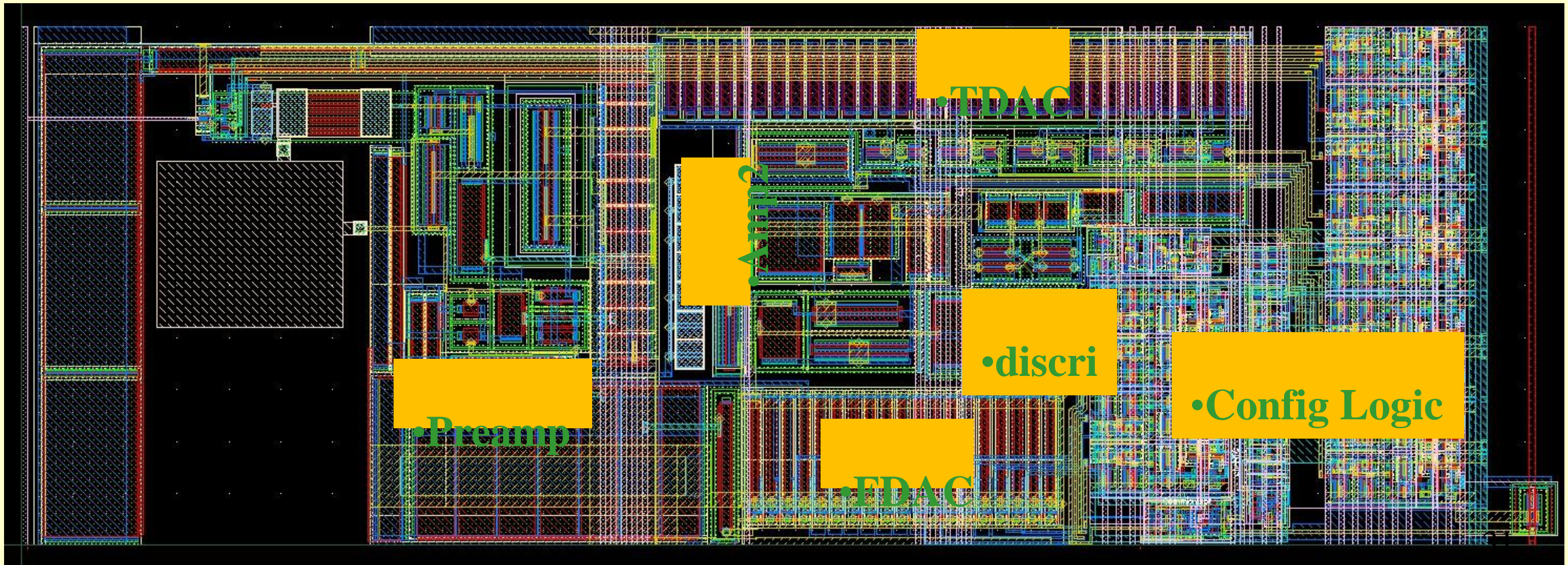
- Fermilab organize a dedicated 3D multi project run using Tezzaron for HEP beginning 2009.
- 25 wafers from Chartered will be bonded by Tezzaron into 12 double wafers
- The wafers will be bonded face to face.

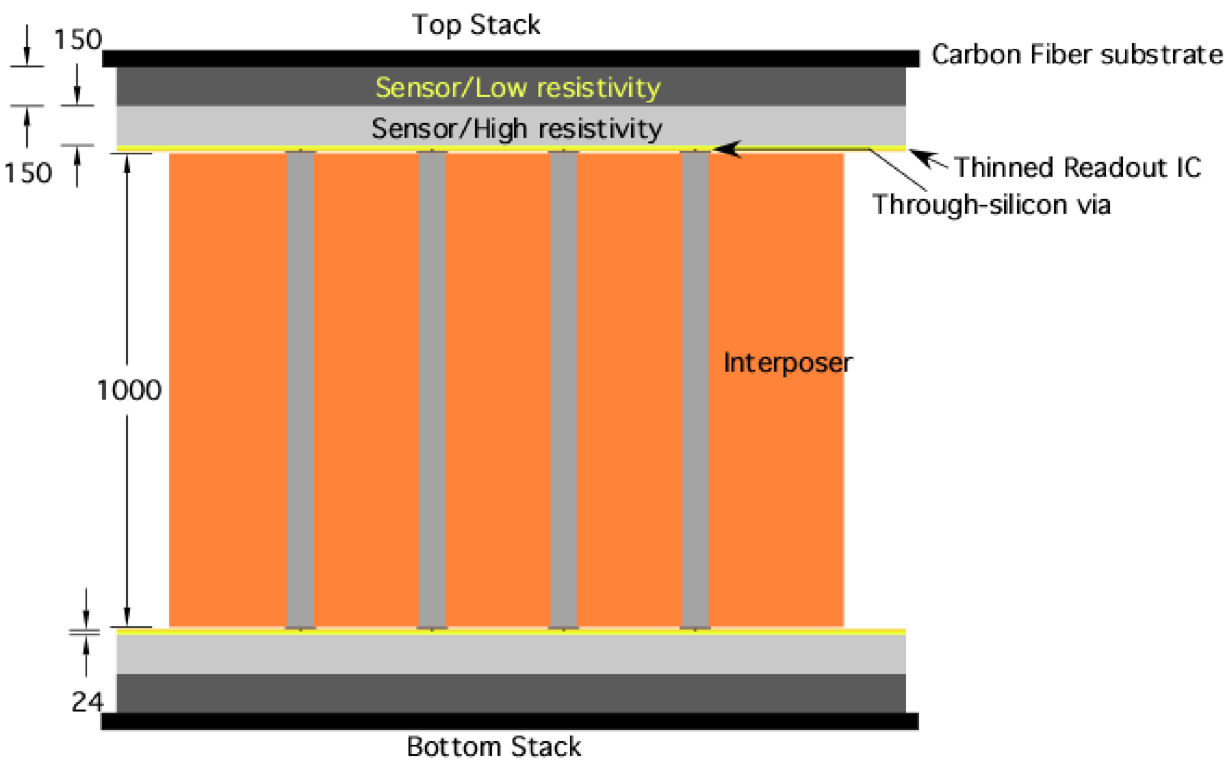


•FNAL, Italy (Bergamo, Pavia, Perugia, Bologna, Pisa, Rome), France (Marseille, Strasbourg, Orsay, Saclay, Grenoble, Paris)

ATLAS in Tezzaron-Chartered

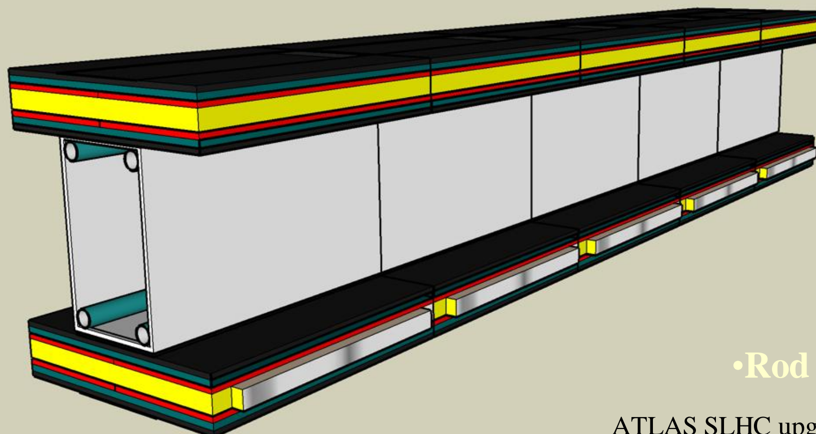
- Porting FE-I4-Proto *(61x14 pixel array 50*250 µm , overall chip 3x4 mm)* into Chartered FE-C4-Proto(test technology, irradiation tests) Collaboration of CPPM-LBNL-Bonn. Chip submitted in February2009
- Put FE-C4-Proto into Tezzaron run with vias to bump-bond and wire bonds
- Split the pixel electronic into analog & digital tiers parts in FE-TC4-3D-Proto
- Direct comparison of 2D-3D test results
- Low threshold design with separated analog and digital tiers and minimal pixel size (LAL)





Track trigger

- Strong point at CMS, some RD at ATLAS
- ATLAS FE-C4-Proto (CPPM-LBNL-Bonn) will be used in first FNAL-CMS pixel trigger prototype in Tezzaron-Chartered 3D run
- LAL will participate in the variant of FE-TC4-Proto with holes collection



- Rod

Conclusions 3D

- **3D electronics offers the reduction of the pixel size needed at SLHC**
- **3D electronics can offer analog tier with most optimal technology (.13 um) and digital tier with high density technology (90 nm/65 nm)**
- **extra tier may offer comfortable buffer sizes, data compression**
- **possibility to include trigger functions in the chip and create double layers - tracklets**
- **first step in May 2009 with FE-TC4-Proto and LAL-testchip in Tezzaron/Chartered 3D run**
- **More unexpected benefits of 3D electronics for SLHC are quite probable**

ATLAS SLHC Organisation

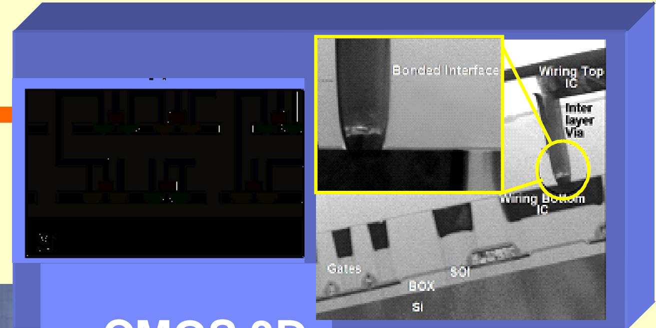
- **Steering Committee, Project Office, RD Review Commitee**
- **Letter of Intent in 2010**
- **Technical Proposal 2011-2012 synchro with sLHC phase-II approval**
- **TDRs by subsystem in 2012-2013**
- **Preliminary cost estimates**
- **34 Mchf pixels**
- **105 Mchf Si strips**
- **10 Mchf ID integration**
- **60 Mchf shielding, muons, calorimeters, trigger, DAQ**

Spares

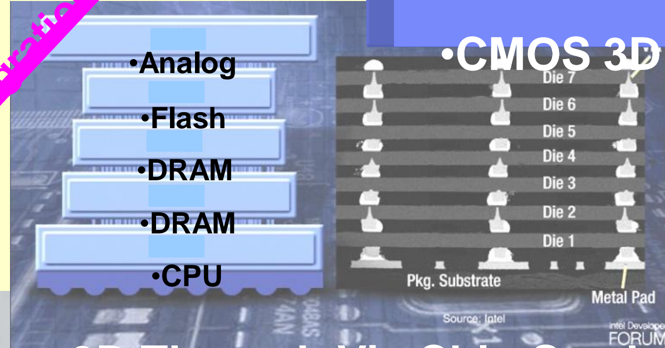
Introduction

- **Why pixel 3D electronics ?**
- **Initiatives in ATLAS**
- **Tezzaron-Chartered prototypes**
- **How can 3D electronics technology help us to challenge the physics at LHC ?**

•Evolution of 3D



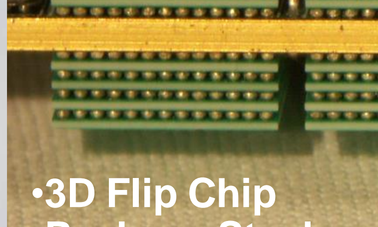
•CMOS 3D



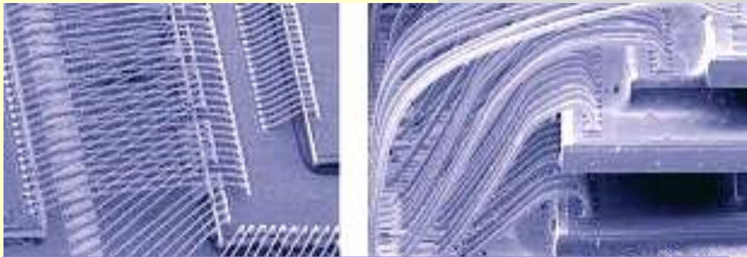
•3D Through Via Chip Stack

•Increasing 3D Integration

•3D•Pkg•Chip
•Stack



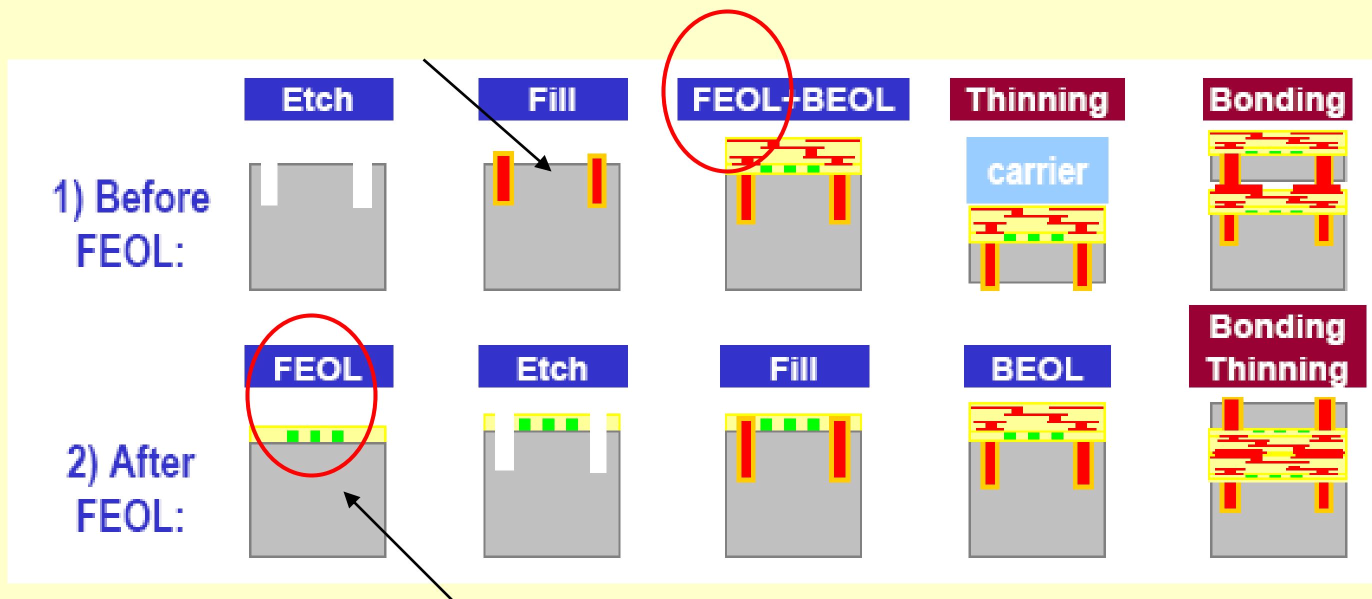
•3D Flip Chip
•Package Stack



Via First Approach

- Through silicon Via formation is done either before or after CMOS devices (FrontEnd of Line) processing

•Form vias before transistors



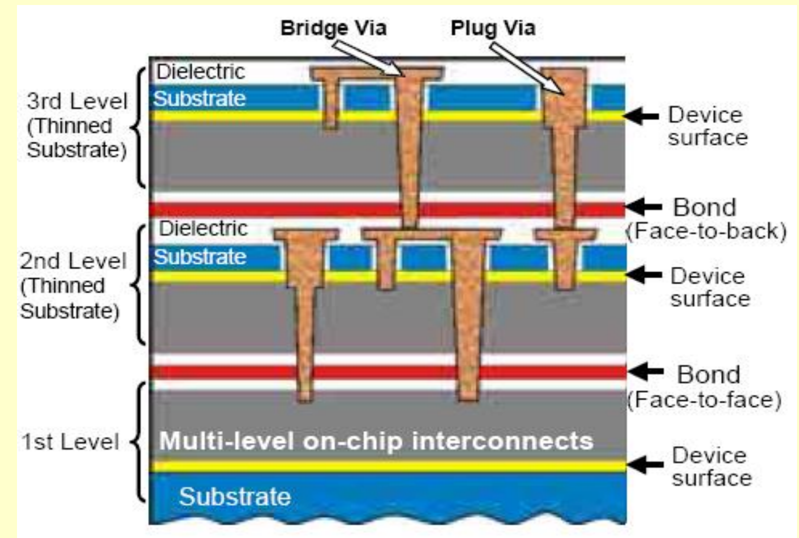
•IBM, NEC, Elpida, OKI, Tohoku, DALSA….

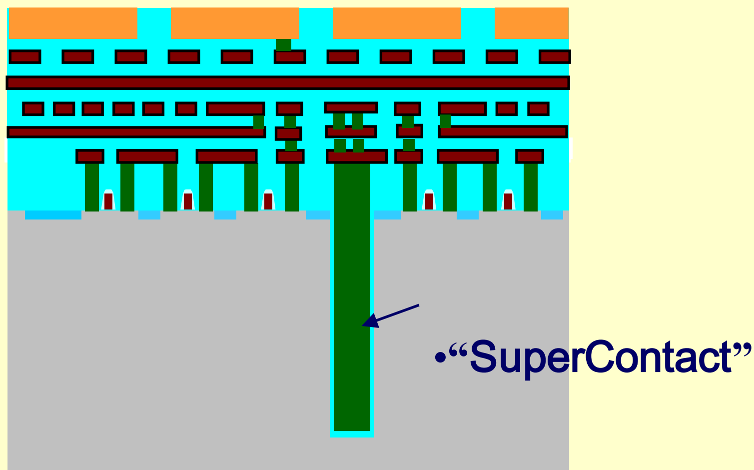
•Tezzaron, ZiptronixChartered, TSMC,RPI, IMEC……..

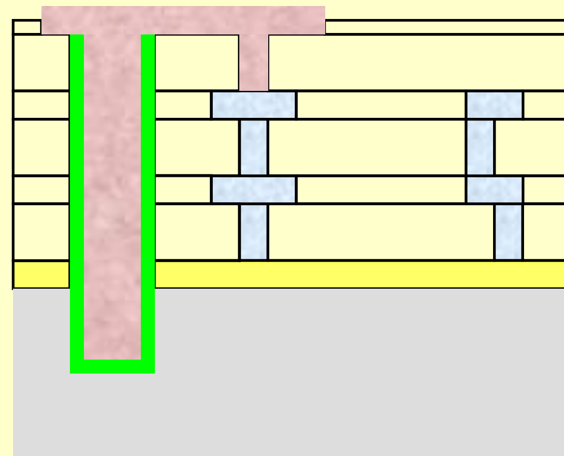
•Form transistors before vias

Through-Silicon Via (TSV)

- Via First
- Via Last
- Via at Front end (FEOL)
- Via at Back end (BEOL)





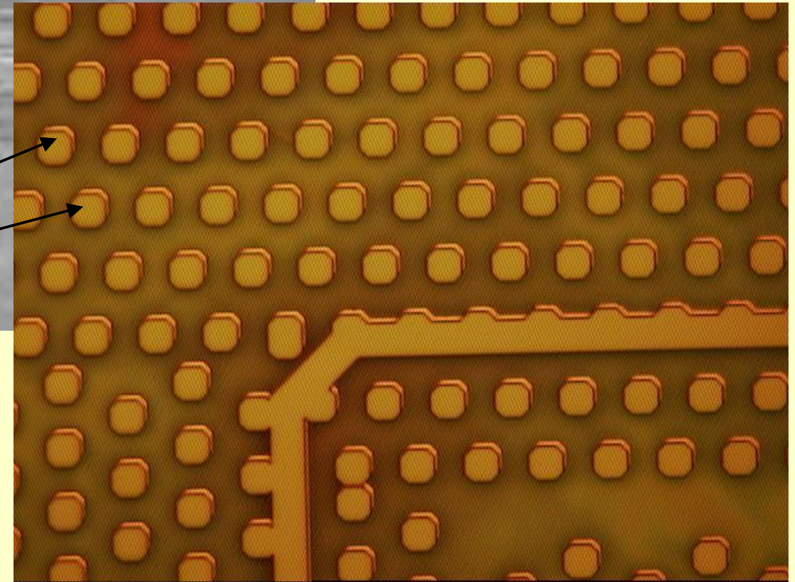


Tezzaron/Chartered 0.13 um Process

- **Large reticule – 24 mm x 32 mm**
- **8 inch wafers**
- **Features**
  - **Deep N-well,MiM capacitors – 1 fF/um^2 Single poly, 8 levels of metal available, Zero Vt (Native NMOS) available, variety of transistor options (Nominal,Low voltage,High performance,Low power)**
  - **Vias 1.6x1.6 x10um, pitch 3.3 um**
  - **Bond points Cu 1.7x1.7 um, pitch 2.4 um**
  - **Wafer bonding at 375 deg C**
  - **Alignment 3 sigma ~ 1 um**
  - **Missing bonds ~ 0.1 ppm**
  - **1500 Temp cycling -65deg/+150deg on 100 devices without failures**

•Eight

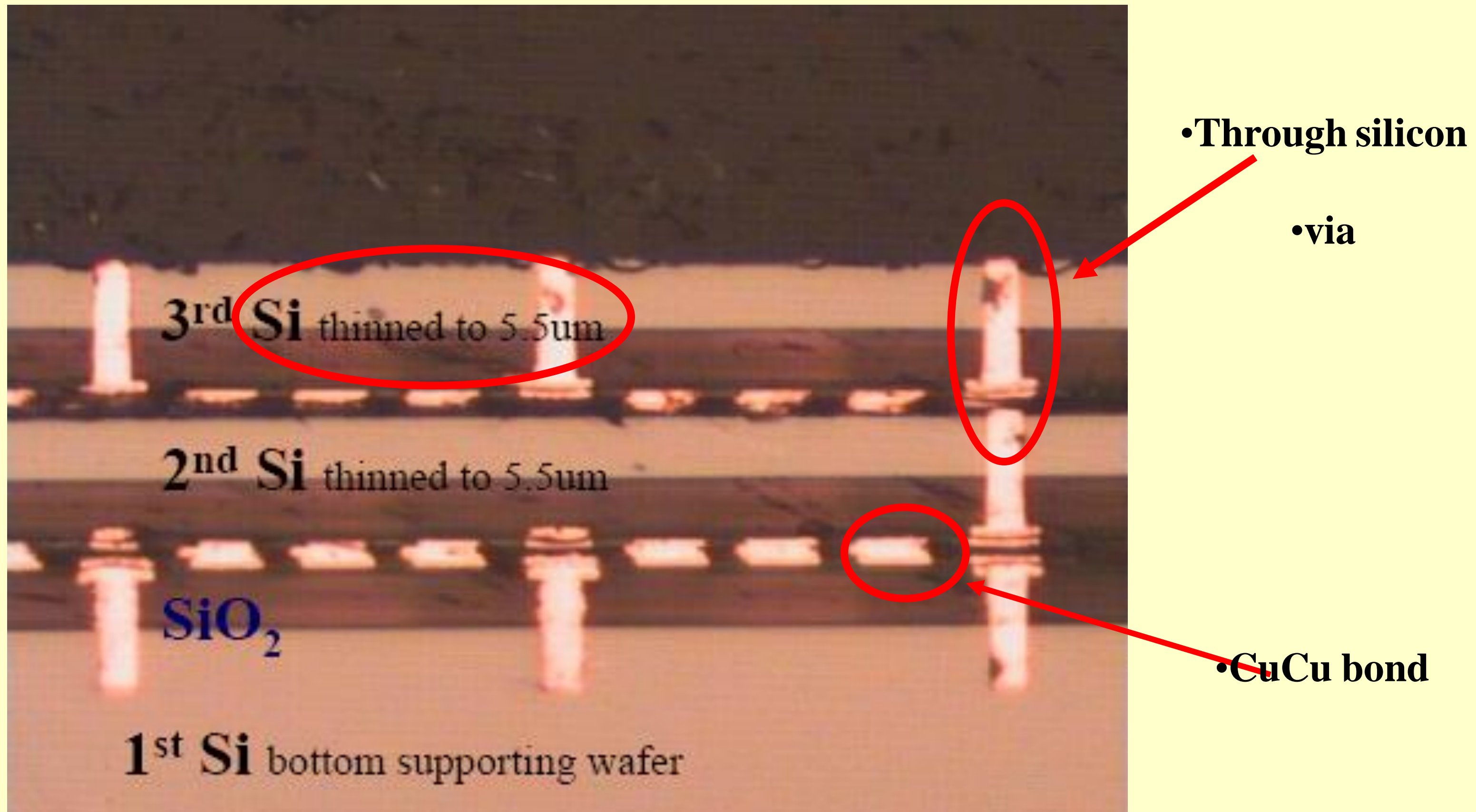
•inches



•Interconnect at 10um pitch

•10,000 I/O per sqmm

Cross section of Tezzaron 3 Layer Stack



Phase-II ATLAS ID Upgrade