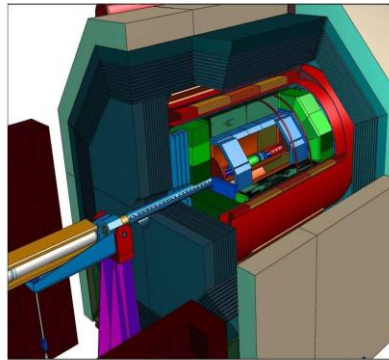




Some Studies on ILC Calorimetry



M. Benyamna, C. Carlogan, P. Gay, S. Manen,
F. Morisseau, L. Royer (LPC-Clermont)

&

Y. Gao, H. Gong, Z. Yang
(Tsinghua Univ.)



Topics of the collaboration

- Algorithm for photon identification
- Microelectronics for SiW ECAL

Very preliminary results !



γ at ILC: Why photon ID



- “Isolated” photon is an important probe for new physics at ILC, e.g.

Higgs:

$$H(h) \rightarrow \gamma\gamma$$

Graviton:

no-pointing γ

Extra-D:

$$\gamma + \textit{Emiss}$$

Excited States:

$$l^* \rightarrow l + \gamma$$

.....

- Suffers from high energy π^0 decays



Algorithm for Photon ID



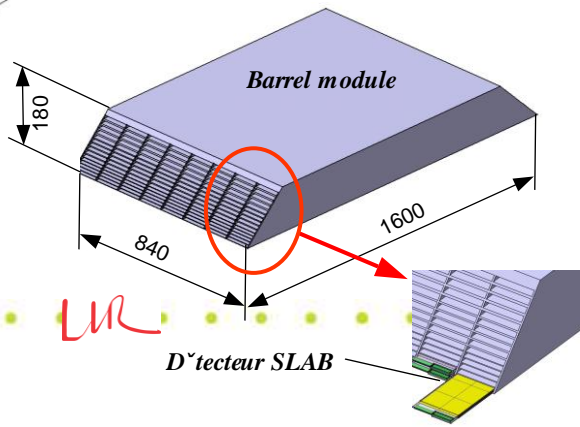
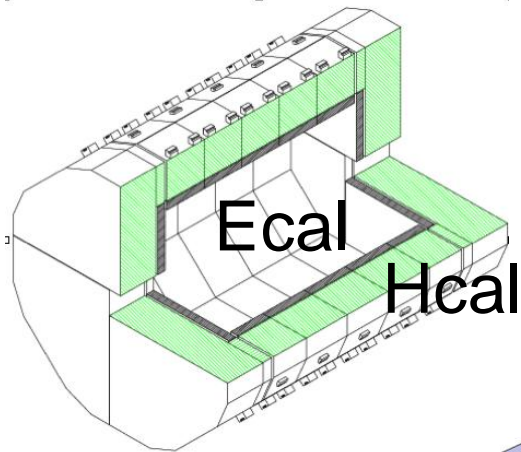
- A photon ID algorithm should provide:
 - Quality of an isolated EM cluster to be identified as a photon (preliminary result)
 - Discriminating power against π^0 (under study)
- Checked with MC and Test Beam data



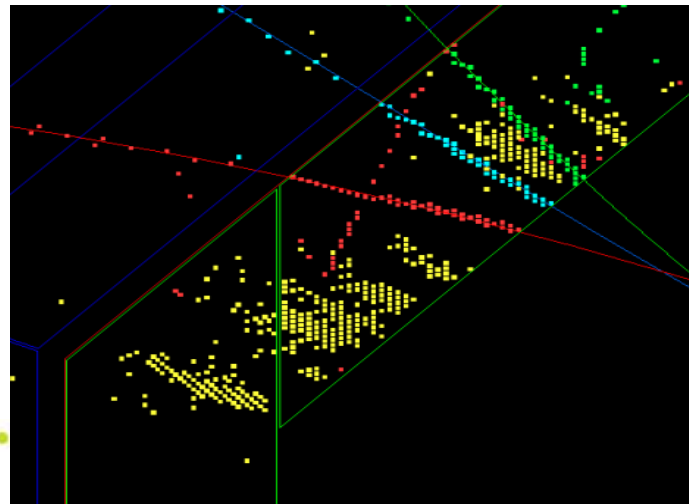
SiW ECAL for ILC



- The primary goal for SiW ECAL is jet reconstruction
- High granularity
- Also benefits to photon ID



$Z\gamma$	2 l, 2 jets
W^+W^-	1 l+2 jets, 4 jets
$t\bar{t}$	l+jets, 6 jets
$t\bar{t}h$	8 jets
hZ	2l+2 jets, 4 jets
hhZ	2l+4 jets, 8 jets
$\chi_1^0\chi_1^0$	jets + \cancel{E}
$\tilde{t}\bar{\tilde{t}}$	6 jets+ \cancel{E}
$R_p \chi_1^0\chi_1^0$	2l+ 4 jets, 6 jets
$R_p \chi^+\chi^-$	2l+ 6 jets, 10 jets





The algorithm

- Longitudinal profile of energy deposition in an EM cascades(1GeV-100GeV)

$$\frac{1}{E_0} \frac{dE}{dS} = \frac{\beta^\alpha}{\Gamma(\alpha)} S^{\alpha-1} e^{-\beta S}$$

$$\alpha = \frac{\langle S \rangle^2}{\langle S^2 \rangle - \langle S \rangle^2}, \quad \beta = \frac{\langle S \rangle}{\langle S^2 \rangle - \langle S \rangle^2}, \quad \frac{\beta}{\alpha} = \frac{1}{\langle S \rangle}$$

$$\langle S^n \rangle = \frac{\sum_{\text{layer}} E_l \times X_l^n}{\sum_{\text{layer}} E_l} \quad \left(\begin{array}{l} E_l : \text{energy in in each layer} \\ X_l : \text{particle range in radiation length unit} \end{array} \right)$$

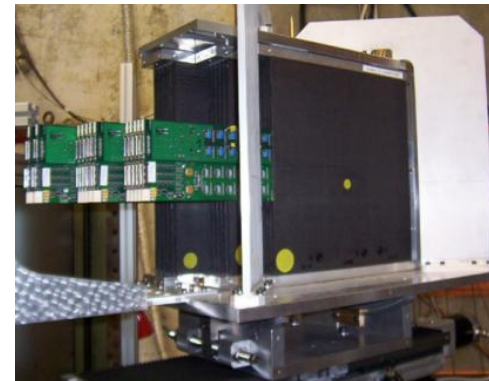
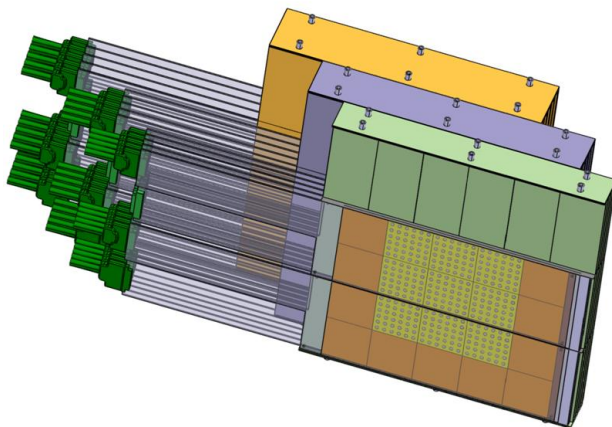
- Build an estimator based on α & β



The Prototype



- 30 layers
- The absorber(W):
 $0.4x_0=1.4\text{cm}$ for each of the 1st 10 layers
 $0.8x_0=2.8\text{cm}$ for each of the 2nd 10 layers
 $1.2x_0=4.2\text{cm}$ for each of the 3rd 10 layers
Absorber: totally $(1.4+2.8+4.2)*10=84\text{cm}$
Si, Al and others could be neglected.





Data samples



- MC data

Energy = {6, 10, 12, 15, 30, 45}GeV

$\theta = 0$

- Test beam data

Energy = {6, 10, 12, 15, 20, 30, 40, 45}GeV

$\theta = 0$

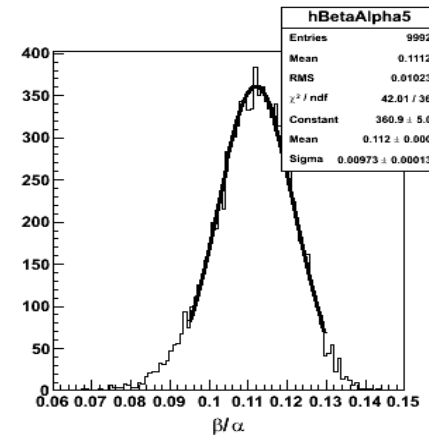
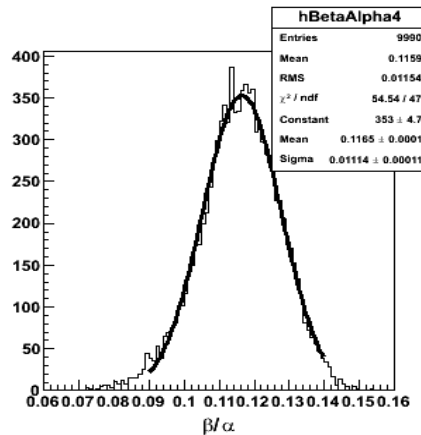
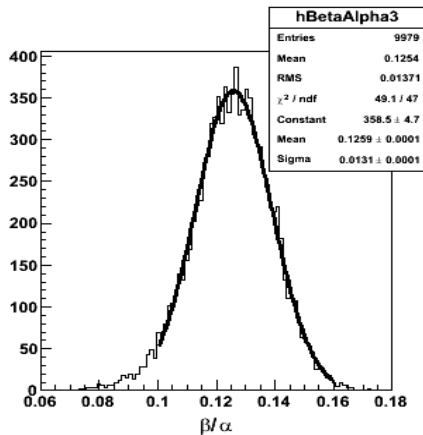
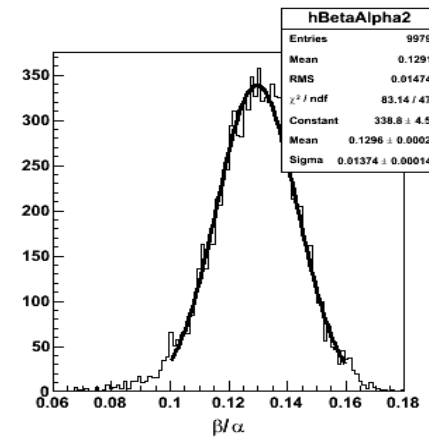
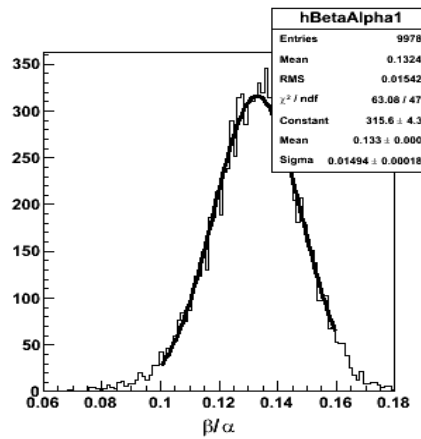
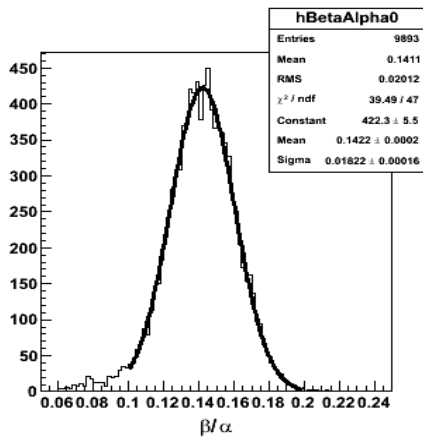
- Energy calibrated to MIPs (260MIPs~1GeV)



The estimator (1)



- MC studies show β/α distributed gaussian-like

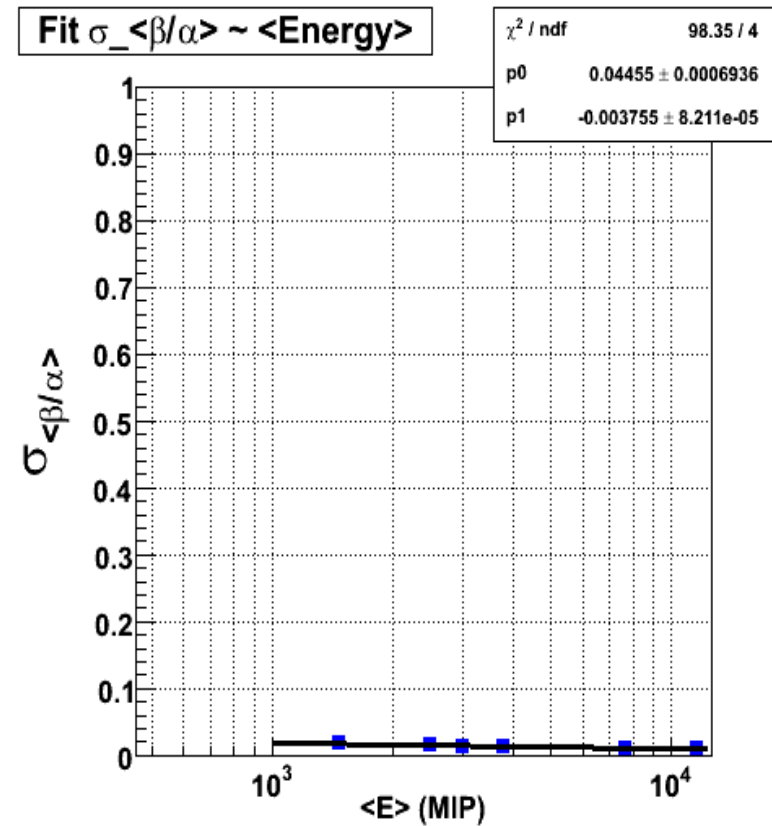
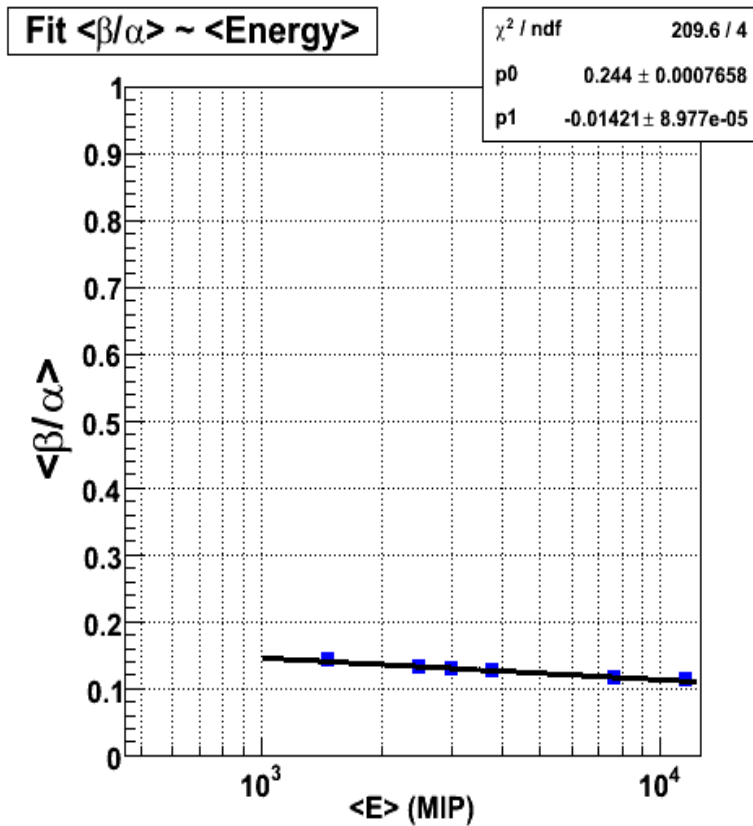




The estimator (2)



- Energy dependence





The estimator (3)



- MC studies suggest

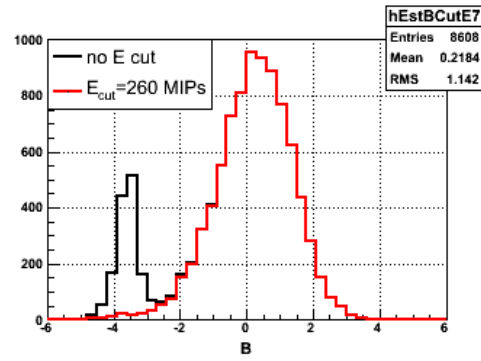
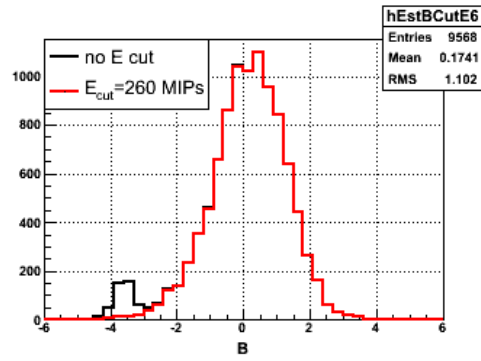
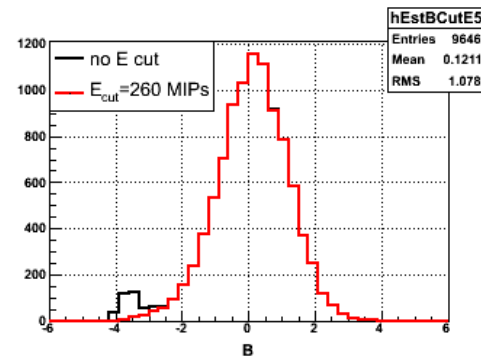
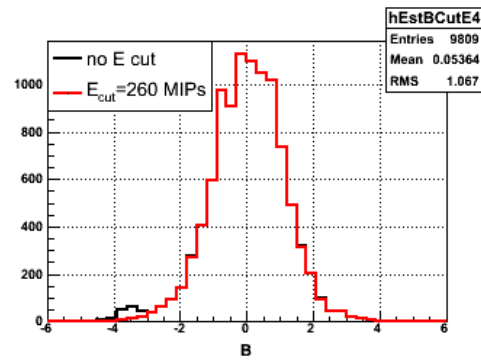
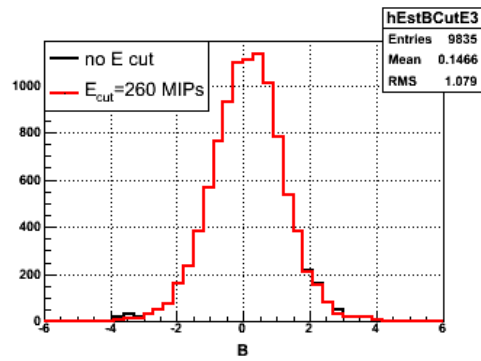
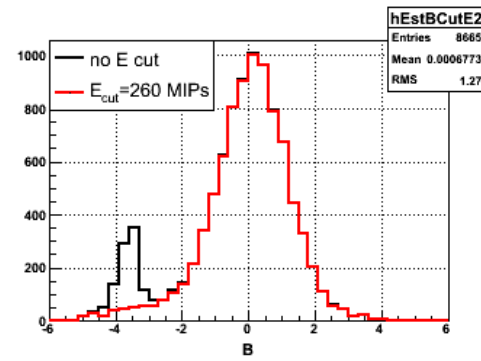
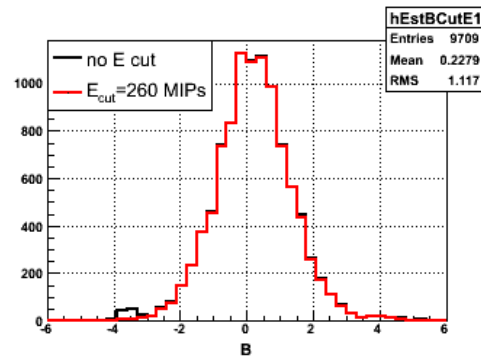
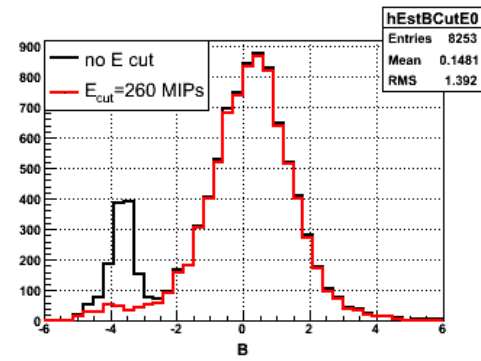
$$\frac{\frac{\beta}{\alpha} - \left\langle \frac{\beta}{\alpha} \right\rangle (E)}{\sigma_{\frac{\beta}{\alpha}}(E)} \leftarrow \text{From MC}$$

should follow normal distribution.

- As the very first step, we propose to use it as the estimator for photon ID



Checked by test beam data



$E > 1 \text{ GeV}$



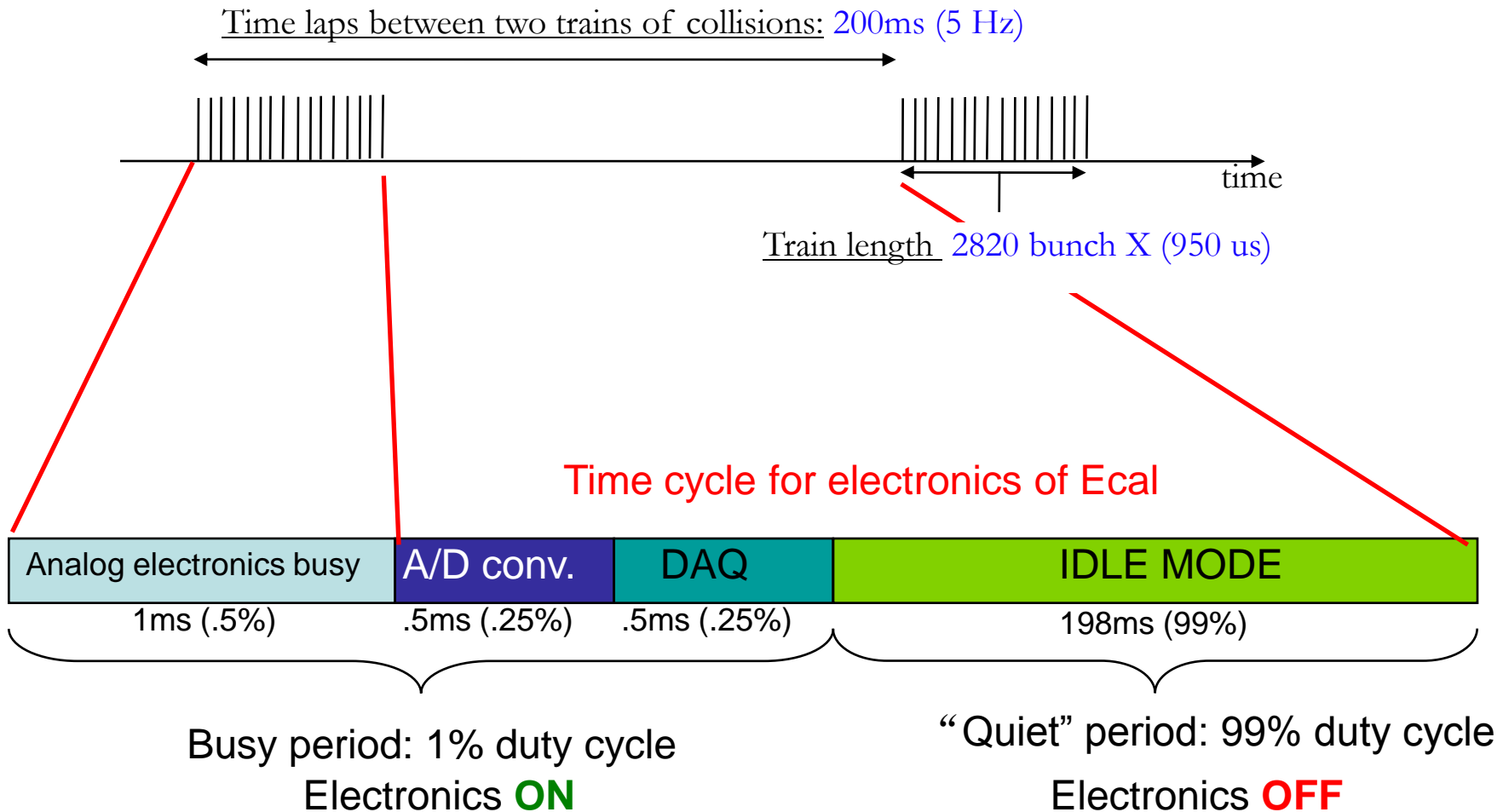
Summary of photon ID



- An estimator proposed
- MC/Data consistent with each other
- So far, only partial information are used.
More studies are underway
(likelihood, + transverse information ...)
- Eventually should be optimized towards
highest possible discriminating power
against neutral pion



Timing of ILC





Skills with development of ASIC for LHC



- ❑ LHCb experiment
 - Very-front-end electronics for the preshower detector (scintillators and photon multipliers)
 - Current amplifier, shaper (switched integrator), Track&Hold
 - \approx 2000 chips fabricated, tested and installed at Cern

- ❑ ALICE experiment
 - Very-front-end electronics for the dimuon trigger detector (resistive plate chambers)
 - Dual fast discriminator, "one shot", pulse shaping, tunable delay, LVDS driver
 - \approx 3000 chips fabricated, tested and installed at Cern



List of chips fabricated for ILC



- ✓ R&D started @ LPC in 2002 with a PhD student
- ✓ 12 chips designed, fabricated and tested

avr.-02	AMS BiCMOS 0,8	Intégrateur
nov.-02	AMS BiCMOS 0,8	2 comparateurs: entrées bipolaire et MOS
juin-03	AMS CMOS 0,35 csi	ADC pipeline 10bits + comparateur + amplis (gains 2 et 100)
avr.-04	AMS CMOS 0,35 c35b4	Comparateur et ampli. boucle ouverte
juin-04	AMS CMOS 0,35 c35b4	ADC pipeline 10 bits
juin-05	AMS CMOS 0,35 c35b4	Comparateur et ampli. boucle ouverte
juin-05	AMS CMOS 0,35 c35b4	ADC pipeline 10 bits
juil.-05	AMS CMOS 0,35 c35b4	Circuit commun: préampli (LAL) + 3 shapers (LPC) gain 1, 9 et 40
avr.-06	AMS CMOS 0,35 c35b4	ADC pipeline 10 bits 1,5 bit par étage 5V
juil.-06	AMS CMOS 0,35 c35b5	1 étage ADC pipeline 1,5 bit par étage 3V
sept.06	AMS SiGe S35b4	ADC rampe 12 bits 50MHz
mars-08	AMS CMOS 0,35 c35b4	ADC cyclique 12 bits - 1MS/s -3,5V



R&D on ADC



- ❑ Performance required for Si-W VFE electronics:
 - Resolution of 12 bits
 - Compactness → one ADC per channel
 - Power consumption of few μW with power pulsing
 - Time of conversion: up to few μs

- ❑ Three types of ADC designed:
 - 12-bit Wilkinson (ramp ADC) architecture for the SKIROC chip
 - **simplest architecture but too high consumption**
 - **limited precision**
 - 10-bit pipeline architecture
 - **well adapted if one ADC shared by tens of channels**
 - **limited precision**
 - 12-bit cyclic architecture
 - **performance well adapted to Ecal**
 - **same building blocks than pipeline ADC (upgraded to 12-bit resolution)**

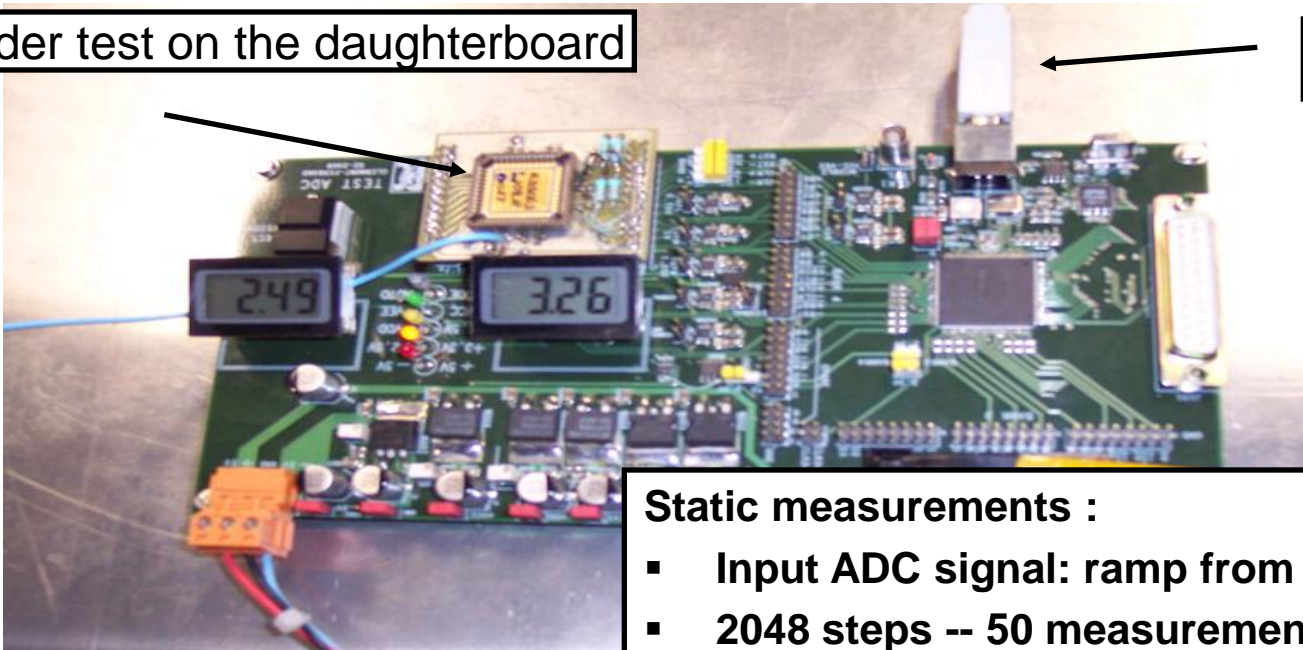
Measurement setup

Test Bench: fast and precise measurements (static)

- Generic board for ADC tests designed @ LPC (electronic service)
- Analogue signal generator: DAC 16 bits (DAC8830)
- PC/LabView Slow Control through **USB** interface
- FPGA + VHDL code to control USB interface, DAC, to generate clocks ...
- Data acquires processed with **Scilab** package

Chip under test on the daughterboard

USB link

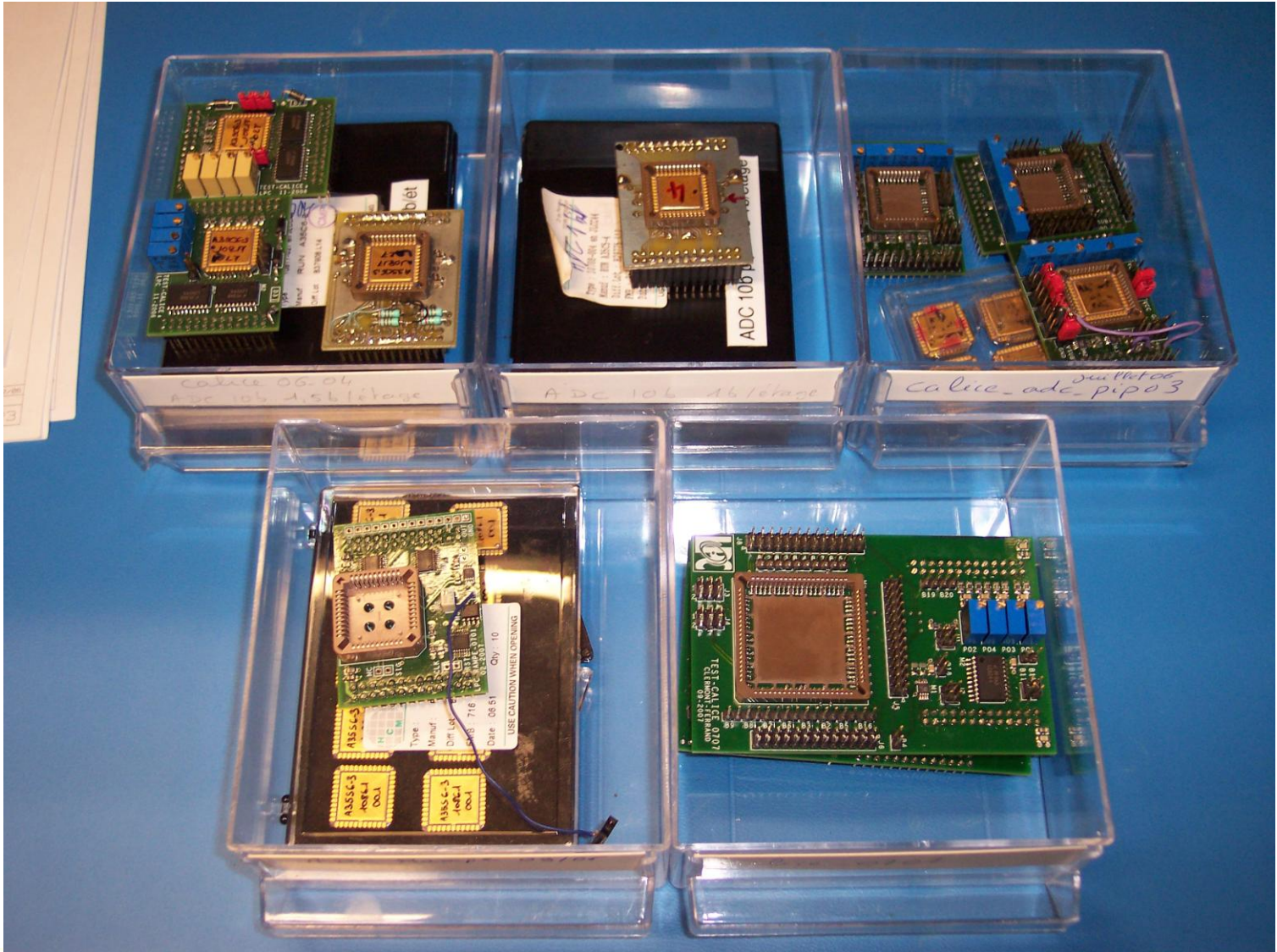


Static measurements :

- Input ADC signal: ramp from 0 to 2V
- 2048 steps -- 50 measurements / step



Some daughterboards





Collaboration plan



- Chips designed in LPC so far
- Elaboration and design of the test bench by Tsinghua
- Elementary part of the chip may be designed by Tsinghua in the future (transformation of knowledge)

Calorimetry for International Linear Collider

Beijing, China. April 22-26, 2009.

Organizers: Roman Poeschl (LAL)
Yuanning Gao (Tsinghua Univ)

Sponsors: [China Center of Advanced Science and Technology \(CCAST\)](#)
[Center for High Energy Physics, Tsinghua University \(TUHEP\)](#)

Lecturers: Paul Dauncey (*Imperial College*)
Christophe De La Taille (*Laboratoire de l'Accélérateur Linéaire – Orsay*)
Imad Laktineh (*Institut de Physique Nucléaire de Lyon*)
Lucia Linssen (*CERN*)
Roman Poeschl (*Laboratoire de l'Accélérateur Linéaire – Orsay*)
Frank Simon (*Max-Planck-Institut für Physik - München*)
Tohru Takeshita (*Shinshu University*)
Mark Thompson (*University of Cambridge*)
Jae Yu (*University of Texas Arlington*)