

# R&D Collaboration between DUT (Dalian University of Technology) & IPHC (Institut Pluridisciplinaire Hubert Curien)

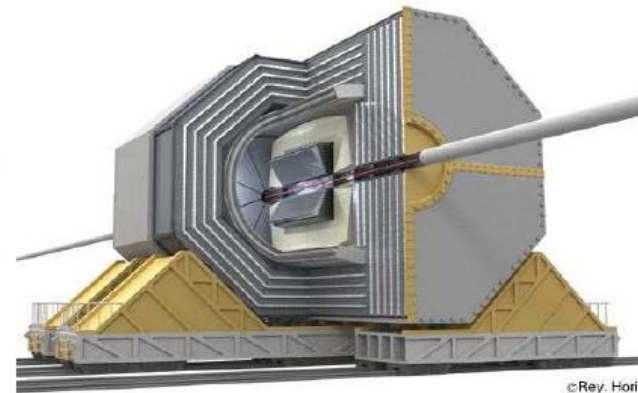
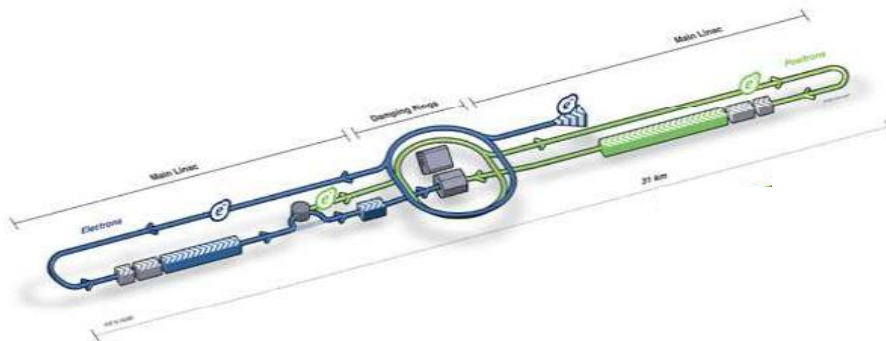
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- **Particle detector (ULP Strasbourg)**
- **Micromachining technology (DUT)**

# IPHC: MAPS development

- Since 1999, the CMOS sensor group at IPHC led by Marc Winter has worked on R&D of MAPS (Monolithic Active Pixel Sensors) for future vertex detectors and imagers for bio-medical applications
  - ↳ MAPS is also called "CMOS" sensors
- Future ILC vertex detectors need:
  - ↳ Excellent reconstruction of secondary vertices
    - Granularity & low material budget
  - ↳ Precise measurement of the momenta of tracks
  - Improve the system's accuracy by an order of magnitude w.r.t. the state of the art



→ MAPS provide an attractive trade-off between granularity, material budget, readout speed, radiation tolerance and power dissipation

## ■ MAPS: the sensitive volume and the front-end readout electronics integrated on the same substrate

↪ Charge collection: epitaxial layer (substrate)

## ■ Achieved performances:

↪ *Single point resolution ( $> \sim \mu\text{m}$ )*

↪ *Material budget  $\rightarrow 50 \mu\text{m}$  thin sensors*

↪ *Radiation tolerance ( $\sim 10^{13} \text{Neq} / \text{cm}^2$ ,  $\sim 1 \text{Mrad}$ )*

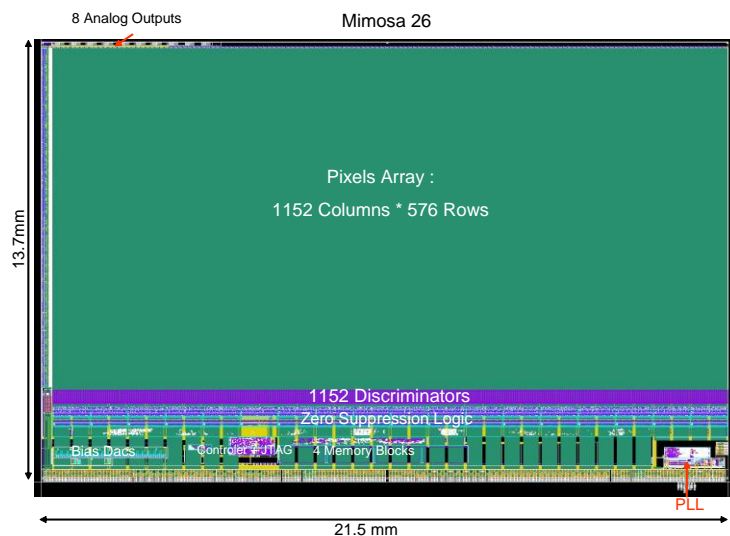
↪ *Speed ( 1-10 G pixels / sensor / s)*

■ *10 k frame / s*

↪ *Power consumption  $O(100 \text{ mW} / \text{cm}^2)$*

# Main R&D Direction: (Detection & Signal Processing)

- High readout speed, low noise, low power dissipation, highly integrated signal processing architecture:
  - ↪ Analogue part (charge collection, pre-amplifier, CDS,...) inside pixel
  - ↪ Mixed (ADC) and digital (sparsification)  $\mu$ -circuits integrated inside pixel or aside of active surface
  - ↪ MIMOSA26 (21.5x13.7 mm<sup>2</sup>): 1st sensor with digital output and integrated zero suppression



- Radiation tolerance:
  - ↪ Minimize dark current (after irradiation)
    - Room temperature operation
    - Specific layout
  - ↪ Design against Latch-up
    - Specific layout and proper technology

# Micromachining Technology (DUT)

## ■ Study of thinning procedure:

↳ Minimal thickness → minimal material budget

- Mechanical properties
- Accuracy tool dependency

↳ Individual chips rather than wafer → yield

## ■ Study of edgeless dicing procedure:

↳ Minimise insensitive areas when several sensors needed to cover a large detection geometry

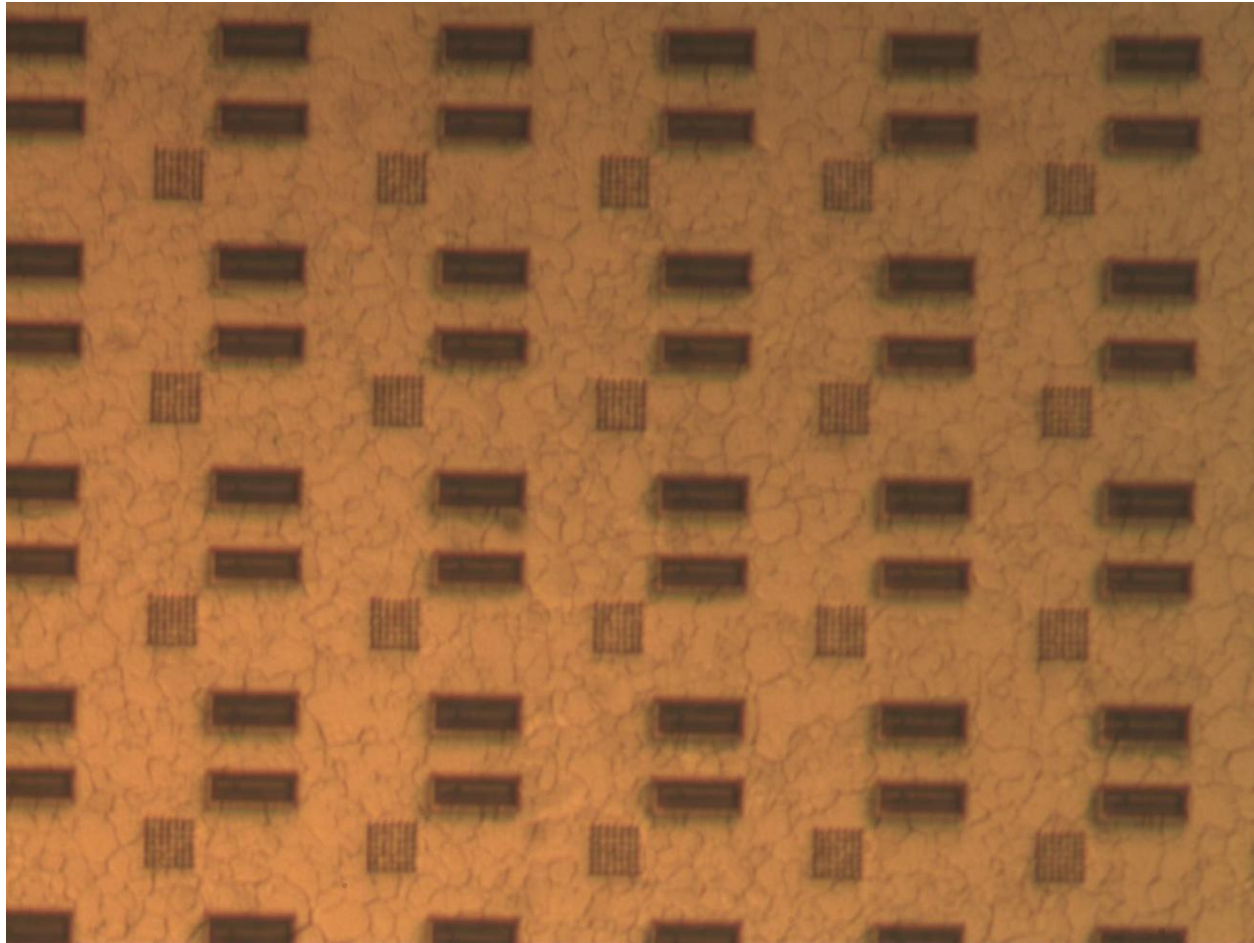
- Accuracy tool dependency

## ■ Optimisation of the thickness value of the epitaxial layer to have maximum charge collection

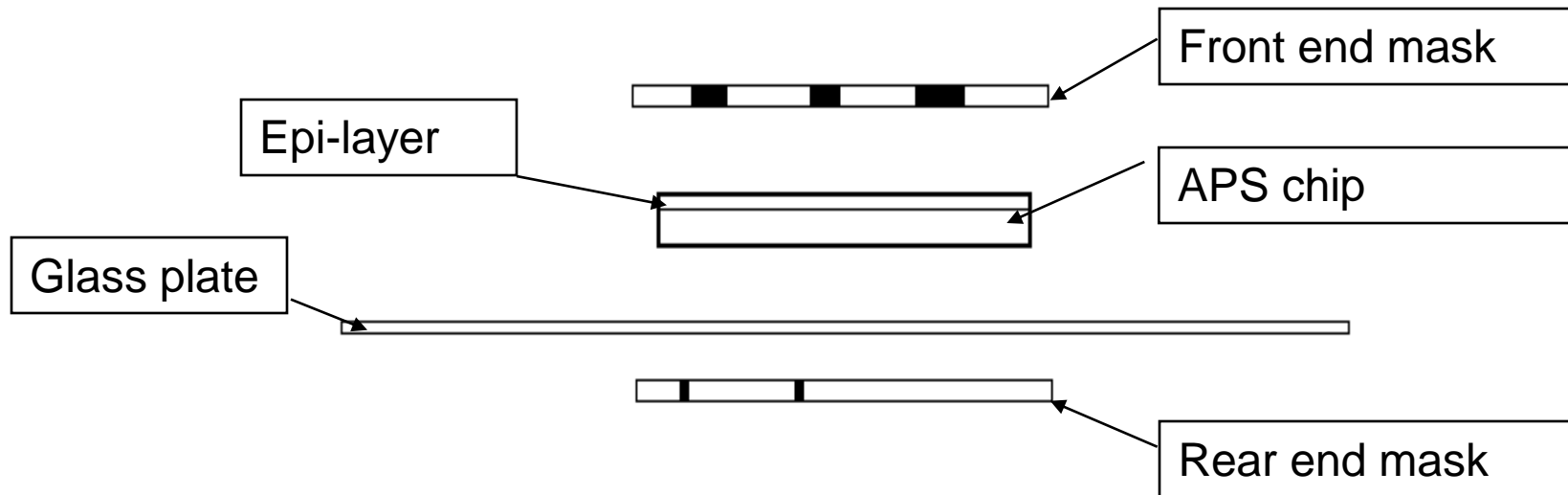
↳ New facility in DUT

# Joint research project

- Thinning and Edgeless Dicing



# Basic procedures







大连理工大学 – 法国斯特拉斯堡大学

# 集成电路联合实验室

DUT-ULP Integrated Circuits Joint Lab



# Professors and Students program

- Prof. Yann Hu of ULP Strasbourg is a visiting Prof of DUT and give one month teaching to DUT student every year
- Li Jinfeng, 2006, France doctor program, 3 months, ADC design
- Fu Min, FCPPL-CSC, one year, IC and detector design.

## R&D Domain:

- **Microscale heat transfer in Microdevices**
- **Integrated Circuit Design**
- **Microsensors**
- **Micro/Nano Machining Technology**

## Current Projects

- **SoC of MicroPirani Pressure Sensors array Combine with their Drive and signal Process Circuits, NSFC, 2M ¥**
- **Data Fusion of MultiSensors of a Chemical Production Vehicle for Safety Monitoring, 11.4M ¥**
- **Heterogeneous Multiprocessor System on Chip for Wireless Applications, Intel and DUT joint project, 150,000 ¥ 。**

# Superiority of DUT in semiconductor technology

- Intel has announced to build *Fab 68* in Dalian since September 2007.
- 300mm wafer line, 90nm CD dimension
- Focus on chip set.
- 2010 first production.



# Superiority of DUT in semiconductor technology (cont')

- Intel decide to construct a Semiconductor Technology School (STS) in Dalian by collaboration with Dalian government and DUT.
- Intel's contribution is to donate an 8 inch equipments to the STS.





# Superiority of DUT in semiconductor technology (cont')

- The equipments are mainly from an 8' Feb in US.
- 0.25 CD.
- In total, the initial value of the donated equipment is more than 44 million\$
- 90M¥ for cleanroom construction
- The Lab. will open to be used soon.



# Platform of Integrated Circuit Design

- Mentor Graphics donated IC design tools of \$60M



# Cooperation with IMEC



**CEO of IMEC visit DUT and Dalian mayor**

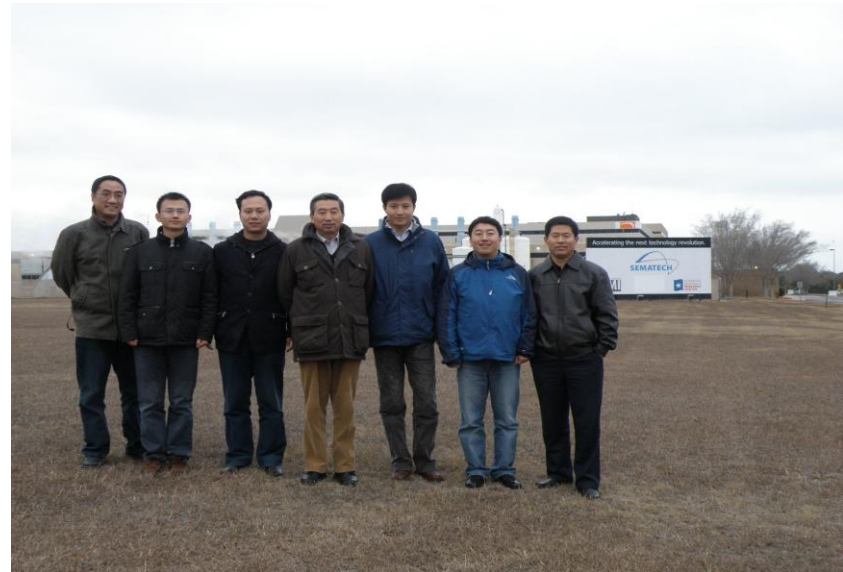


# MOU between IMEC and DUT

- **IMEC and DUT will explore the possibility of cooperatively carry out research and development in the field of More Than Moore.**
- ....
- **In order to execute the above mentioned cooperation, IMEC has intention to explore the possibility of setup its China branch “IMEC China” in Dalian.**

# Cooperation with SEMATECH of US

- Vice CEO of SEMATECH Mr. Raj Jammy and chief technologist Prof. Hsing-Huang Tseng and DUT team discussed coop project on 3D in detail.



# Cooperation with IEEE EDS

- IEEE EDS Dalian chapter
- Workshop, Oct., 2009



# Final words

- **DUT is very happy to be a member of FCPPL**
- **It is very important for DUT to enhance cooperation with FCPPL**
- **You are warmly welcome to visit DUT and try to cooperate with DUT in semiconductor technology domain.**

**Thanks for your attention!**