IN2P3

Omega

FCPPL 09
Microelectronics

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*OMEGA-LAL Orsay
** IHEP Beijing

http://omega.in2p3.fr

Orsay MicroElectronic Group Associated

OMEGA-IHEP collaboration (2008)

- Collaboration laid out at Beijing in april 07 around a pekinese duckling
- Proposed to Host chinese pHD student in Orsay in 2008
- Goal : design common chip for PM readout and sharing building blocks
- Later perform joint measurements in Beijing and Orsay

OMEGA-IHEP collaboration (2009)

- Wei Wei has stayed 6 months in Orsay (feb08-aug08)
  - Long time needed to go through the visa procedure !
  - He has joined the PMm2 project (and paid by ANR)
  - He has designed several parts of the ASIC PArISROC developped for PMm2 (high speed amplifier, Wilkinson ADC and TDC)
  - He has made himself very well integrated in the design team
  - He co-signs the publications and presentations of the ASIC (NNN08 Paris and TIPP09 Tsukuba)
  - He will participate to the comparative measurements starting mar 09

OMEGA-IHEP collaboration (2009)

- Xiongbo Ian is staying one year in Orsay
  - He arrived in nov 08 (paid by CAS)
  - He has joined the CALICE (ILC) ECAL project
  - He participates to the design of SKIROC : Silicon Kalorimeter Readout Chip for CALICE
  - He is also very well integrated !

IN2P3

Omega

PArISROC

Photomultiplier Array Integrated in Sige Read Out Chip

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TIPP09
Tsukuba

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* IHEP Beijing

PMm²

Orsay MicroElectronic Group Associated

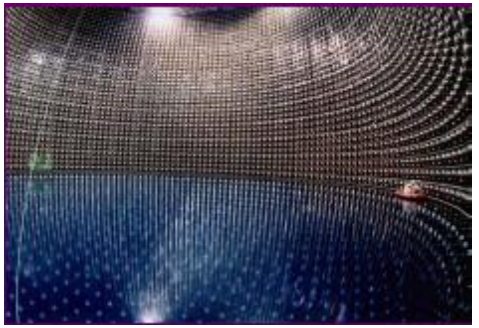
PMm² project (1)

- ***PMm² :*** *"Innovative electronics for array of photodetectors used in High Energy Physics and Astroparticles".*

- R&D program funded by French national agency for research (ref. ANR-06-BLAN-0186) (LAL, IPNO, LAPP and Photonis) (2007-2010)

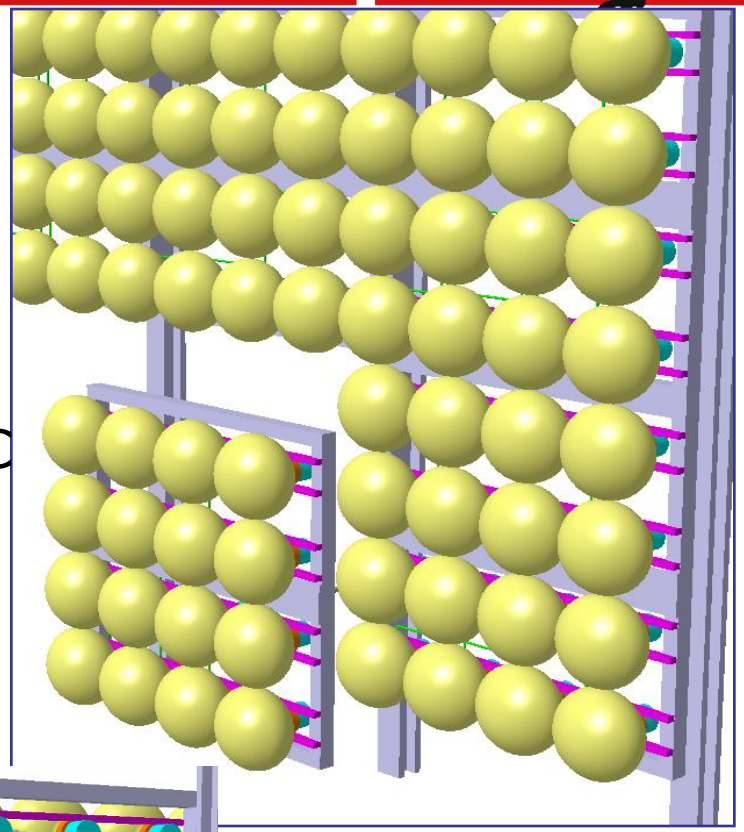
- Application : large water Cerenkov neutrino

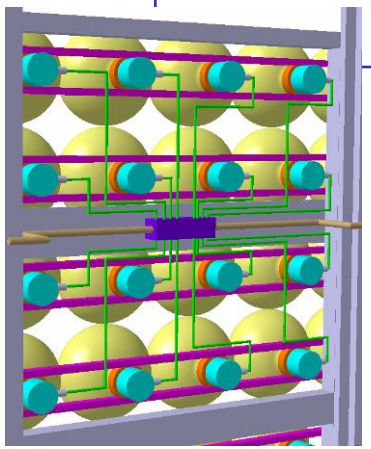
  (more generally: exp. with large number of PMs)



PMm^2 project (2)

- The project proposes to segment the very large surface of photodetection in macro pixels made of 16 photomultiplier tubes connected to an autonomous front-end electronics.
- Replace large PMTs (20") by groups of 16 smaller ones (12") with central ASIC
  - **Independent channels**
  - **charge and time measurement**
  - **water-tight, common High Voltage**
  - **Only one wire out (DATA + VCC)**
- **Target :**
  - **1pe efficiency**
  - **Triggerless**
  - **1ns time resolution**
  - **High granularity**
  - **scalability**
  - **Low cost**

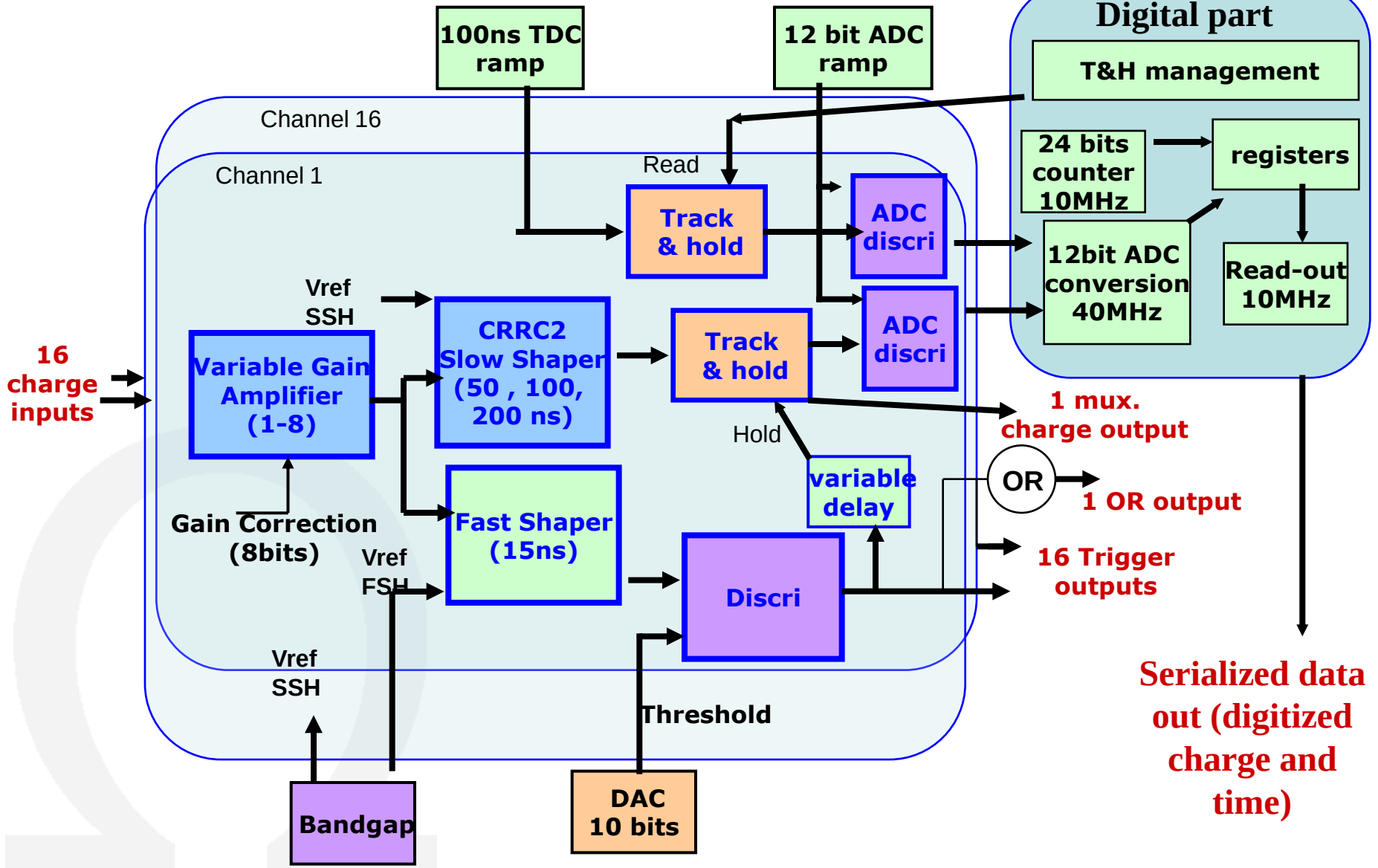




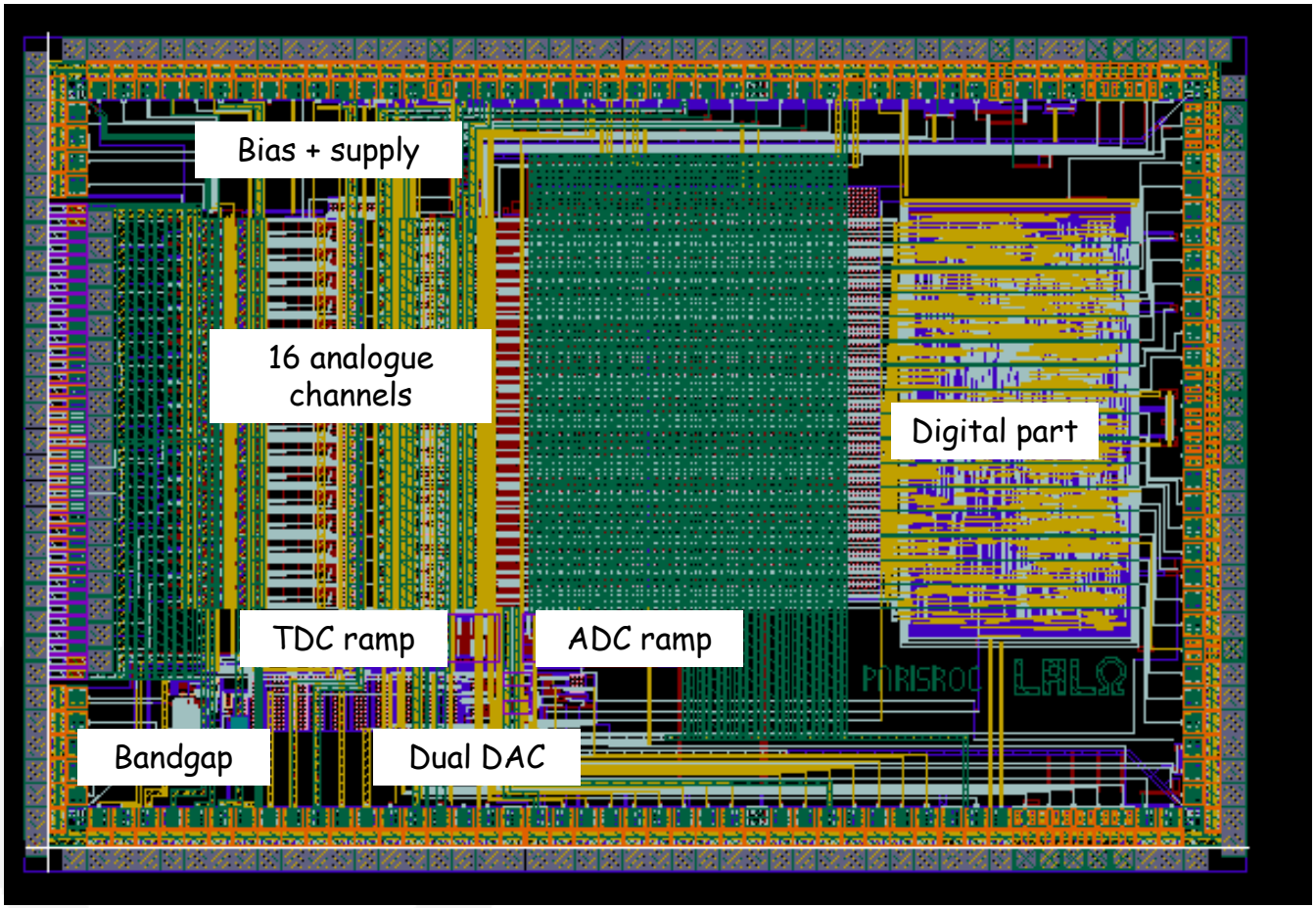
PARiSROC description (1)

- Characteristics :
  - 16 preamplifier inputs
    - Variable gain :1 → 8 (3bits) (common on 16 channels)
    - PMTs gain adjustment by a factor 4 (8 bits) (channel by channel)
    - Input dynamic range : 0 → 300 pe (0 → 50pC) with 1% linearity
  - 16 trigger outputs:
    - Fast shaper (τ=15ns) + low offset discriminator
    - Threshold provided by common internal 10bit DAC (1/3 pe)
    - "OR" of 16 triggers output
  - 1 digitized and multiplexed charge output :
    - Slow shaper with variable shaping time (τ=50ns,100ns,200ns)
    - Dual Track & Hold + multiplexed analog output or internal ADC
  - 8 to 12-bit internal ADC (Wilkinson) for charge and fine time measurement
  - Internal TDC : 24 bits counter (coarse) + fine 1 ns
  - One serial output : 2channel number + BCID + Charge + time
  - Dissipation : 5mW/ch

PARiSROC architecture



PARiSROC layout



Technology :

AMS SiGe 0.35µm

Size **:**

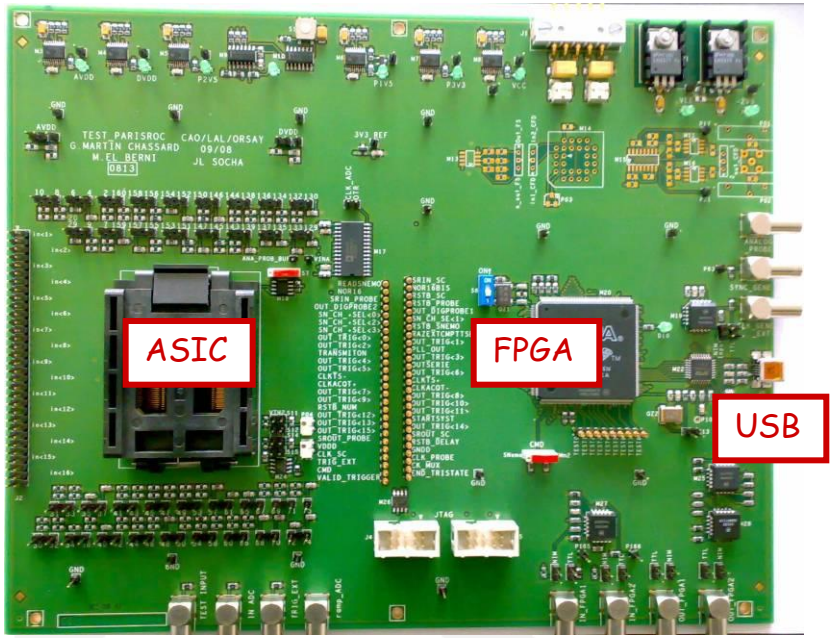
5mmX3.4mm

Package **:**

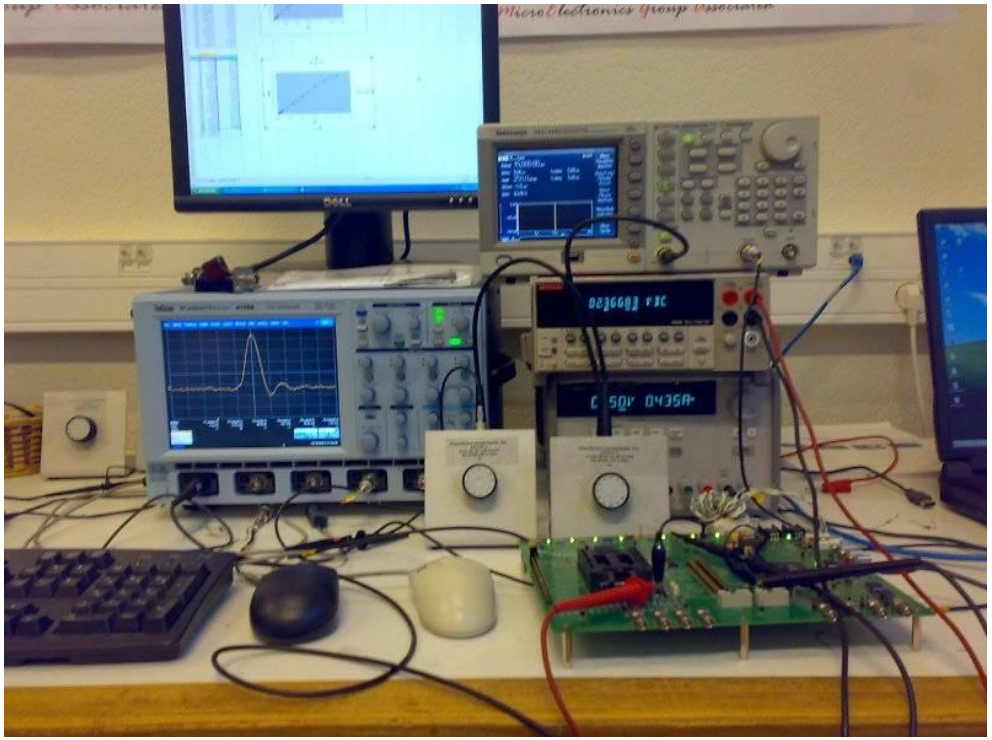
CQFP160

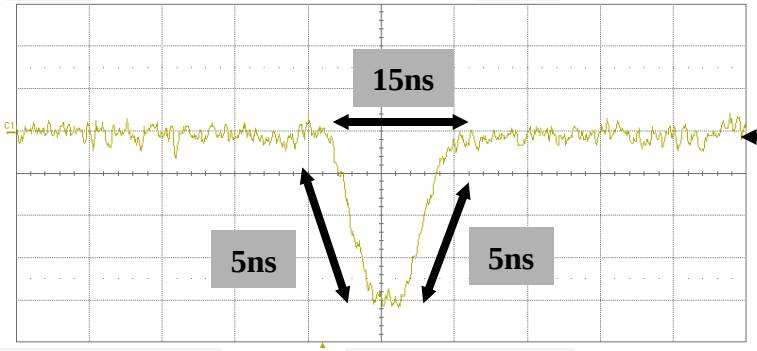
Measurements

TEST BOARD



TEST BENCH



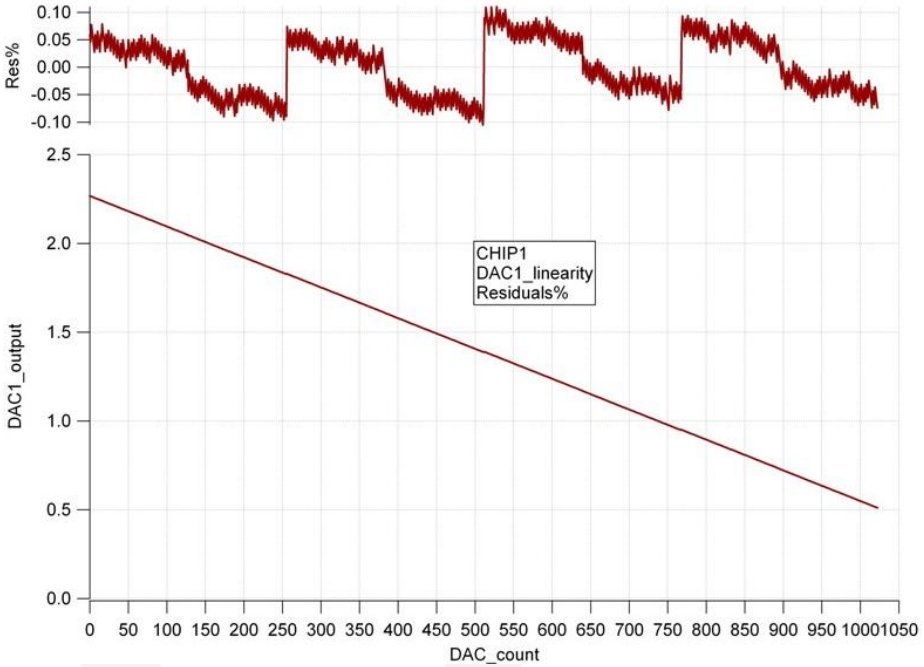


input signal : *Ii= 0 to 5mA*
0 to 300 pe → 0 to 50 pC
PM's Gain=10⁶ (1pe=160 fC)

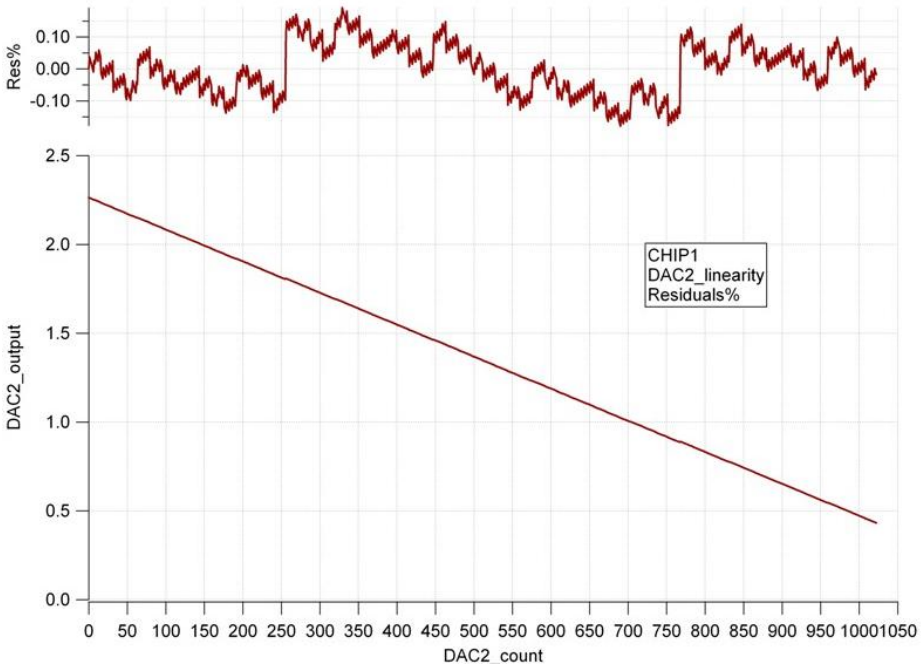
Internal 10bit DAC linearity

	Residuals(%)
DAC1_Chip 1	-0.1 to 0.1
DAC2_Chip 1	-0.1 to 0.1

DAC1_LINEARITY_CHIP1



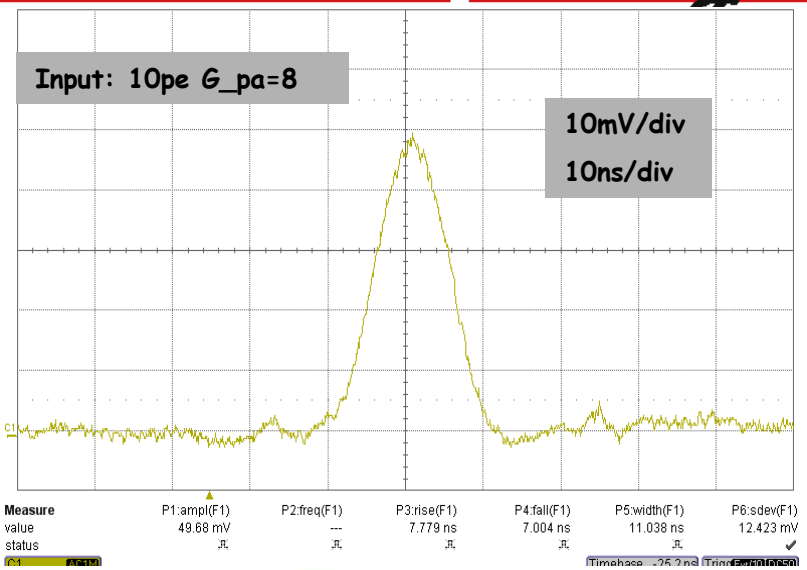
DAC2_LINEARITY_CHIP1



Preamplifier measurements

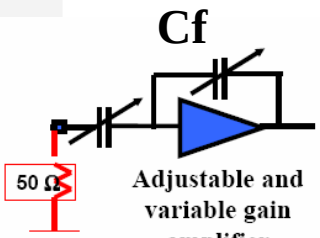
Preamp	meas	sim
Vout(1pe)	5 mV	5.2 mV
Rms noise	1 mV	316 μV
Noise in pe	0.2	0.06
SNR	5	16

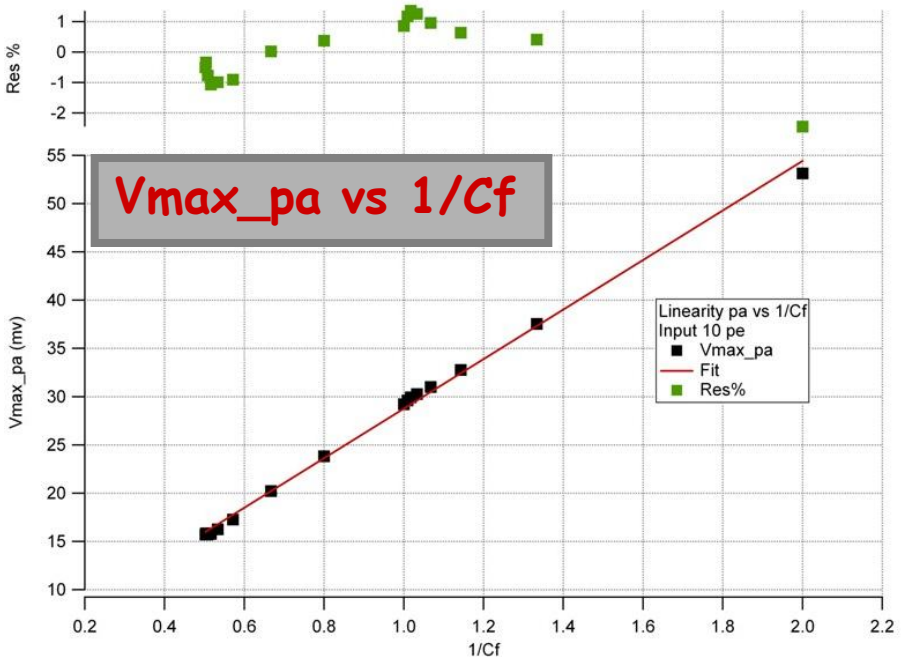
Some clock noise and low frequency noise under investigation



Gain adjustment linearity :

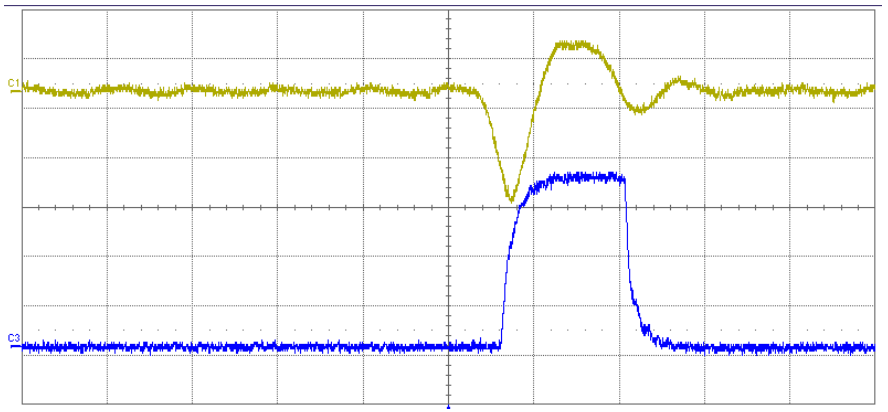
- **Vout/vin = Cin/Cf**
- **8 bits range**
- **2% non linearity**

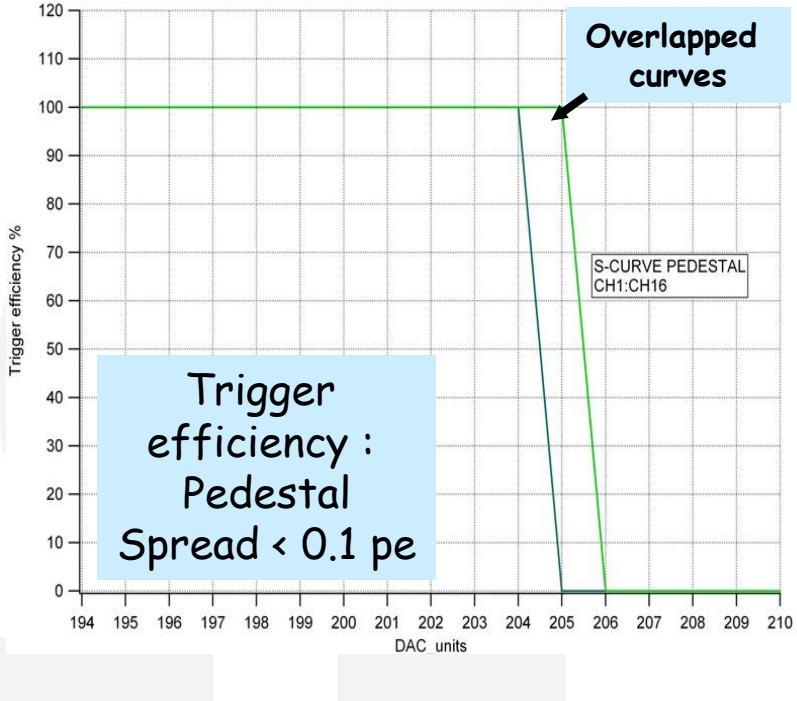


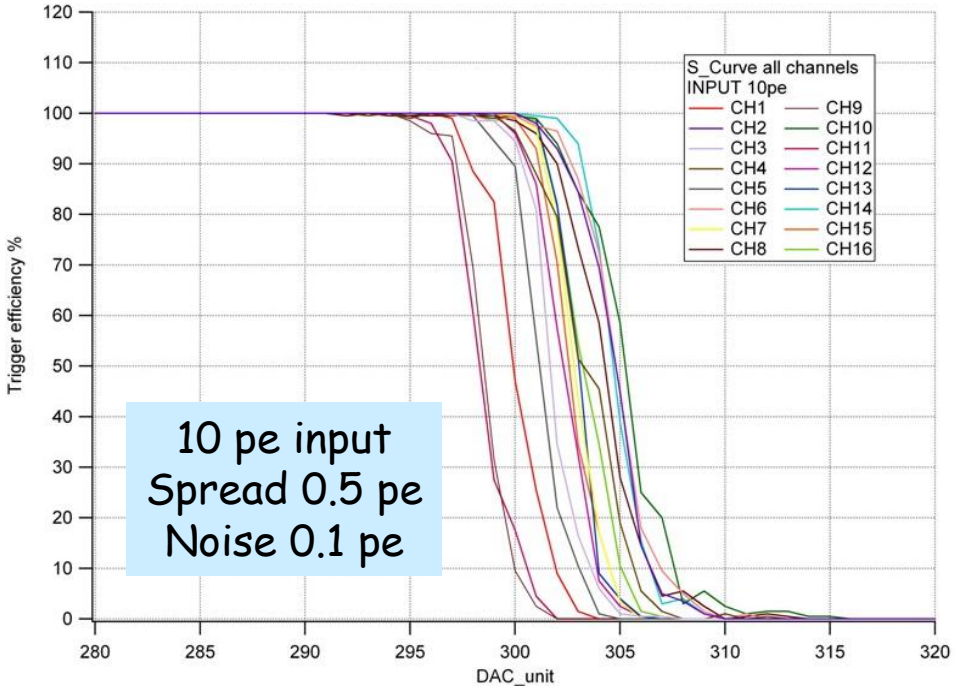


Fast shaper and discriminator

Fast shaper	meas	sim
Vout (1pe)	30 mV	37 mV
Rms noise	2.5 mV	2 mV
SNR	12	16
Rise time	7 ns	5 ns



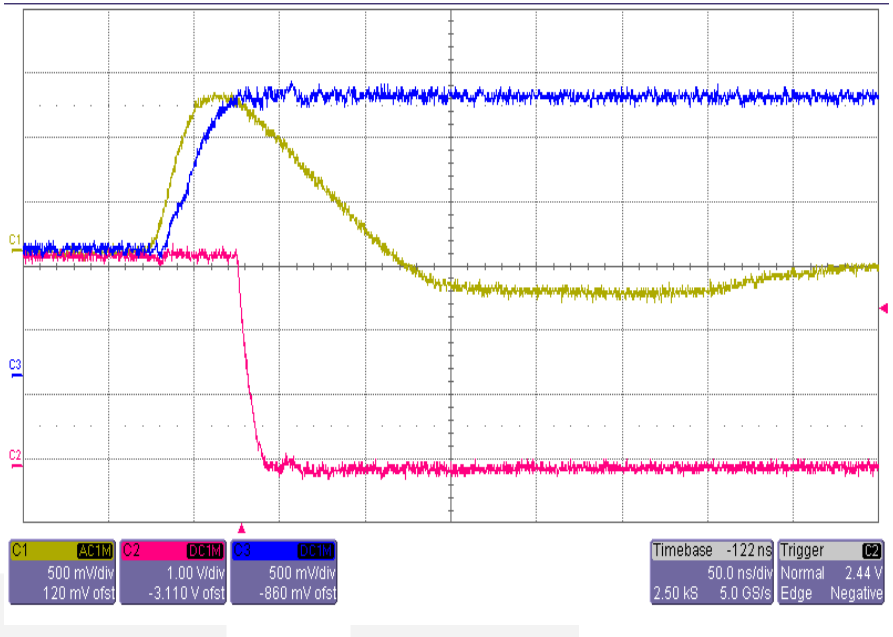


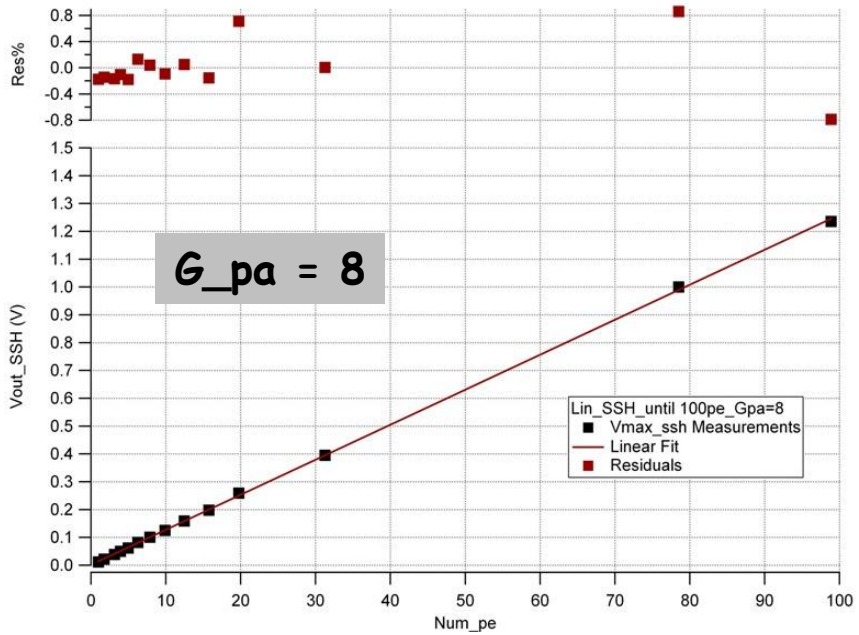


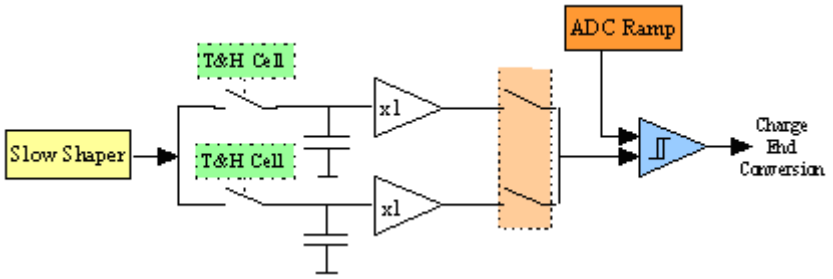
Slow shaper

Slow shaper	meas	sim
Vout (1pe)	12 mV	18 mV
Rms noise	3.5 mV	1 mV
SNR	3.5	18
Rise time	28 ns	27 ns

Low frequency to be understood and removed (power supply noise ?)



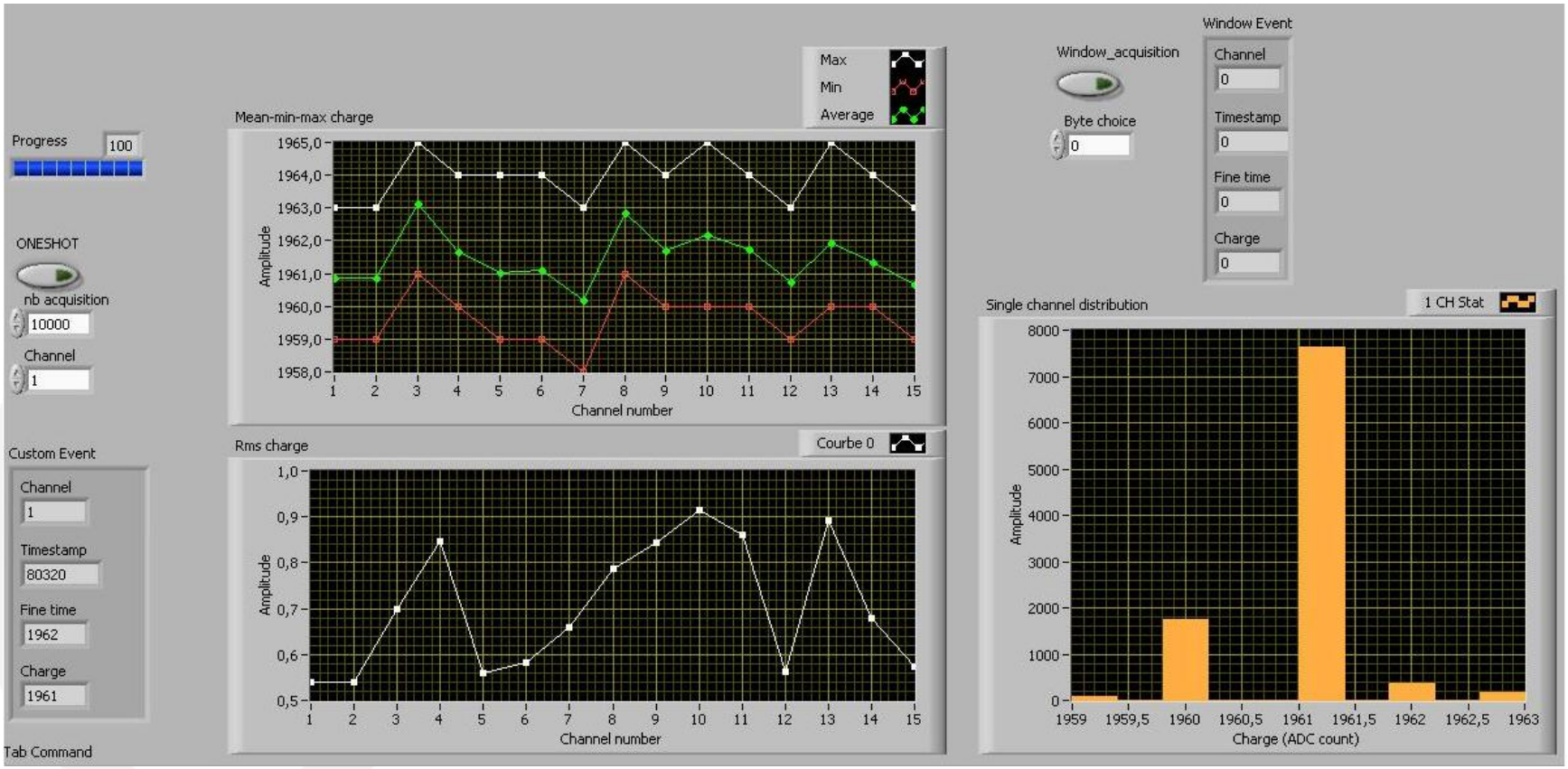




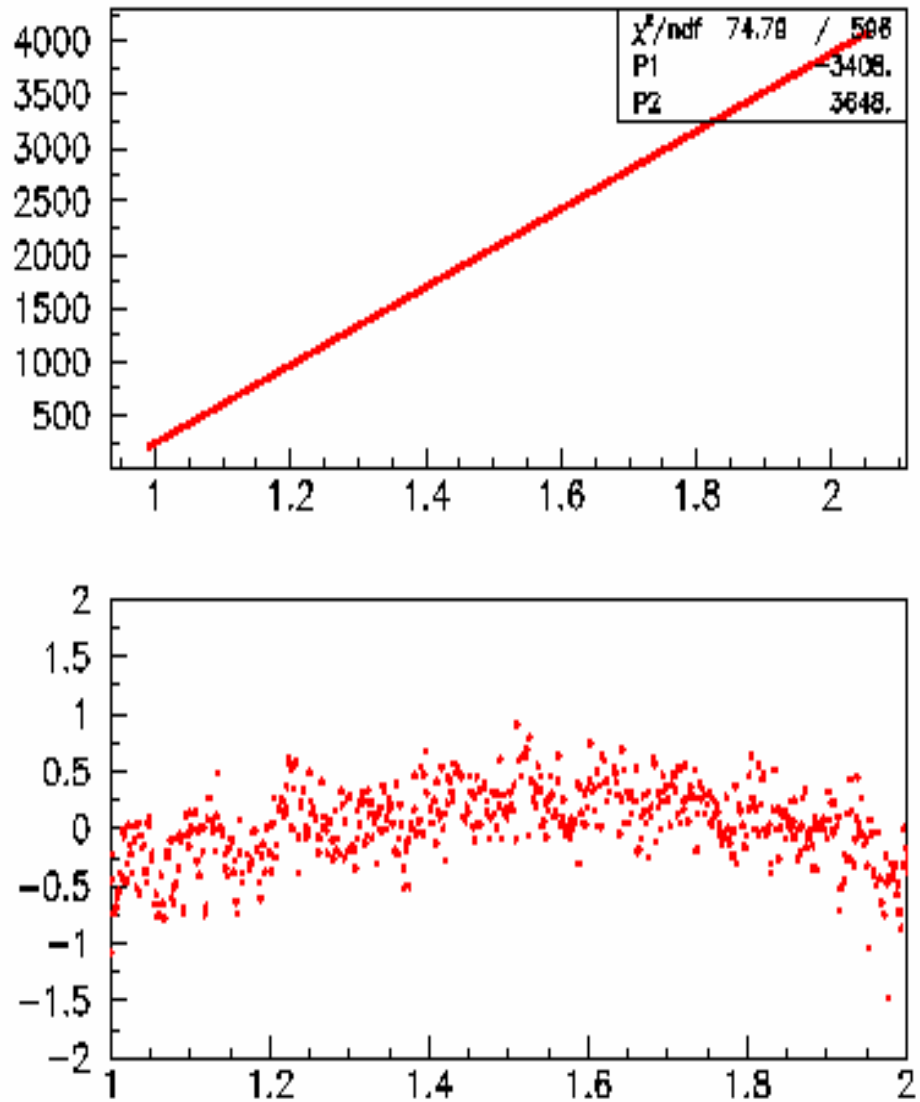
Internal 12bit Wilkinson ADC

Input signal : DC = 1.4523V (middle scale)
Number of acquisitions: 10000 per channel

Mean : 1961
ADC_UNITS
with spread of 5 LSB



Internal 12bit ADC (2)



ADC linearity with external signal

Residuals < ± 1 LSB

Rms 0.3 LSB

Next steps

- Comparative measurements starting
  - Testboard arrived a few weeks ago in IHEP
  - First measurements started these last days
  - Complex chip => long measurements
- Collaboration will continue for PArISROC2
  - A few bugs to fix (ch13, low freq noise…)
  - Probable PM gain increase
  - reduce dead time for Water Cerenkov needs
  - Increase dynamic range with 2 gains 8 or 10 bits
- Chip being evaluated by several experiments : Megaton, DUSEL, LHASSO…
- Possible continuation in a large scale experiment

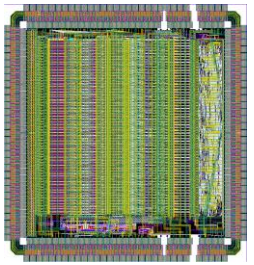
Conclusion

- Very fruitful collaboration on microelectronics between OMEGA-LAL Orsay and IHEP
- Good performance of common chip PArISROC
- Look forward to its application in common experiment
- We thank warmly Dr Wang Zheng and his group for their remarkable hospitality in China

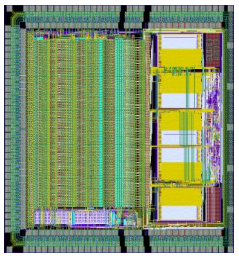
Backup slides

Orsay Micro-Electronics Groups Associated

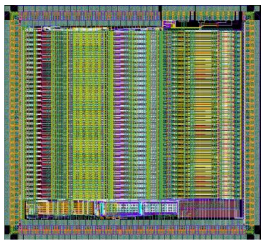
- A strong team of 10 ASIC designers…
  - = 20% of in2p3 designers
  - = 60% of department research engineers
  - A team with critical mass : pole created in 2007 = OMEGA
  - Expertise in low noise, low power high level of integration ASICs
  - 2 designers/ project
  - 2 projects/designer
  - Regular design meetings
- …Within an electronics departmt of 50
  - Support for tests, mesaurements, PCBs…
- A steady production
  - A strong on-going R&D
  - Building blocks SiGe 0.35µm



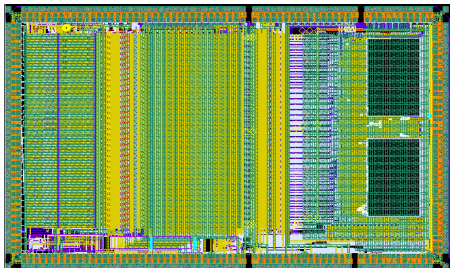
MAROC 2



HARDROC



SKIROC



SPIROC

Orsay micro-electronics team

- 8 research engineers (1 IR0, 2 IR1, 5 IR2)
- 1 phD student
- 1 visitor from China IHEP Beijing





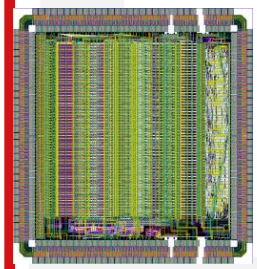
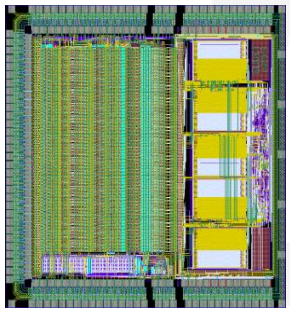
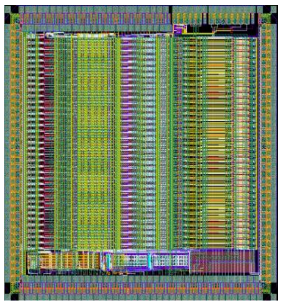
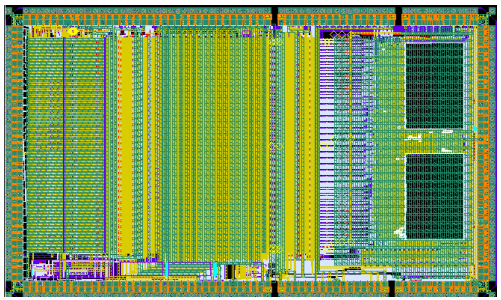
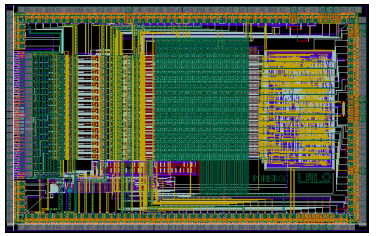




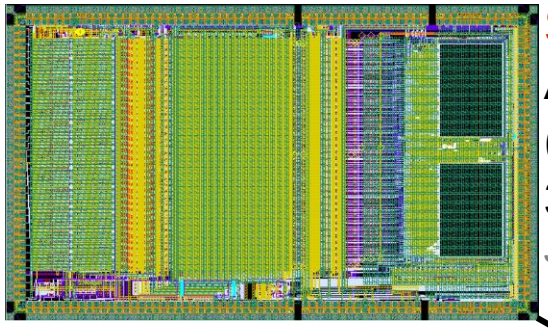

Recent chips

- Several chips developped for ATLAS LAr, OPERA, LHCb, CALICE in BiCMOS 0.8μm and installed on experiments
- Turn to Silicon Germanium 0.35 μm SiGe BiCMOS technology in 2005
- Readout for MaPMT and ILC calorimeters
- Very high level of integration : System on Chip (SoC)
- Parallel activity of building blocks

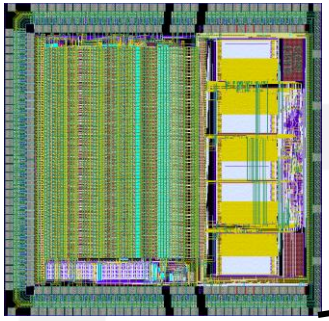
MAROC 2 **HARDROC** **SKIROC** **SPIROC**

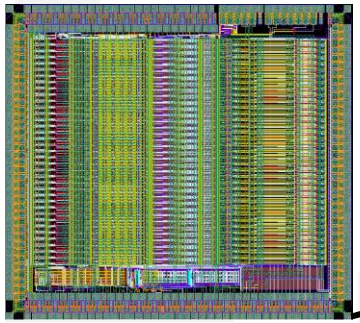
The front-end ASICs : the ROC chips



SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

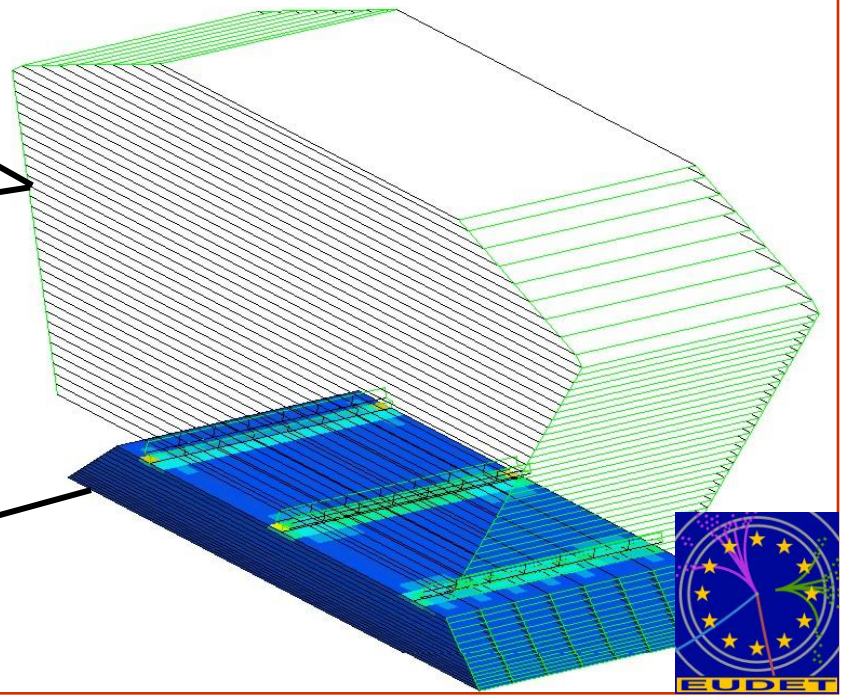


HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06



SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06

- Technological prototypes : full scale modules (~2m)
- EUDET EU funding (06-09)
- ECAL, AHCAL, DHCAL
- B=5T



SPIROC used in SKIROC mode