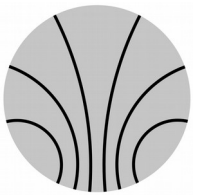
Calorimetry systems for the ILC

Outline

- Calorimetry at a future linear collider
- CALICE Analog Hadronic Calorimeter
- Active Elements – Silicon Photomultipliers & Scintillating tiles
- Electronics development

Konrad Briggl, KIP
HighRR seminar
28.10.15



ILC: The international linear collider

Future e^--e^+ accelerator, sqrt(s) up to 500 GeV (Possible upgrade to 1TeV)

31km length in 500GeV baseline design

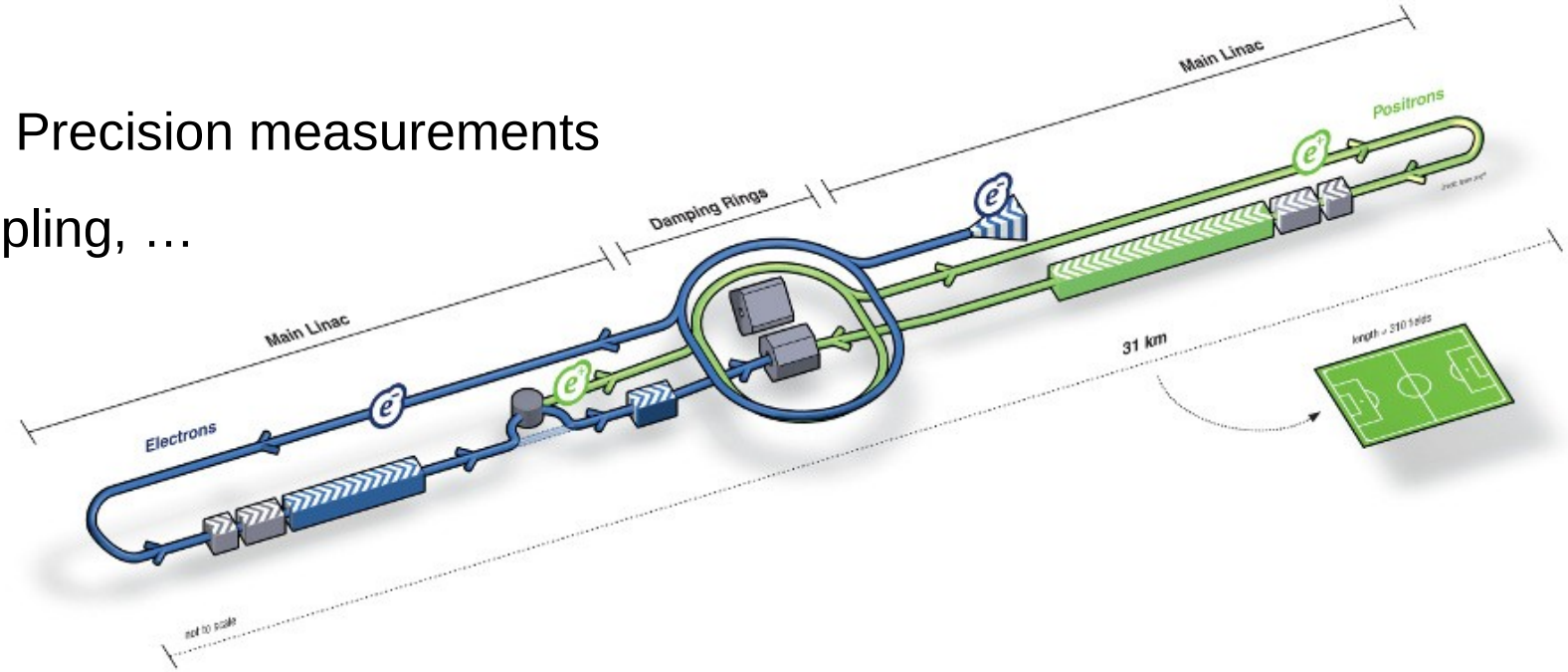
Mature machine technology

Two interchangeable Detectors:

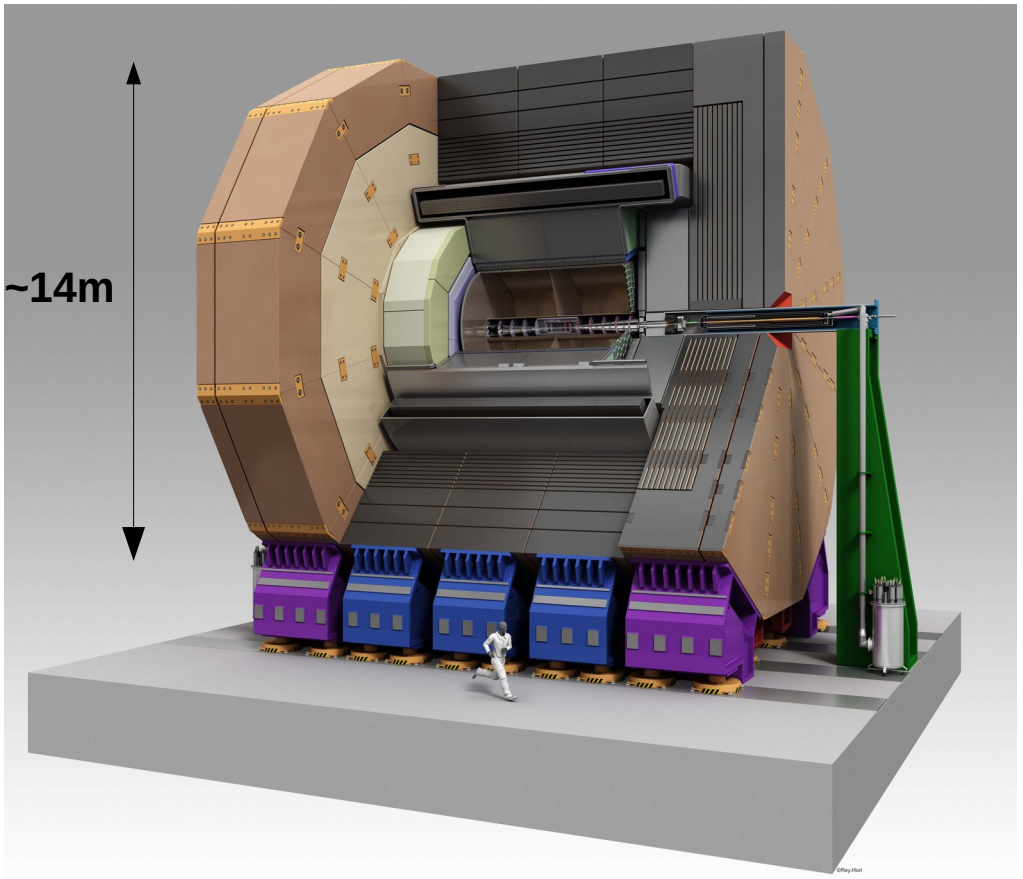
ILD & SID

Physics goals: Precision measurements

e.g. Higgs coupling, …



ILD - International Large Detector



Tracking:

Pixel Detectors (CMOS/CCD/DEPFET)

TPC (Micromegas / GEM)

Calorimetry

Si / Scintillator+SiPM (ECAL)

RPC / Scintillator+SiPM (HCAL)

Muon system

RPC / Scintillator+SiPM

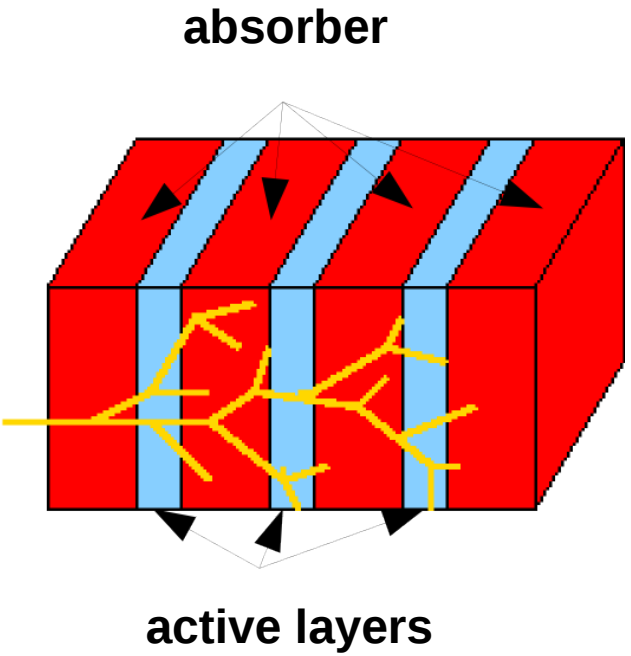
Calorimetry in HEP

Most common structure:

Sampling Calorimeter

Dense absorber (e.g. steel, tungsten, …)
Cost optimization: material volume ↔ magnet size
Active medium (e.g. scintillator, RPC, LAr)

Energy measurement by “counting” of tracks in shower



Calorimetry for ILC experiments

CALICE collaboration

Calorimetry for a future linear collider experiment. Includes SiD, CLIC

Seeking energy resolution:

$\sigma(E_{jet})/E_{jet} \approx$ 3-4% for E_{jet}= 40 – 500 GeV

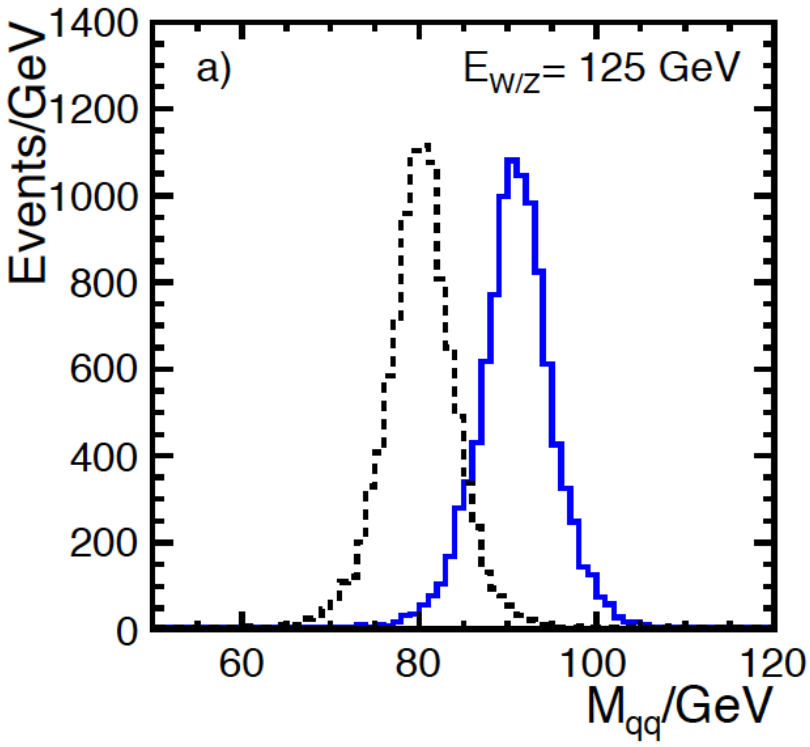
Differentiate decays W → jj ,Z → jj from mass reconstruction

Typical hadronic calorimeter:

$\sigma(E_{jet})/E_{jet} \approx 60\%/\sqrt{E[GeV]} + 2\%$

→ 10% for E_{jet} = 50GeV

ILD approach: **Particle flow algorithms**



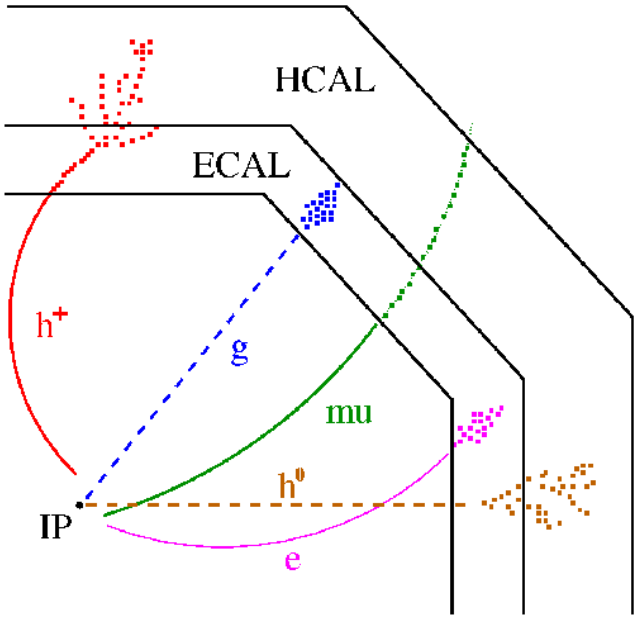
Calorimetry for ILC experiments

Particle flow algorithms

Use sub-detector with highest resolution:

Charged particles	→ Tracking
e, γ	→ ECAL
n, K	→ HCAL

<u>Ideally:</u> Only measure energy of neutrals in HCAL



Calorimetry for ILC experiments

Particle flow algorithms

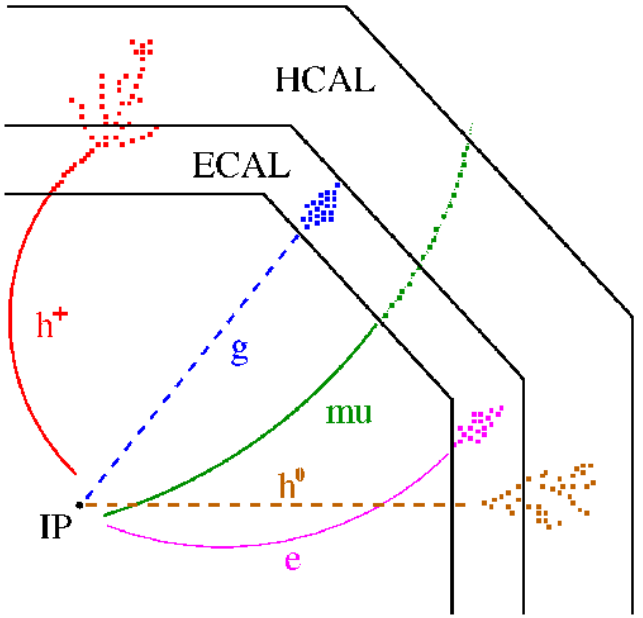
Use sub-detector with highest resolution:

Charged particles	→ Tracking	~60 %
e, γ	→ ECAL	~30 %
n, K	→ HCAL	~10 %

typical jet

Ideally: Only measure energy of neutrals in HCAL

10 % neutrals in typical jet



Calorimeters for Particle Flow

Particle flow algorithms

Use sub-detector with highest resolution:

Charged particles	→ Tracking	~60 %
e, γ	→ ECAL	~30 %
n, K	→ HCAL	~10 %

typical jet

$\sigma_X \sim 0$

$\sigma_\gamma \sim 6\% / \sqrt{Ej}$

$\sigma_{had} \sim 16\% / \sqrt{Ej}$

Ejj contributions

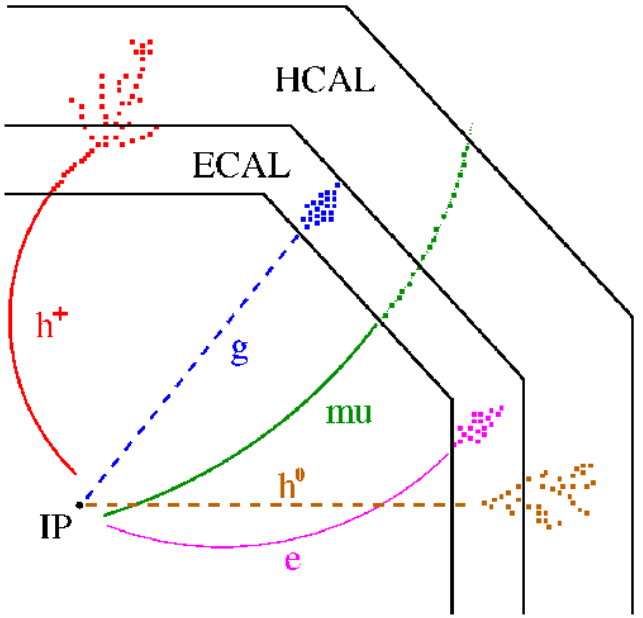
Ideally: Only measure energy of neutrals in HCAL

10 % neutrals in typical jet

… still 16%/√E contribution from neutral Hadrons

… still need a good calorimeter!

$$\sigma^2_{jet} = \sigma^2_X + \sigma^2_\gamma + \sigma^2_{had} + \sigma^2_{loss} + \sigma^2_{conf}$$



Calorimeters for Particle Flow

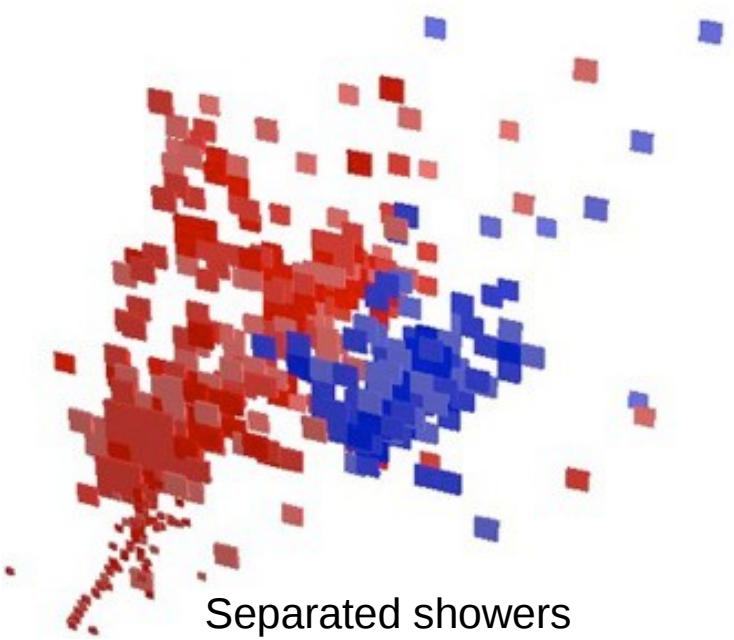
Higher energies: Confusion term dominates

$$\sigma^2_{jet} = \sigma^2_X + \sigma^2_Y + \sigma^2_{had} + \sigma^2_{loss} + \boldsymbol{\sigma^2_{conf}}$$

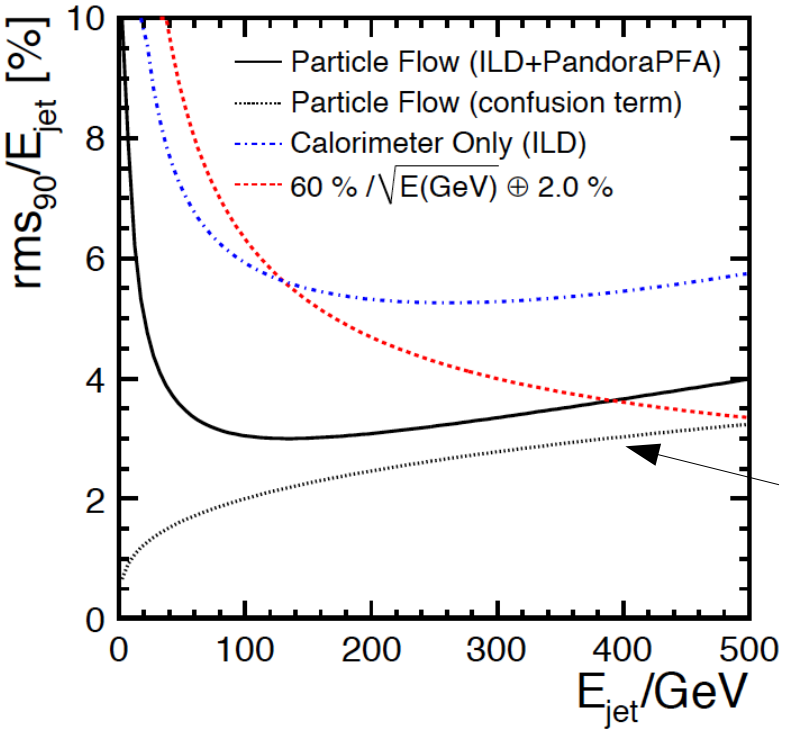
Wrong association of tracks ↔ showers

→ Good Tracking

→ Good shower separation



Separated showers
(distance 8cm)



ILD calorimeter

Particle flow Algorithms

Classical calorimeter

Confusion term

Calorimeters for Particle Flow

Parameters for energy resolution

→ electromagnetic performance

→ hadronic performance

→ shower separation

Requires precise modeling of shower structure

Detector optimization

→ **High Granularity**

“Imaging Calorimeters”

Calorimeters for Particle Flow

High Granularity

"Imaging Calorimeters"

Different concepts:

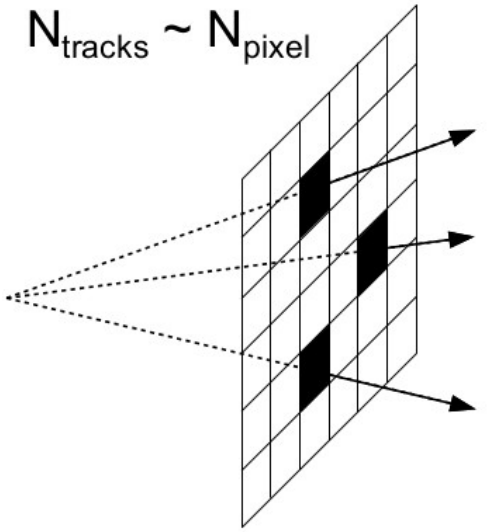
Cell size vs. Quantization resolution

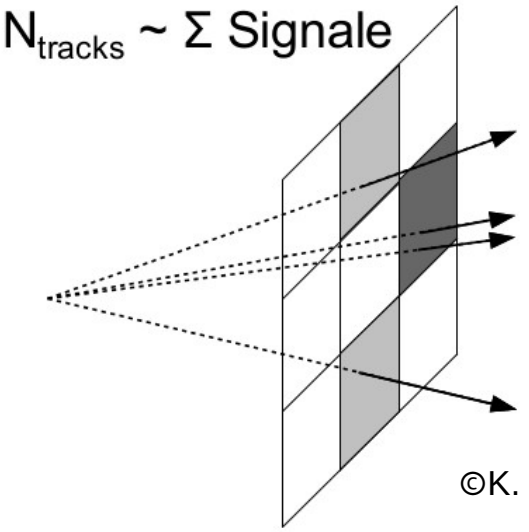
→ Digital / Semi-digital HCAL

1 or 2bit per cell, ~1cm²

→ Analog HCAL

10-12 bit per cell, ~10cm²

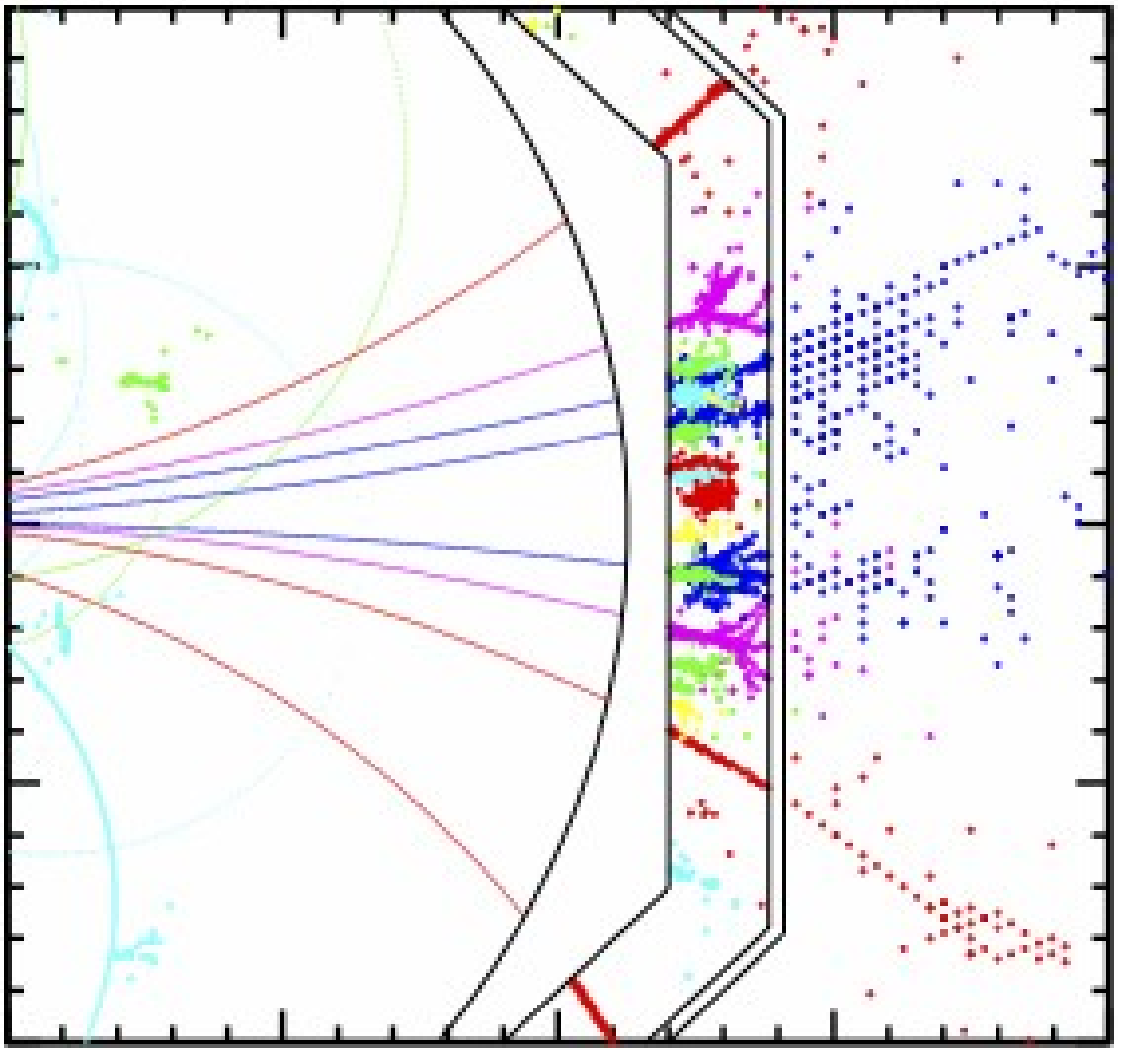




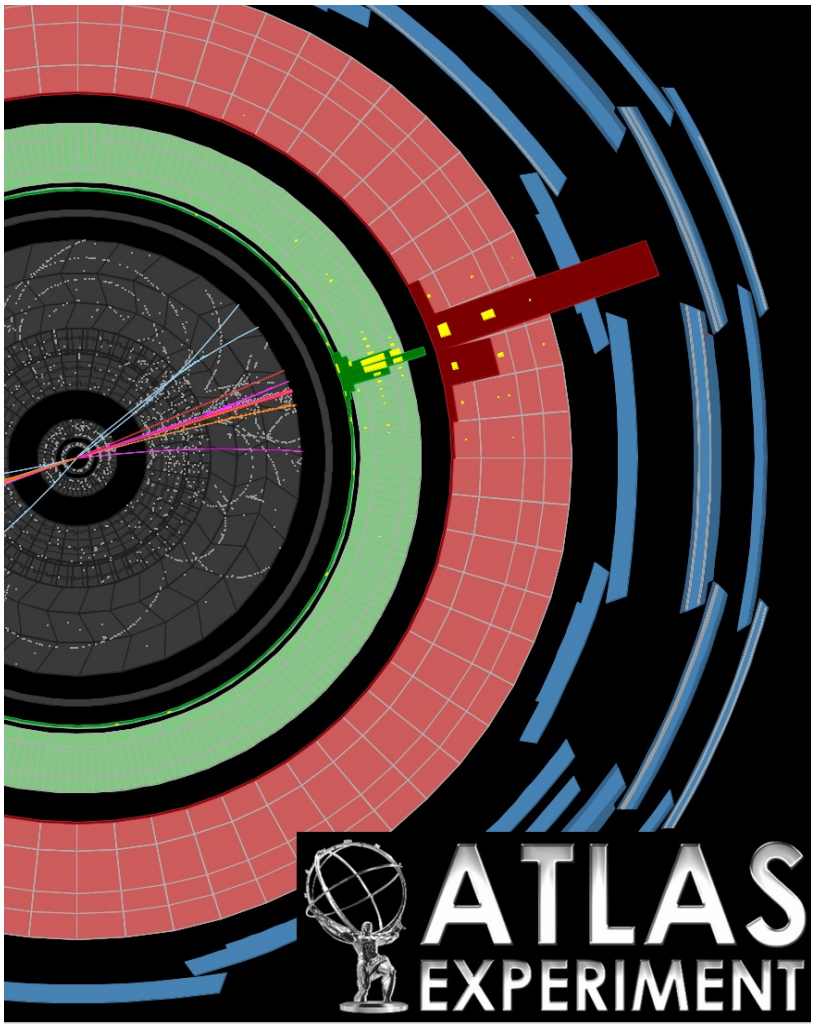
©K. Krüger

High granularity?

ILD simulation of a 100GeV jet [arXiv:0907.3577v1]



Atlas ~300GeV dijet event

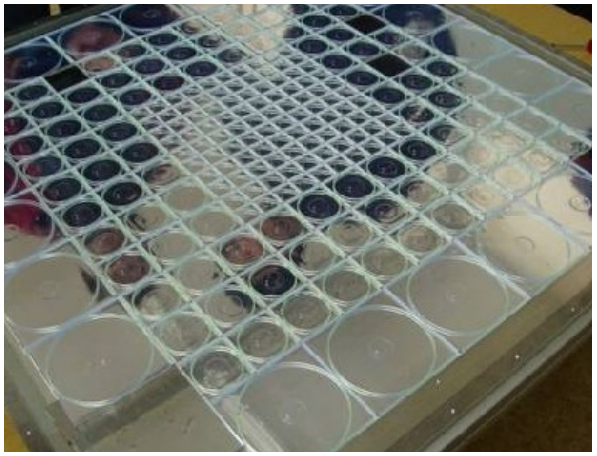


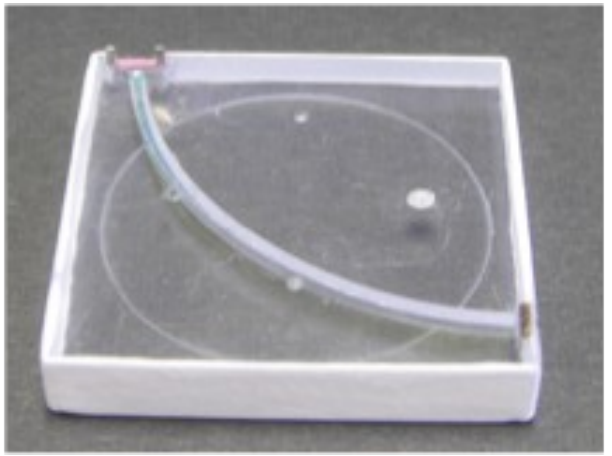
CALICE AHCAL

- **A**nalog **H**adronic **Cal**orimeter concept
- Scintillator based sampling calorimeter,

  tiles of 3x3cm²
- Individual SiPM readout per cell
- 1m³ physics prototype operated 2006 – 2012
- Intensive performance studies:

  EM&Hadronic showers, Imaging capabilities

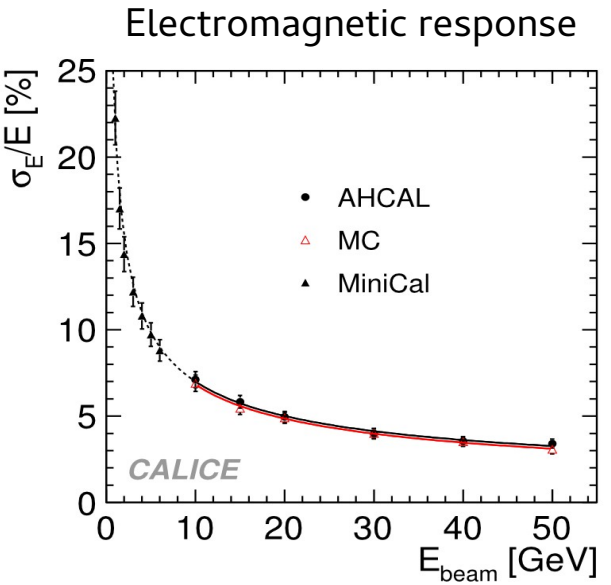




Performance of the physics prototype

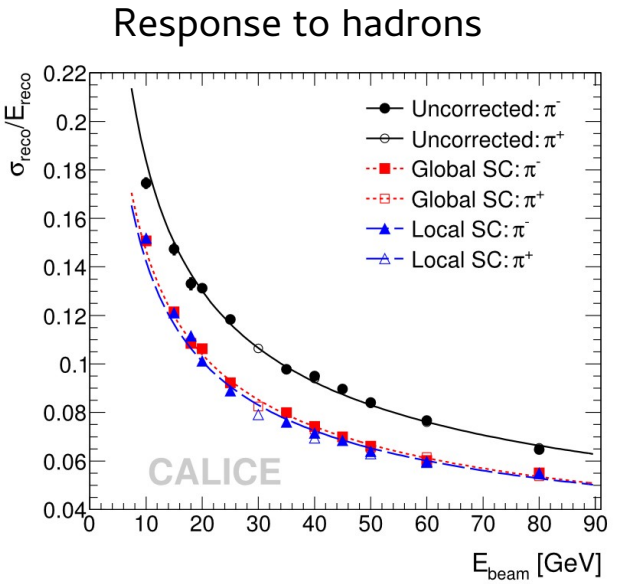
Energy resolution validated, e.g.

- Electromagnetic showers
- Hadrons



JINST 6 P04003 (2011)

Fit: 45%/√E + 1%
(using Software compensation)



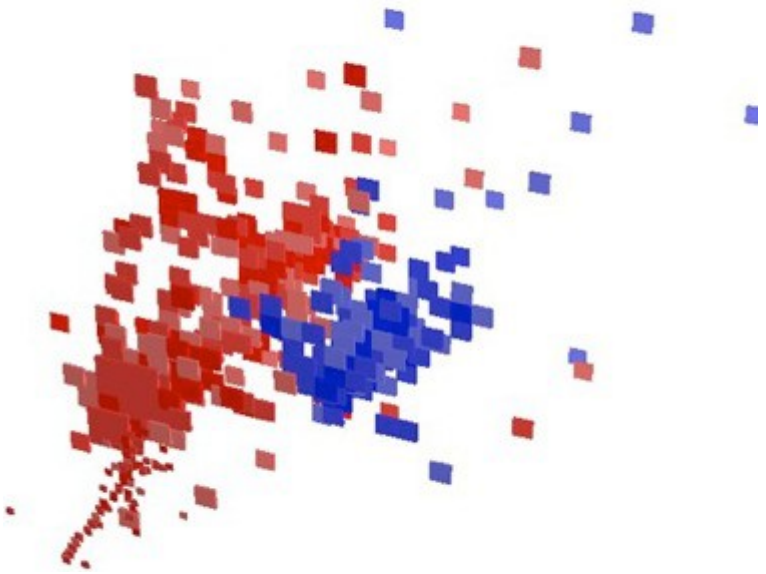
JINST 7 P09017 (2012)

Performance of the physics prototype

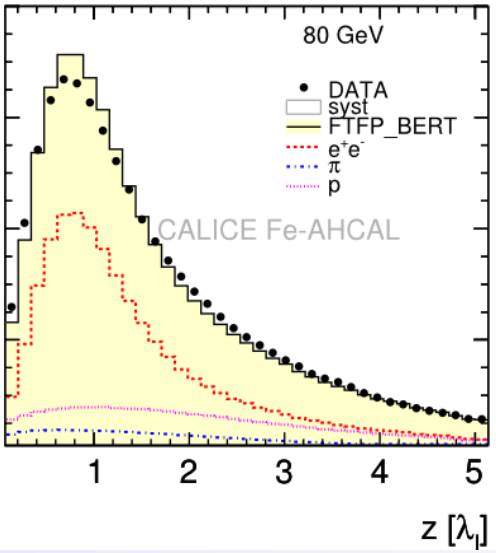
Validation of PFA capabilities and monte carlo shower models

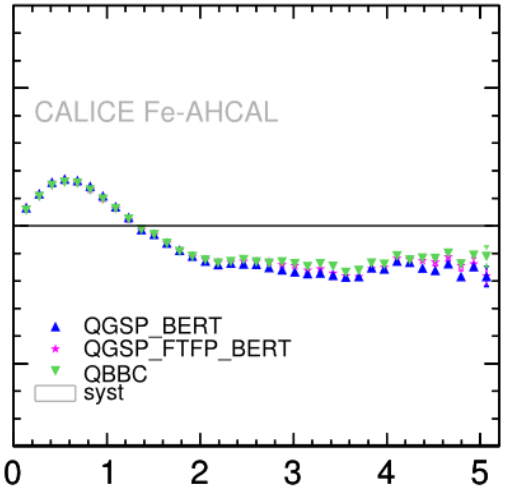
- Shower separation
- GEANT4 shower model validation

Imaging validation & performance
JINST 6 P07005 (2011)

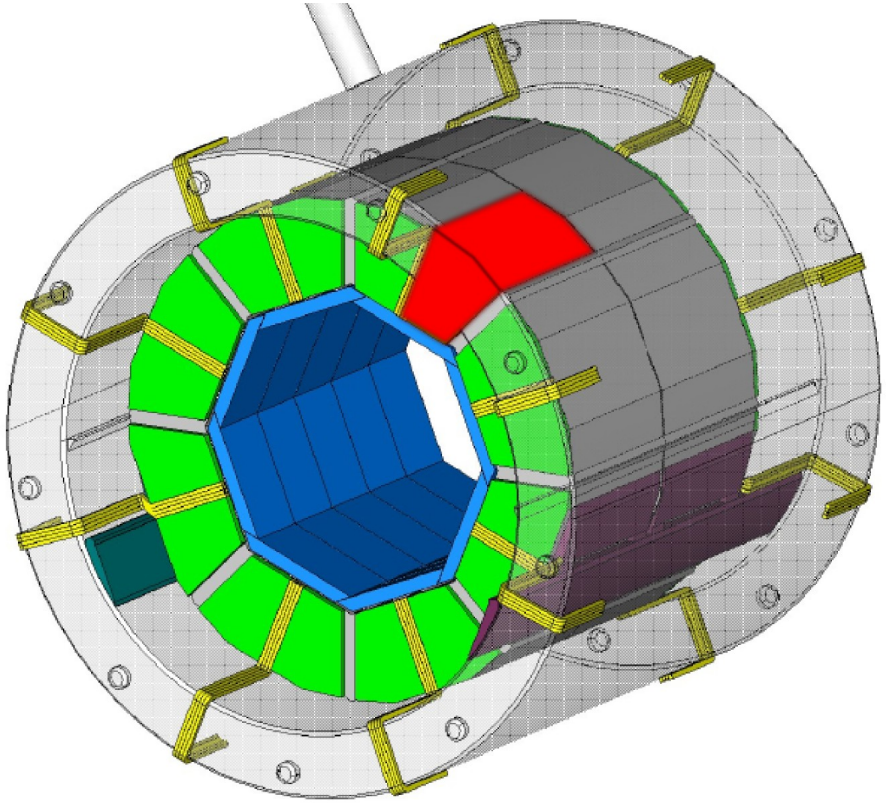


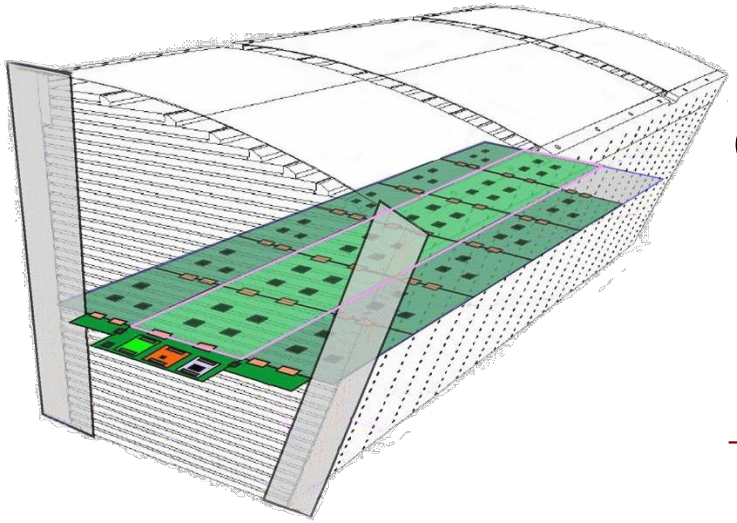
Validation of GEANT4 shower models
JINST 8 P07005 (2013)





Heading to a scalable system - Engineering prototype





Goal:

Develop part of full calorimeter that could be scaled to full size

Challenges:

Scalability:

10 000 channels in physics prototype

8 000 000 channels in ILD detector

→ *Tile R&D for scalability*

Compactness:

High integration level

No active cooling

→ *Destinct readout electronics, DAQ and calibration system*

Active Elements – Scintillating Tiles

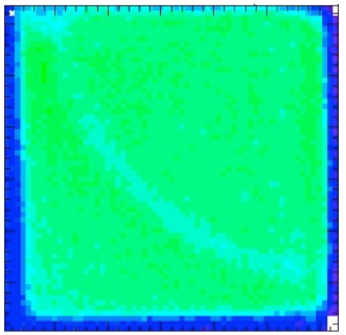
Parameters for tile R&D

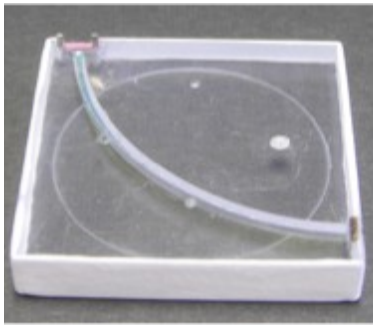
- Light yield, Signal-to-noise ratio
- Response uniformity
- Cell to cell crosstalk

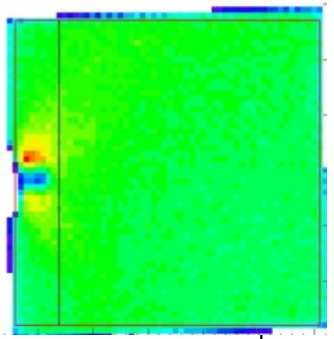
Scalable prototypes:

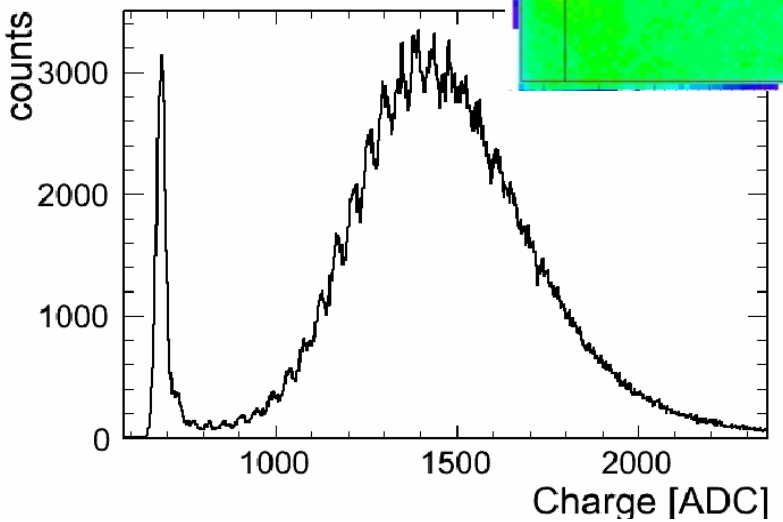
- Possibility of mass production
- cost …
- → *Simplification of tile design*

Uniformity scans
using Sr90 source









Tile B) response to
β source

Active Elements – Scintillating Tiles

<u>Mass production & testing possibility becomes important</u>

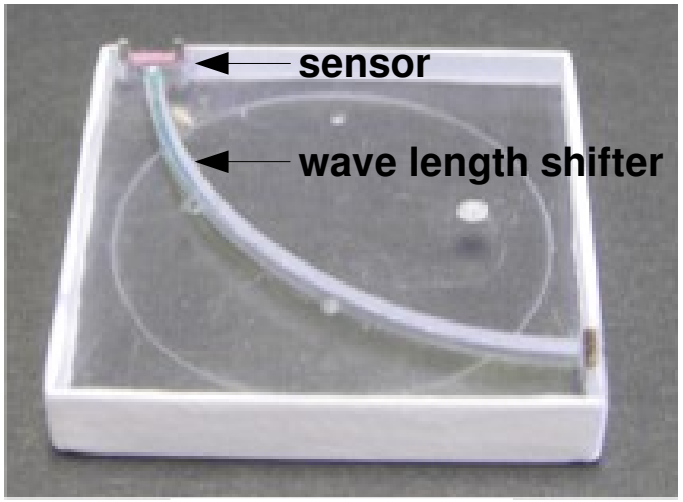
Simplifictation of tile production:

Availability of Blue & nUV sensitive sensors → Fiberless coupling

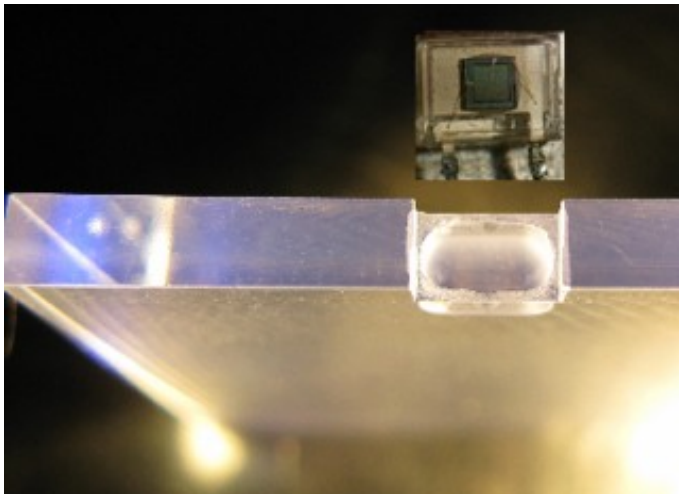
Improved yield & Quality of sensors → SMD mounting of sensors

Cost, Time per tile: Production, Testing, Mounting, … 1s / tile

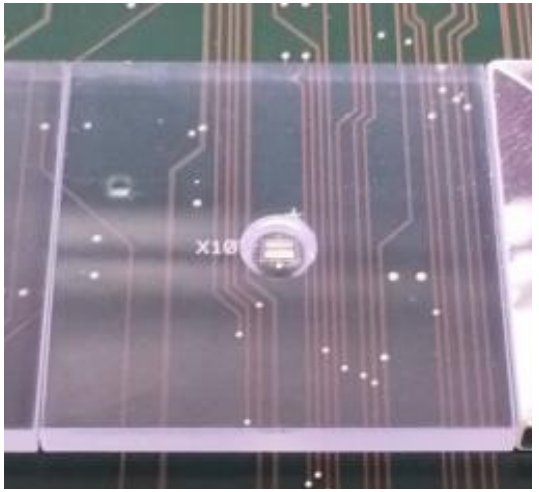
→ Dedicated work on Mass Characterization & Assembly



Physics prototype



Concepts for fiberless coupling



SMD mounted SiPMs

Active elements – Silicon Photomultipliers

Read-out of scintillation light - O(10) detected photons

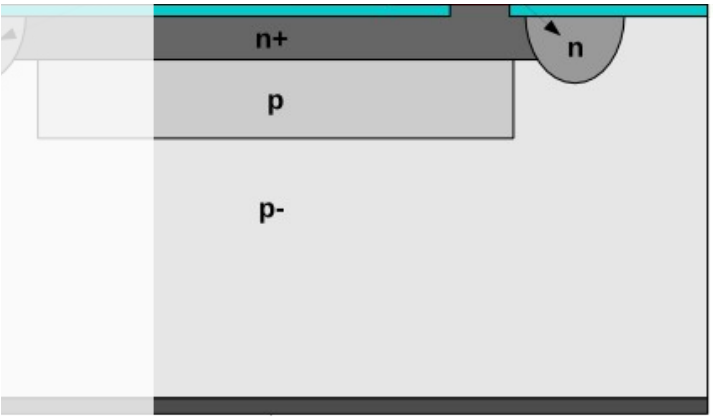
Normal Photomultipliers: Large, B-Field sensitive

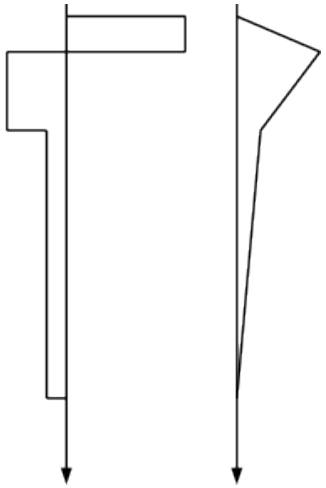
Compact semiconductor devices:

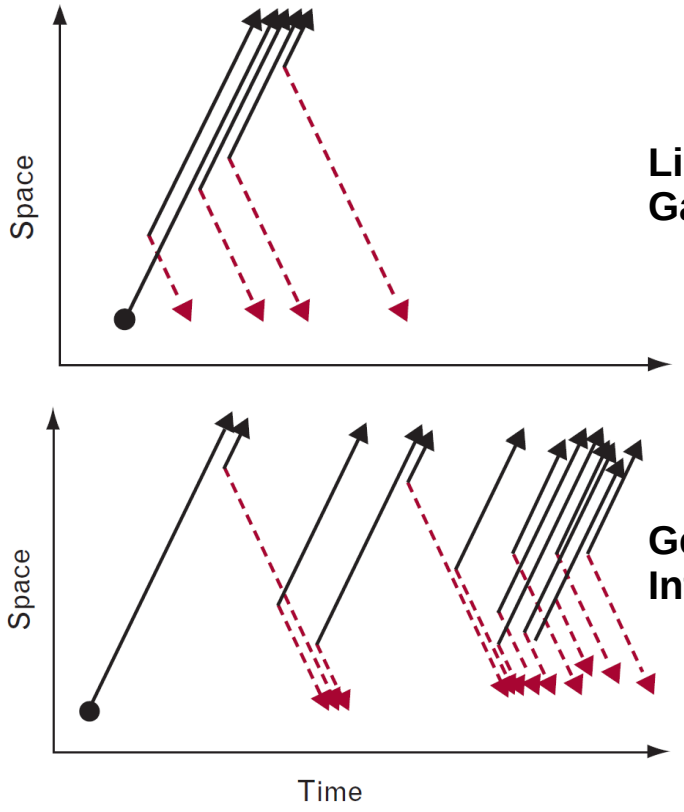
Silicon Photomultipliers

Key component:

Avalanche photo diode







Bias voltage

Drift: Gain = 1

Linear region: Gain O(10^5)

Geiger region: Infinite Gain

APD: Doping concentration & Field

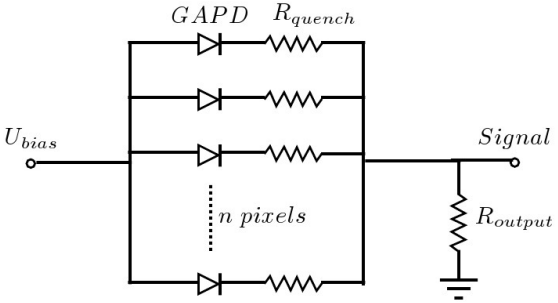
Active elements – Silicon Photomultipliers

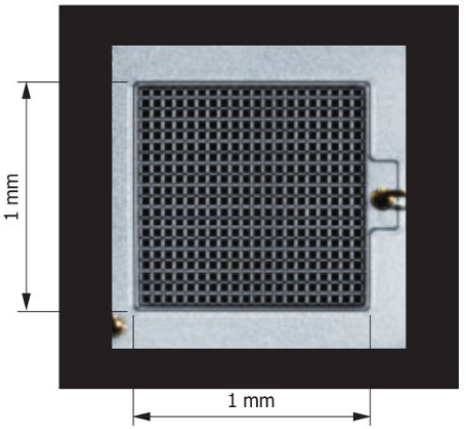
Silicon Photomultipliers

Parallel connected APDs in geiger mode

Avalanche Quenching resistor

→ APD pixels are 'binary devices'



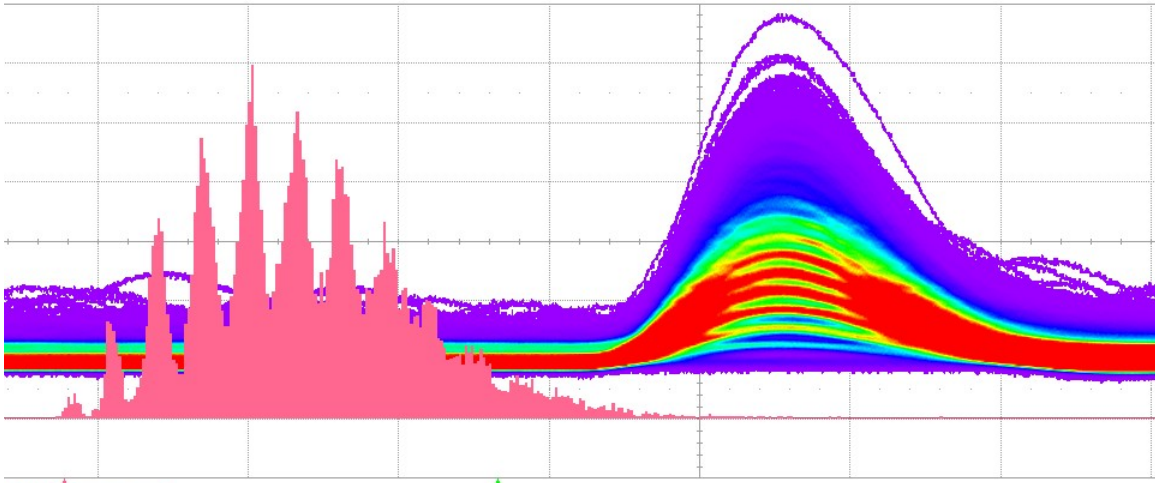


$$Q = N_{px} * C_{px} (U - U_{br})$$

fired pixels — single pixel gain

~ Incident photons

~ Traversing particles



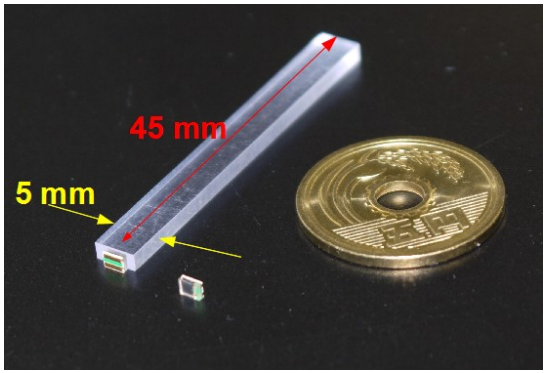
Scintillator ECAL option

Even higher granularity than HCAL

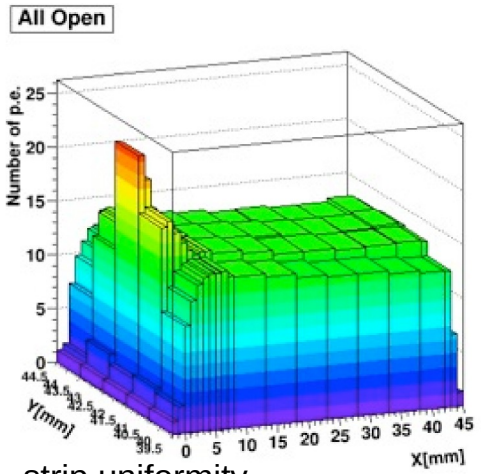
- Segmentation: 1cm²
- One option: Scintillating strips & SiPM readout

Similar scintillator optimizations as for AHCAL

- Large dynamic range
- → Large pixel count SiPMs (10k pixels/mm² – low gain)



SCECAL: scintillator strips



strip uniformity


Layer for engineering prototype

Readout electronics for CALICE

Measurements

Shower timing [<1ns]

Energy measurement:

Small signals (SiPM gain calibration)

[Charge ~15fC … 2pC]

Large signals (MIP counting)

[Charge up to 150pC]

High integration level

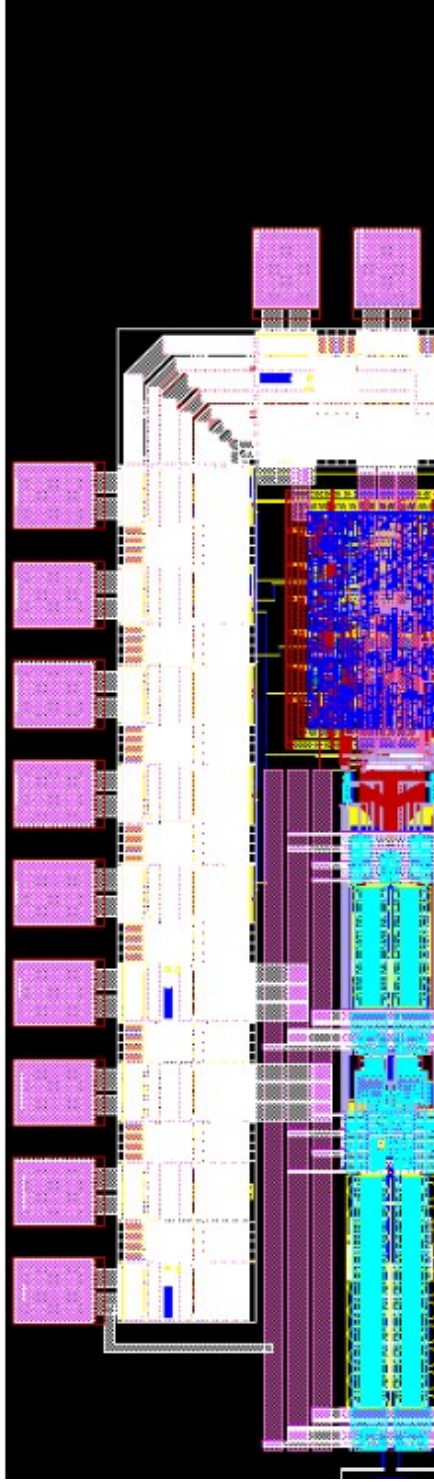
Fully integrated readout electronics

No active cooling → Low power

Self-triggered operation

SiPM gain adjustment

→ Requires a versatile chip



Readout electronics for CALICE

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[Charge up to 150pC]

High integration level

Fully integrated readout electronics →

SiPM gain adjustment

No active cooling → Low power

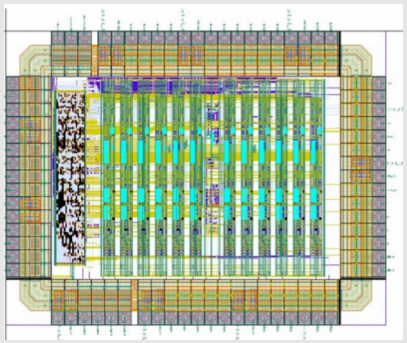
Development of Mixed signal ASICs

- Analog Front-end
- Integrated ADC, TDC
- Digital readout

Baseline solution:
SPIROC, designed by French group

Development for low gain SiPMs:
KLauS ASIC (KIP)

SPIROC2b, Omega/F



KLauS2, KIP

Readout electronics for CALICE

Measurements

Shower timing [<1ns]

Energy measurement:

Small signals (SiPM gain calibration)

[Charge ~15fC … 2pC]

Large signals (MIP counting)

[Charge up to 150pC]

High integration level

Fully integrated readout electronics

SiPM gain adjustment →

No active cooling → Low power

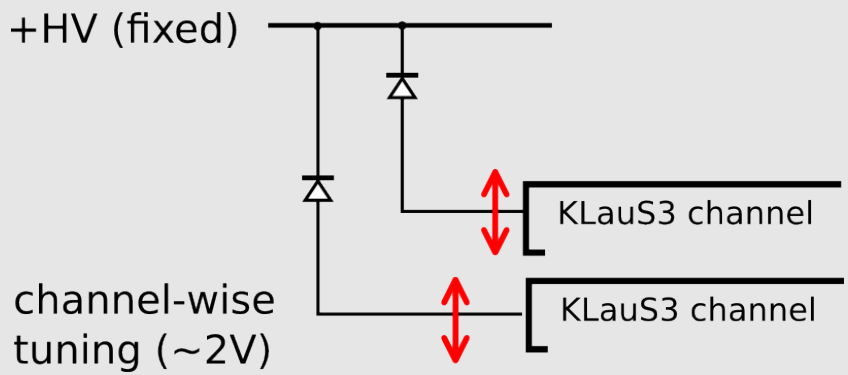
Temperature & SiPM parameter fluctuations

Gain adjustments per channel

Large number of channels

-One HV source per layer (~2500 channels)

-Small tuning range for each SiPM (~2V)



Readout electronics for CALICE

Measurements

Shower timing [<1ns]

Energy measurement:

Small signals (SiPM gain calibration)

[Charge ~15fC … 2pC]

Large signals (MIP counting)

[Charge up to 150pC]

High integration level

Fully integrated readout electronics

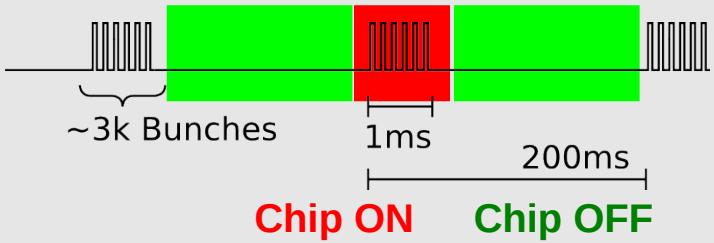
SiPM gain adjustment

No active cooling → Low power

Low power consumption

- Constraint: ~25uW / channel

Met by:
- Intrinsic low power design
- Power gating (1% duty cycle)



Main constraint in design!

Readout electronics for CALICE

Development of 'KLauS'

Analog front-end,

ADC for digitization,

digital parts …

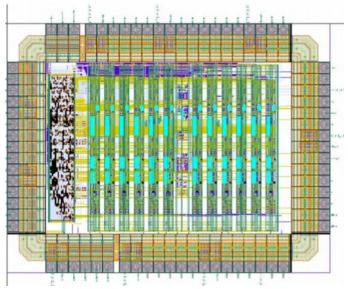
→ *Multi channel ASIC planned for 2016*

All blocks optimized for

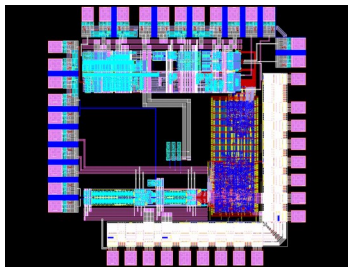
Low power consumption (Power pulsing capable)

Different requirements for Calibration [small signals, low noise]

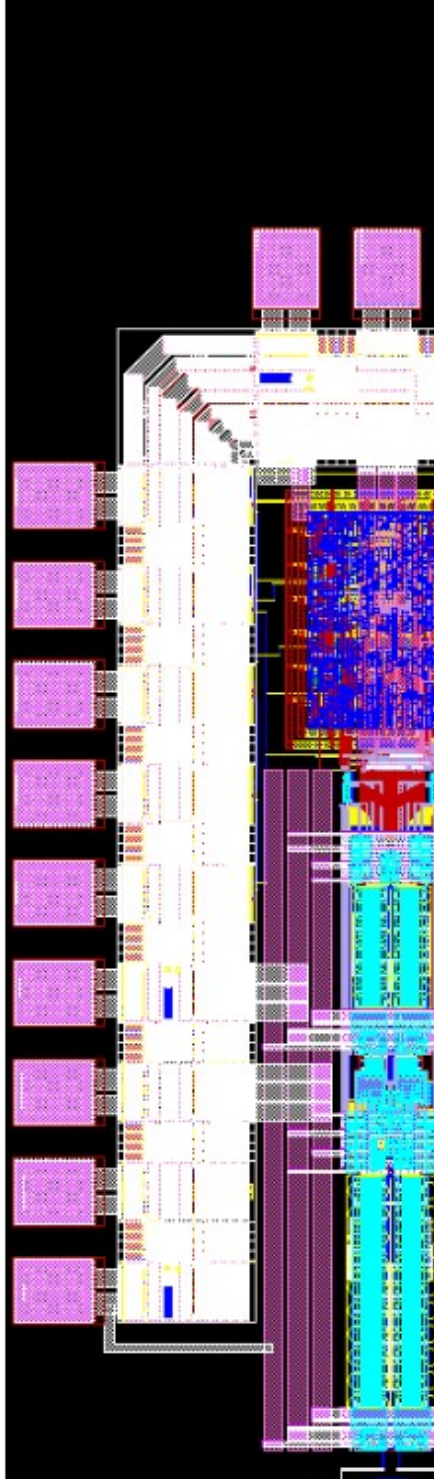
and 'Physics' [Large dynamic range]



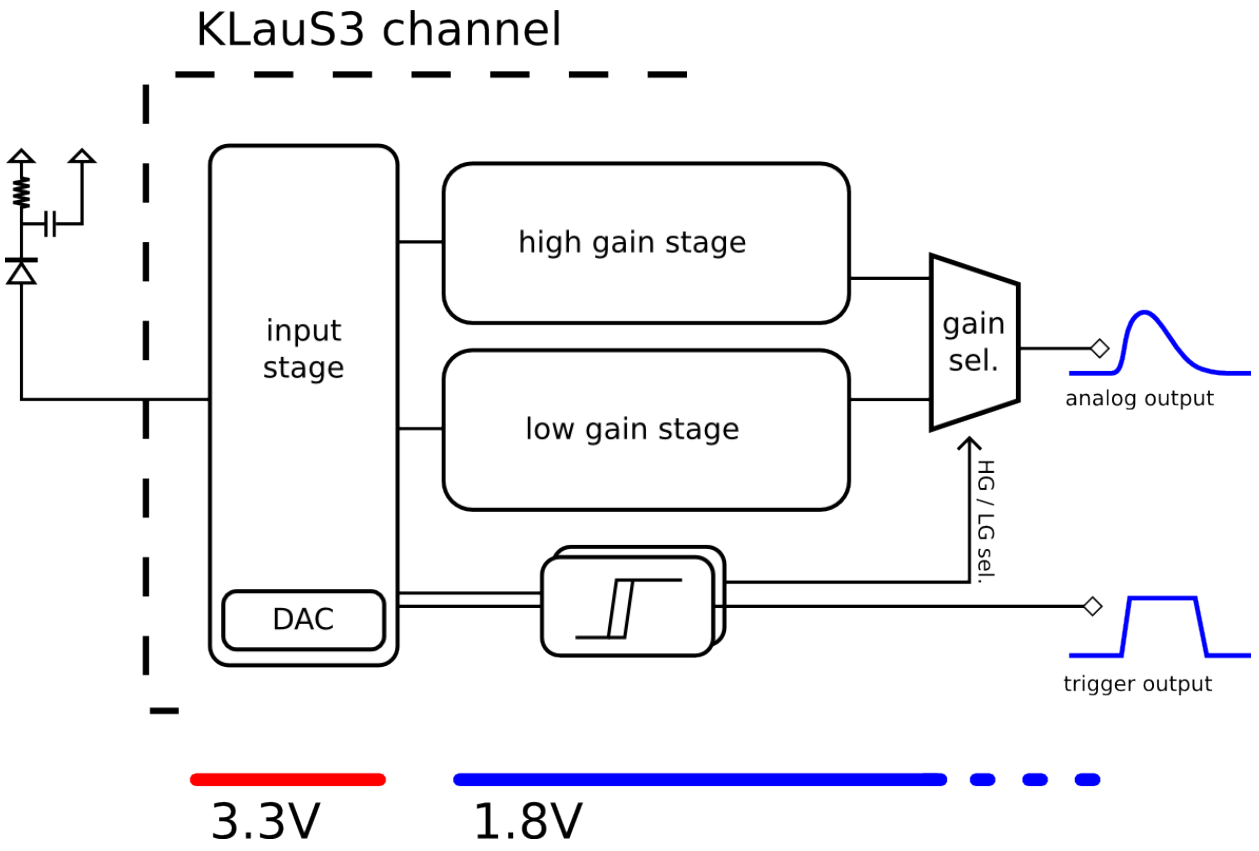
[KLauS2.0 – analog only]



[KLauS3.0 – frontend & ADC]



KLauS3 front-end: Blocks



Input stage:
- Low input impedance
- SiPM bias voltage DAC

High gain stage:
- Single pixel spectra
- O(10ths of pixels)
- Low noise

Low gain stage:
- Full SiPM dynamic range

2 Trigger branches

Minimize power consumption
- Power gating
- Dual supply scheme

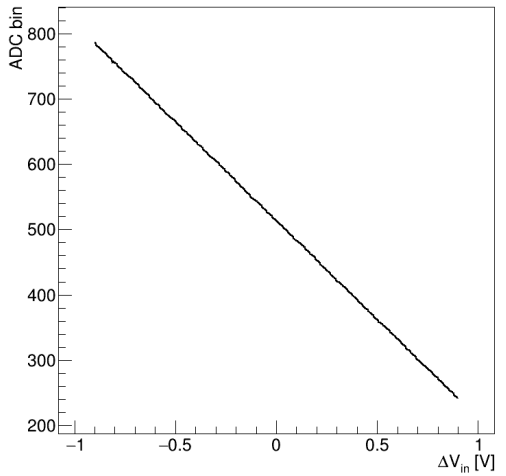
ADC for KLauS

1 ADC per front-end channel
→ Development of low power ADC

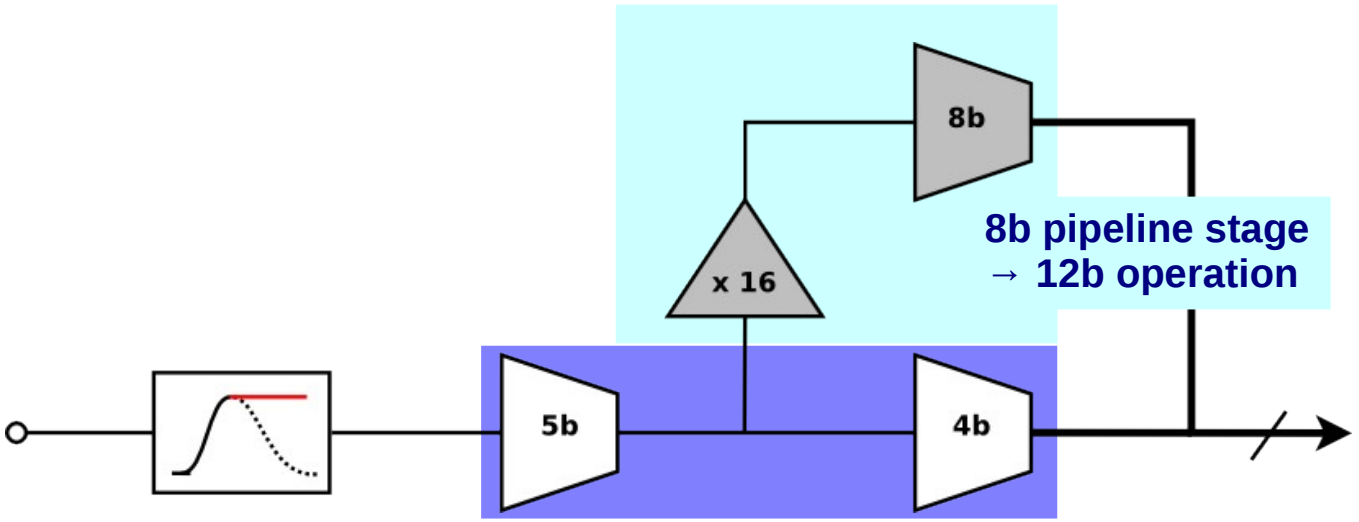
Two operation modes:

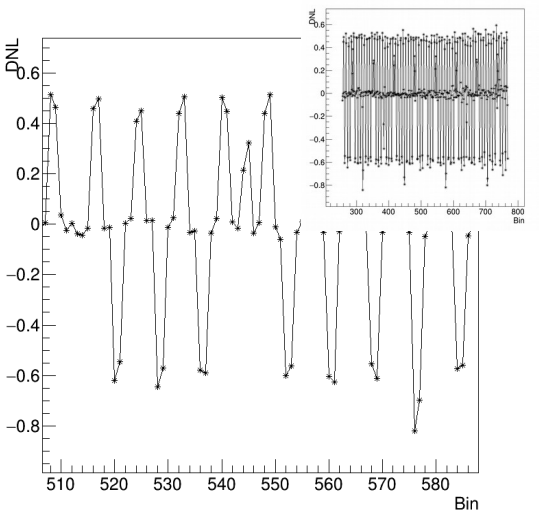
SiPM gain calibration – 12bit resolution
MIP quantization – 10bit resolution

Maximum Event rate: 3MHz



[10b ADC Linearity]





[10b ADC DNL - Preliminary]

Summary

The CALICE collaboration is developing **calorimeters for a future linear collider**

Detector optimization for Particle flow algorithms

- High Granularity
- AHCAL concept: SiPM + Scintillator based hadronic calorimeter

Scalable prototype

- New challenges for active elements:

  Stronger focus on scalability of production,

  testing and assembly
- Development of readout electronics

  Fully integrated

  Very low power consumption

- Backup -

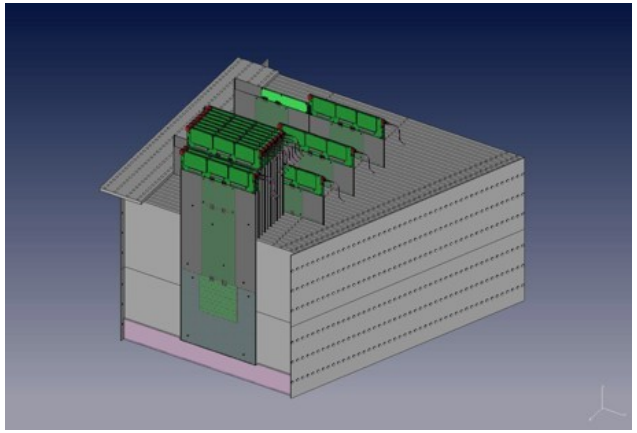
CALICE AHCAL Contributors

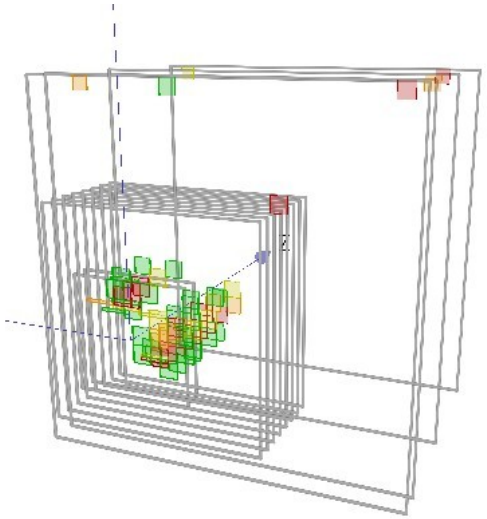
Engineering prototype – Current state

Testbeam 2015 at CERN SPS

- Steel stack
- 2x ECAL layers
- 8x 30x30cm HCAL layers
- 4x 60x60cm HCAL layers

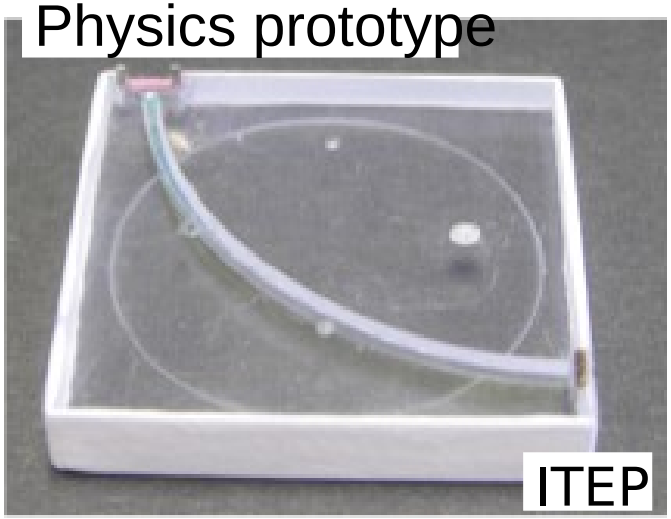
- Pions runs
- Muons





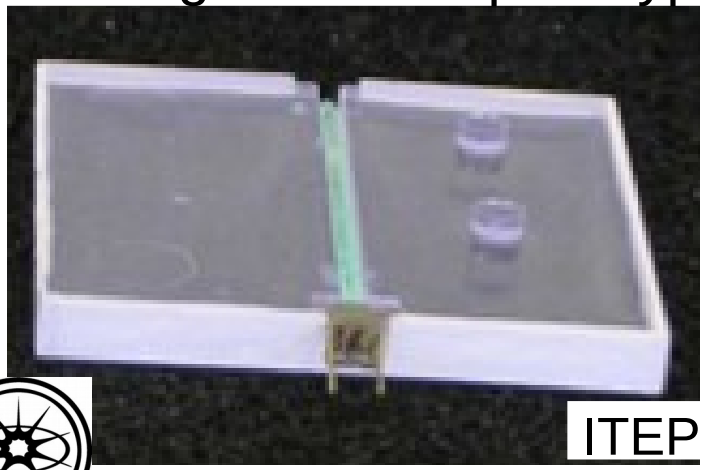
Evolution of tile designs

Physics prototype

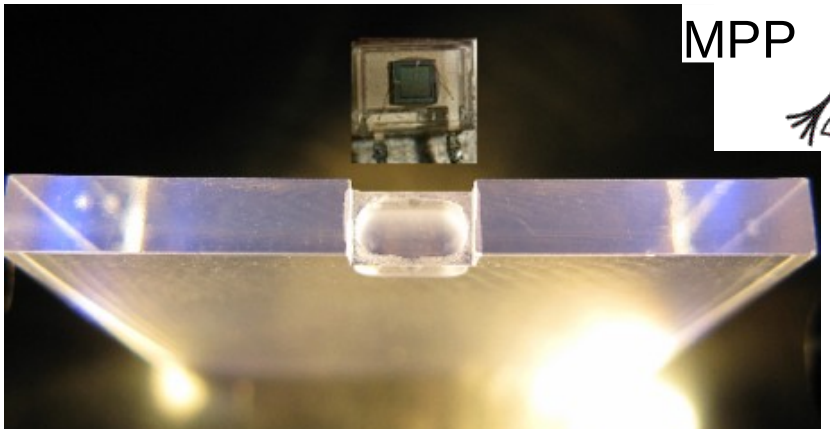


Simplified assembly
Mechanical alignment

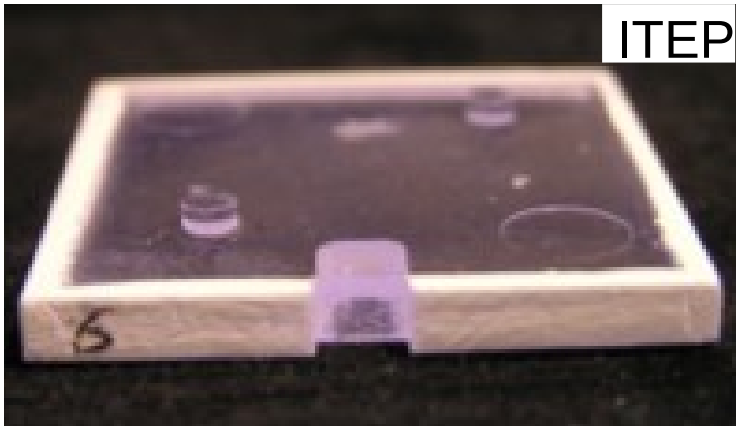
1st design for tech. prototype



Fiber-less coupling,
Tighter tolerances



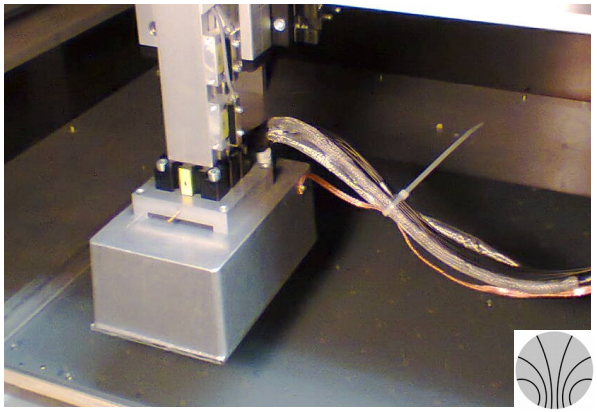
Fiber-less coupling,
Injection molding



After the tile production...

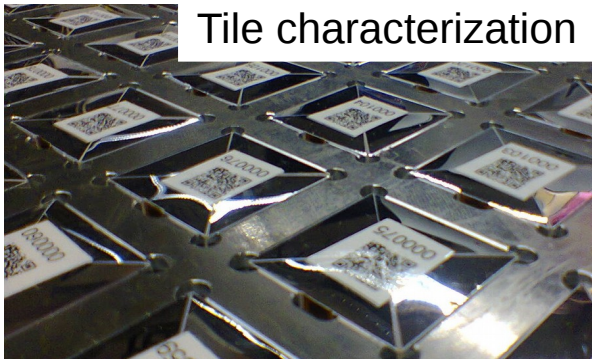
Quality assurance

- SiPM functionality test
- Tile characterization

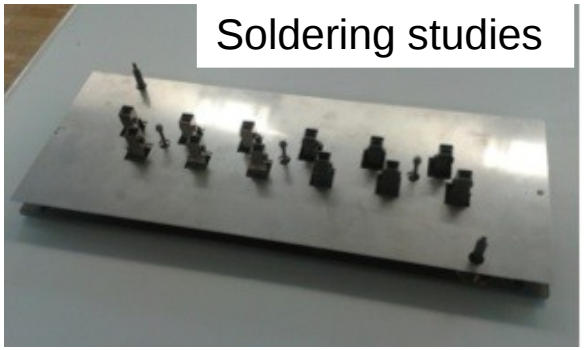


Assembly in larger modules:

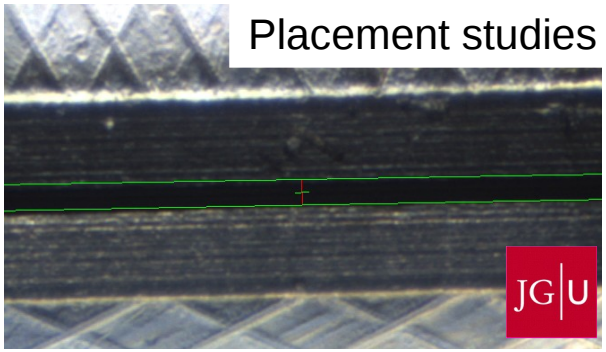
- Precise tile placement
- Soldering



Tile characterization

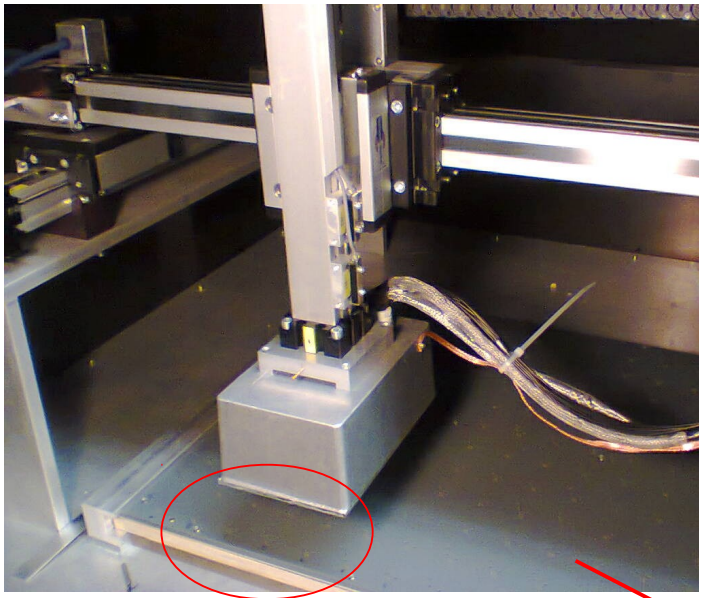


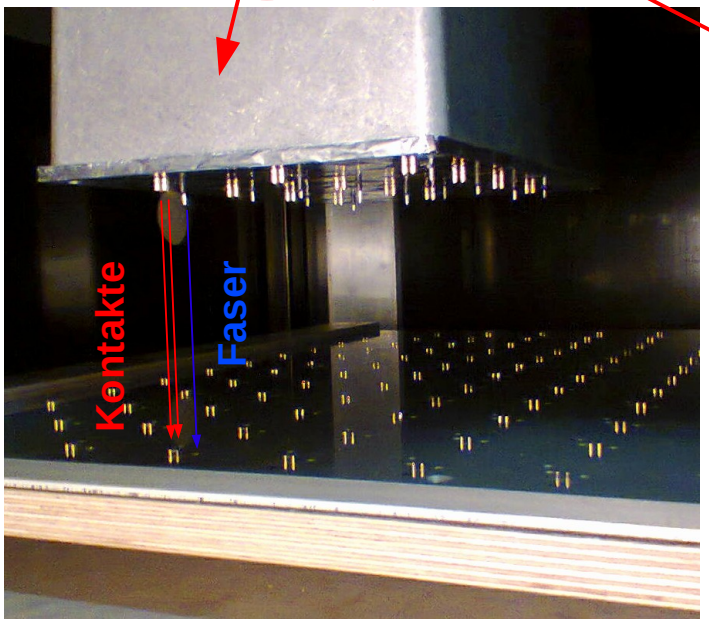
Soldering studies



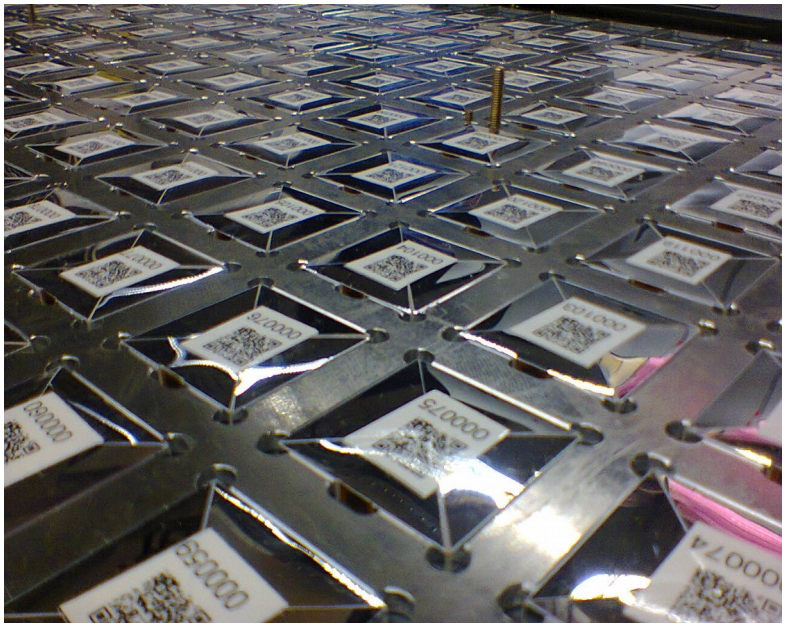
Placement studies

Automated characterization of Tiles

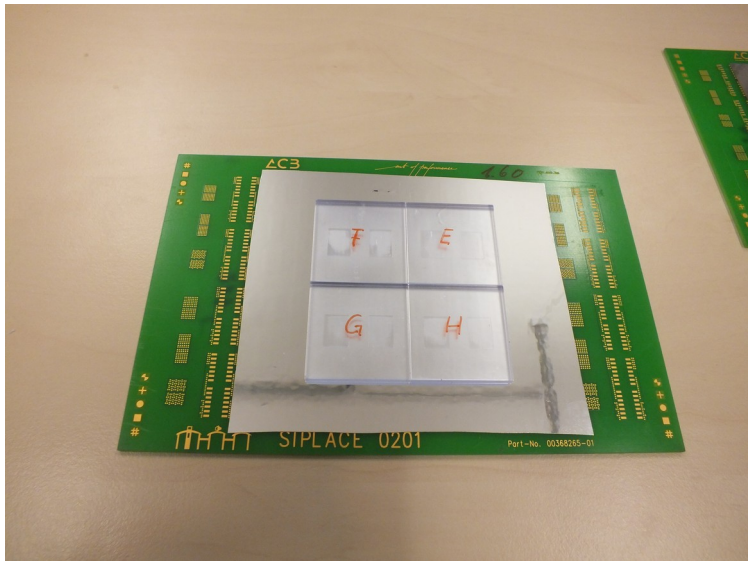




- Fast measurement → Only basic parameters measured
- Parallelization (12 channels)
- UV Laser instead of source
- Currently 2min for 12 tiles, then repositioning
- Automatic electronic and optical connection
- ≈ 1500 tiles characterized for testbeam prototypes

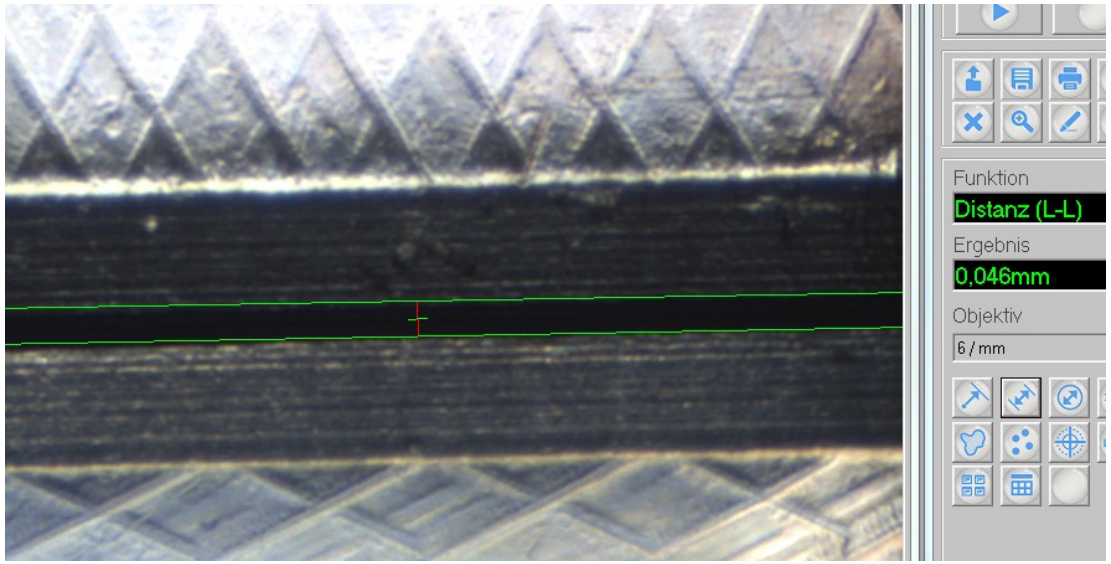


Automated assembly of HBUs



- Large number of components require automatic Placement and soldering of Tiles to HBU
- Precise & fast placement
- Fast gluing procedure

→ Possibility to place tiles without mechanical alignment



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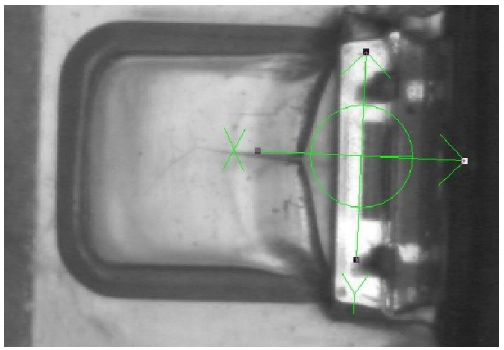
Automated assembly of HBUs



Melted tile dimple after first soldering tests

Multi point head for selective soldering

- Different options for soldering technology
- Challenge: Soldering of (very) heat sensitive components
- Automation poses additional requirements on PCB design
- Wave soldering:
  - Heat protecting mask to avoid heating up other components
- Selective soldering
  - Slower, possible speed up by multi point head

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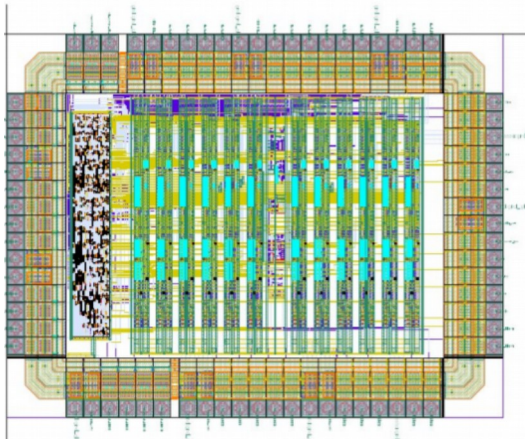
KLauS Development status & Plans



[KLauS2.0 – analog only]

<u>KLauS development status</u>

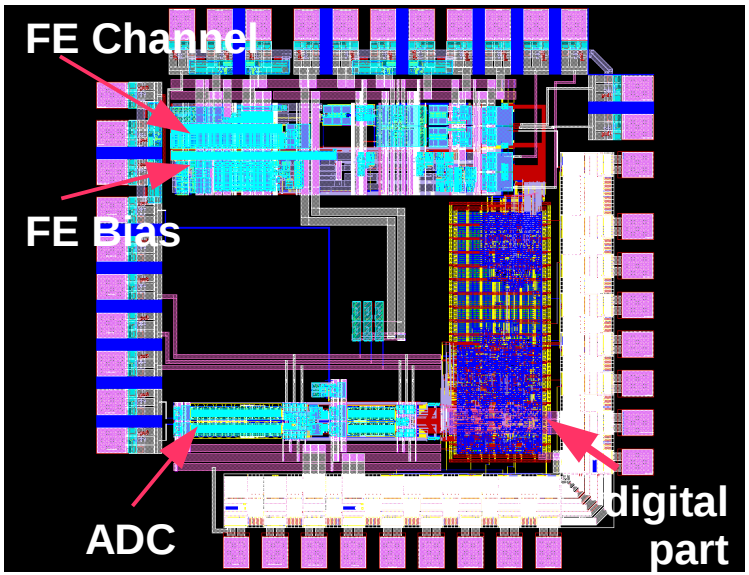
'KLauS2' : AMS 350nm Technology [Design: W. Shen, 2010]
→ Validation of input stage topology
'KLauS3.0a/b' : UMC 180nm (March/15 & May/15)
→ ADC [Design: W. Shen; Layout: H. Chen]
→ New front-end [Design: K. Briggl]

<u>Further development plans</u>

Until Summer 2016

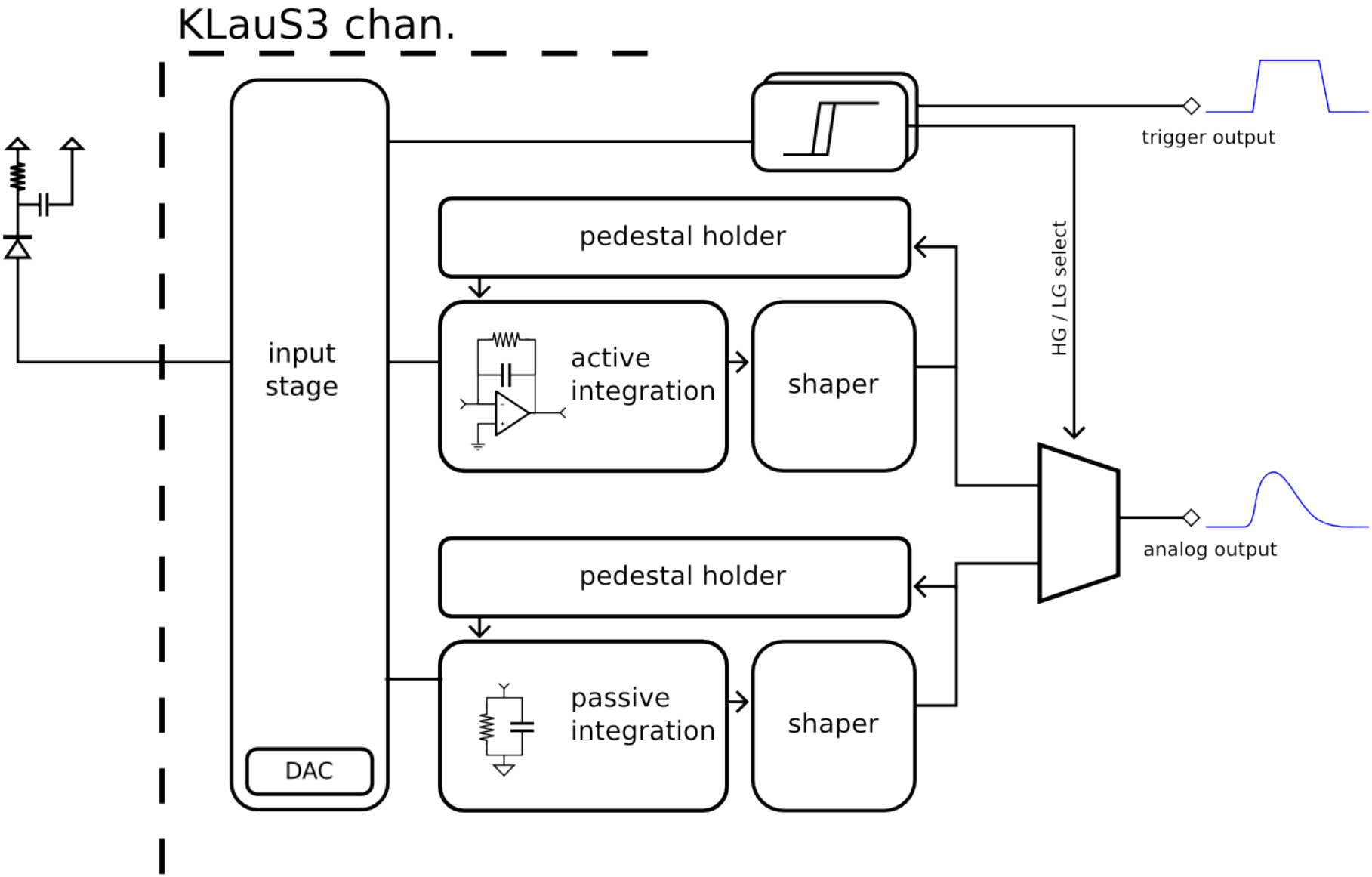
Multi-channel readout ASIC

Combined front-end; ADC; basic TDC blocks

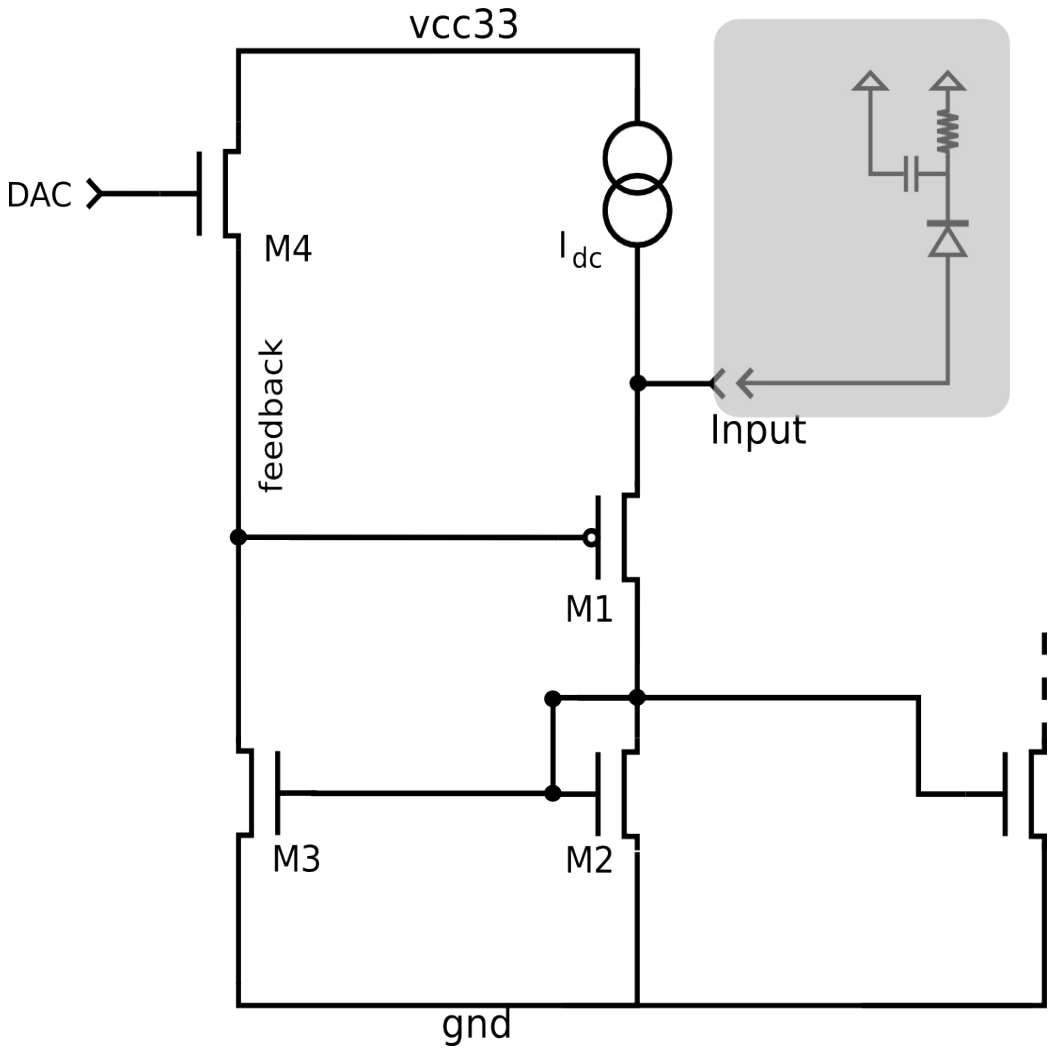


[KLauS3.0 miniASIC – front-end & ADC]

Front-end: block level schematic



Input stage topology



[simplified schematic]

Common gate & current feedback

$$R_{in}^{DC} = \frac{1}{g_{m1}} - \left(\frac{g_{m3}}{g_{m2}} \times \frac{1}{g_{m4}} \right)$$

Nominal input impedance ~50Ω

150uA bias current @ 3.3V

SiPM Bias voltage tuning

['DAC' → 'feedback' → input]

~ 2V tuning range

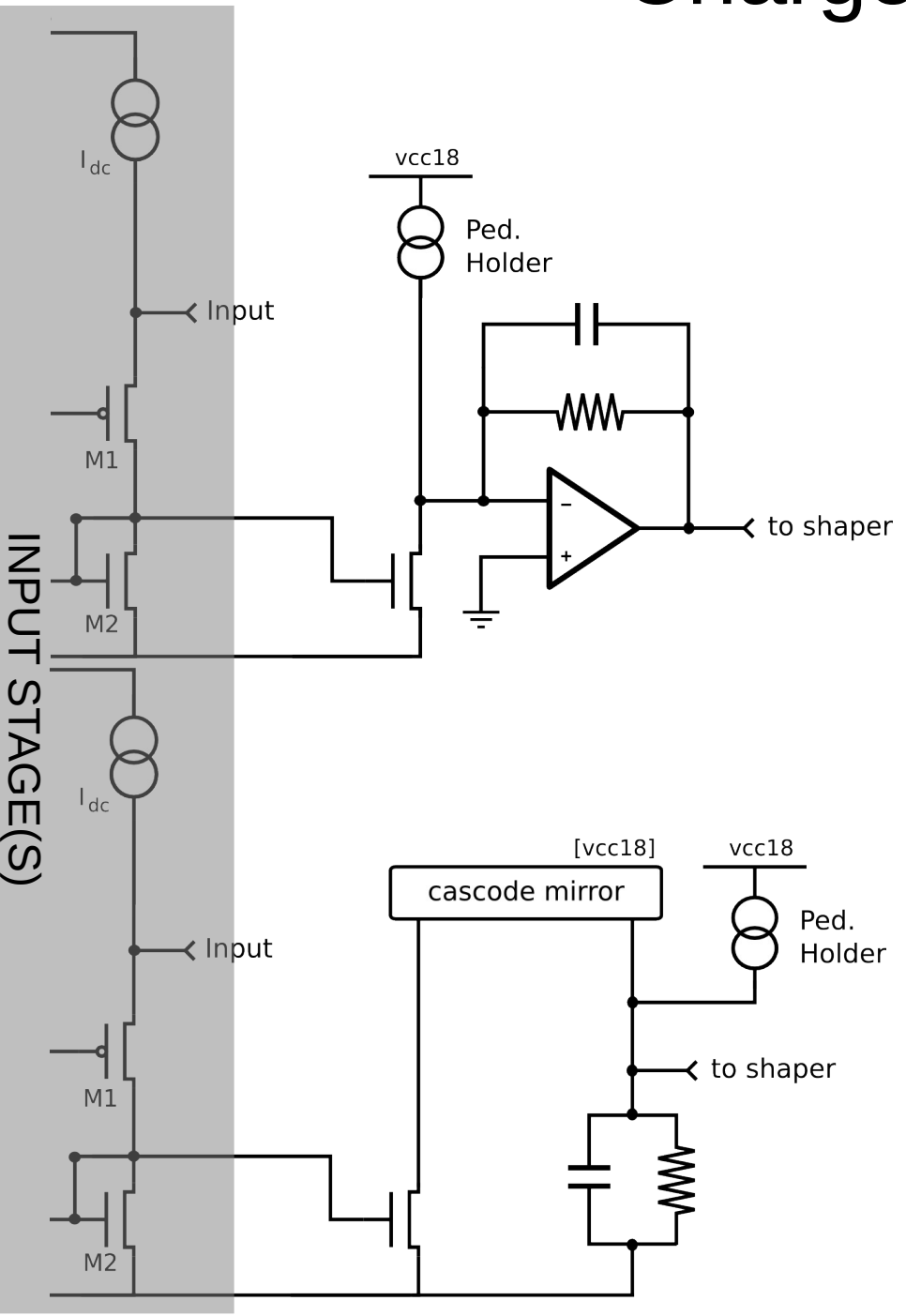
Low power 8bit DAC

2nA / LSB

Power gating compatible

Small DC input voltage change in low power mode

Charge integration



High gain stage: Active integration scheme

for small signals on single pixel level

Miller-opamp with 400MHz GBW

Low gain stage: Passive integration

for large signals

input stage mirror: regulated cascode

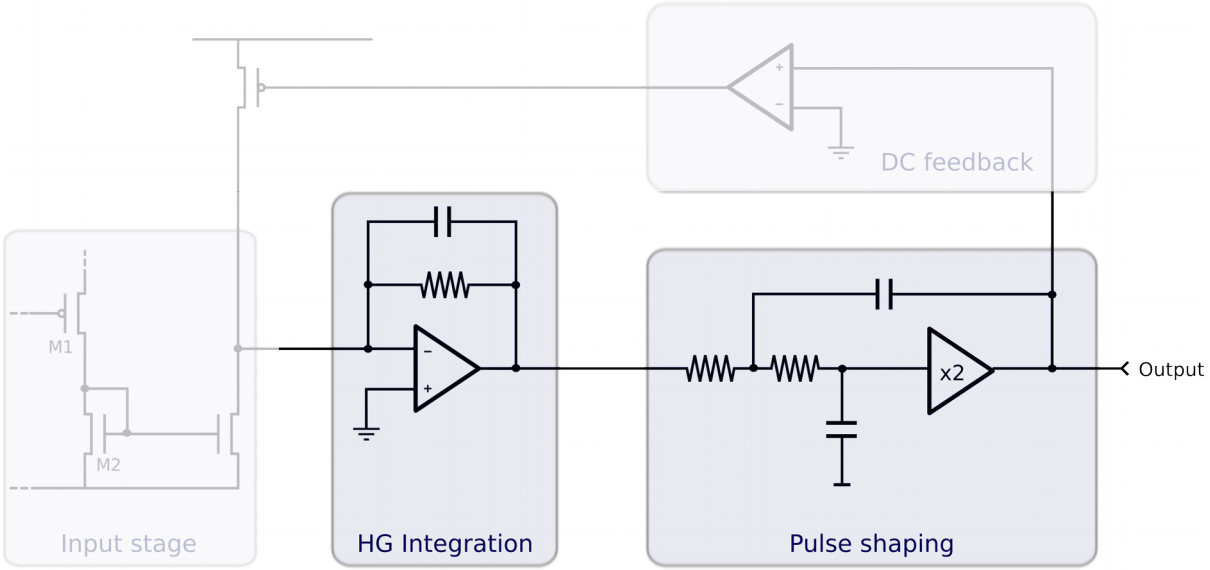
pmos integration mirror: low voltage cascodes

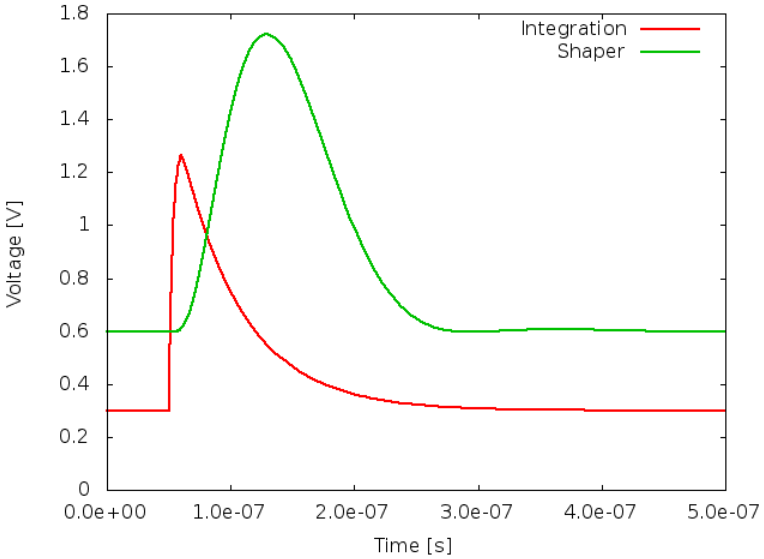
Pedestal stabilization

DC feedback of channel output

Using subthreshold Amplifiers

Shaper and channel pulse response





$$H(s) \propto \underbrace{\frac{1}{s \cdot \tau}}_{Integration} \cdot \underbrace{\frac{1}{(s \cdot \tau + 1)^2 + 1}}_{Shaper}$$

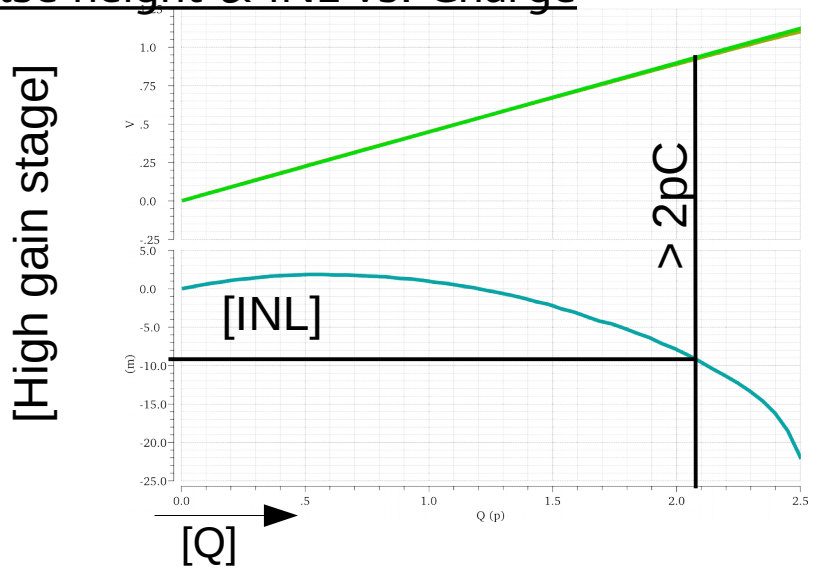
$$h(t) \propto e^{(-t/\tau)} \cdot \left(1 - \cos\left(\frac{t}{\tau}\right)\right)$$

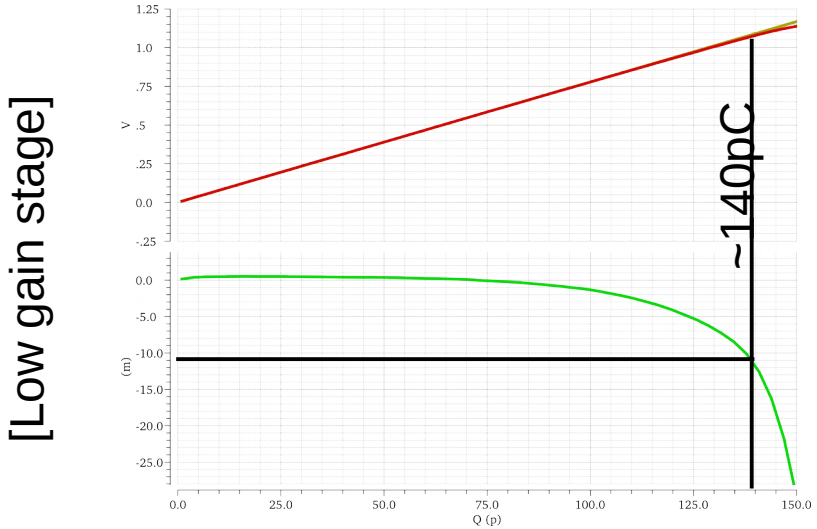
Shaper: Sallen-Key topology
→ pair of complex poles

Same time constants for integration & shaper
→ Semi gaussian pulse, small undershoot

Simulations: Linearity & Noise

Pulse height & INL vs. Charge





High gain stage

Design goal:

Allow decent SNR for very low gain Sensors

[e.g. Hamamatsu 10µm series, Gain ~10^5]

Expected ENC < 3fC

→ Single pixel S/N > 5

Dynamic range ~ 2pC @ INL < 1% FSR

[≈ 135px for 10µm ; ≈34px for 25µm MPPC]

Low gain stage

Exploit SiPM dynamic range

~ 140pC @ INL < 1% FSR

Moderate SNR requirements

Equivalent noise charge ~ 50fC

Front-end measurements: SiPM bias voltage DAC

Measure DC voltage at SiPM input

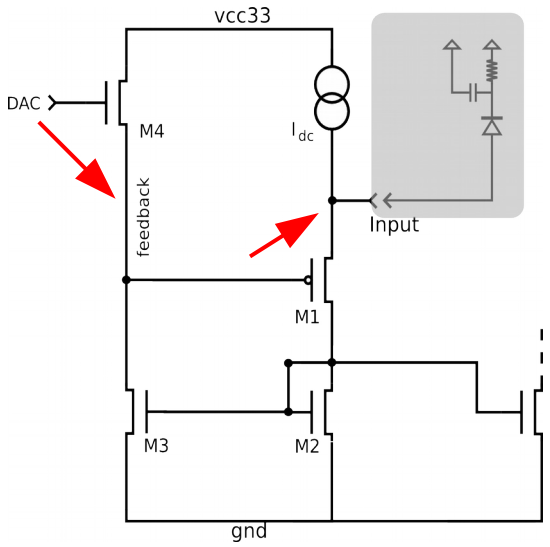
2V tuning range achieved

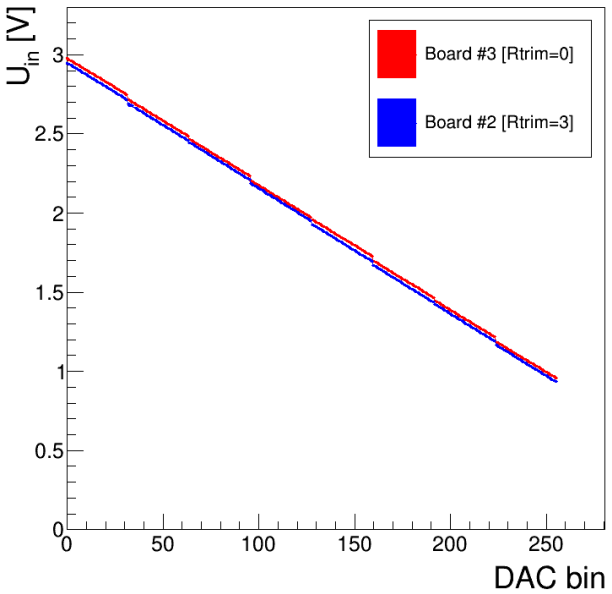
Analysis of Nonlinearity sources

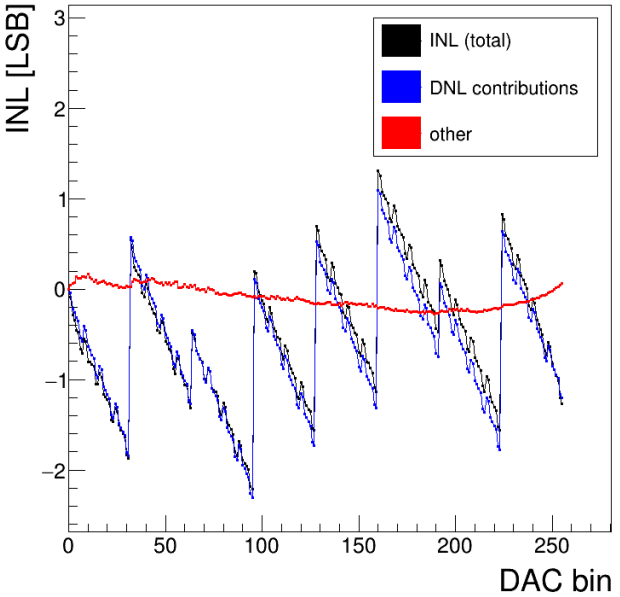
Main source is DNL (3 LSB)

[Layout update in next submission]

Other sources negligible & as expected



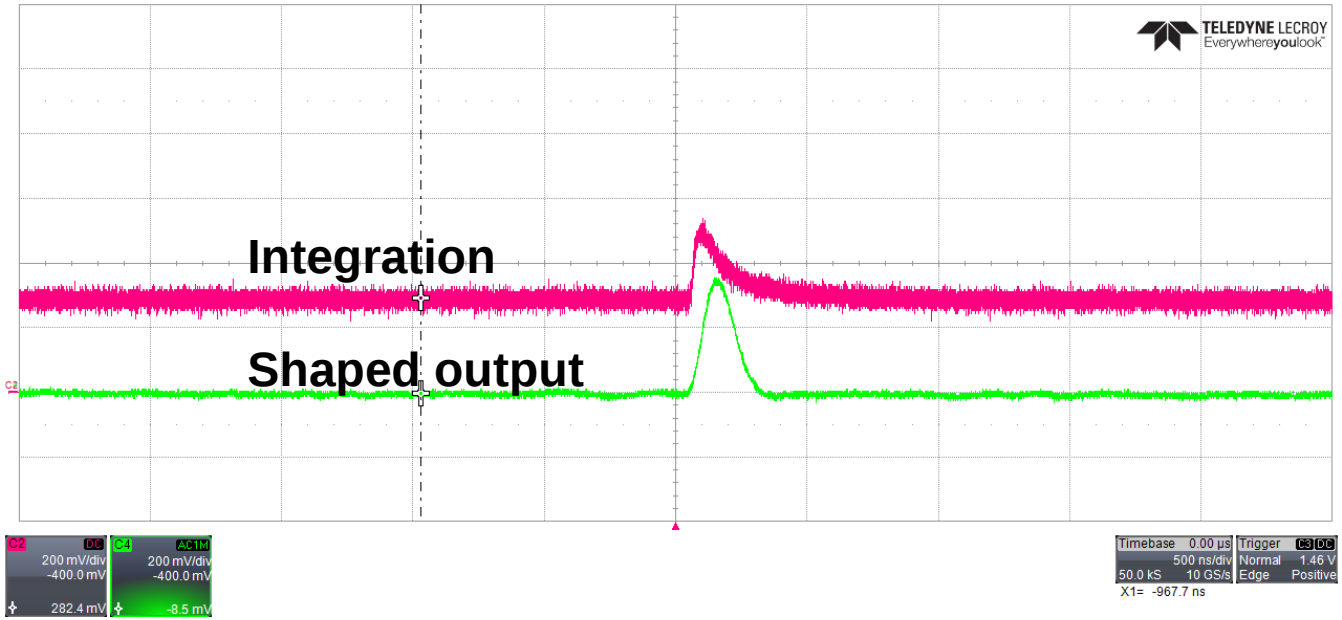


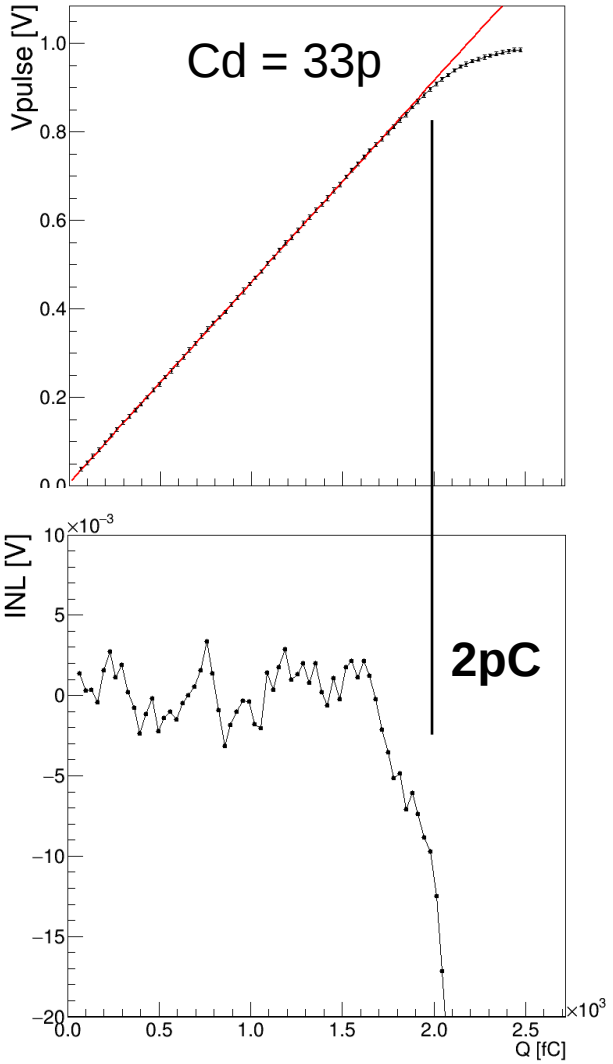


Front-end measurements: Charge injection

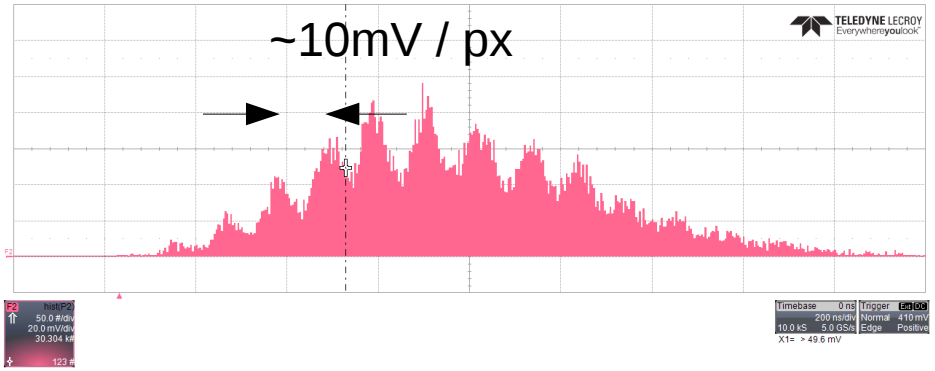
Test of high gain stage

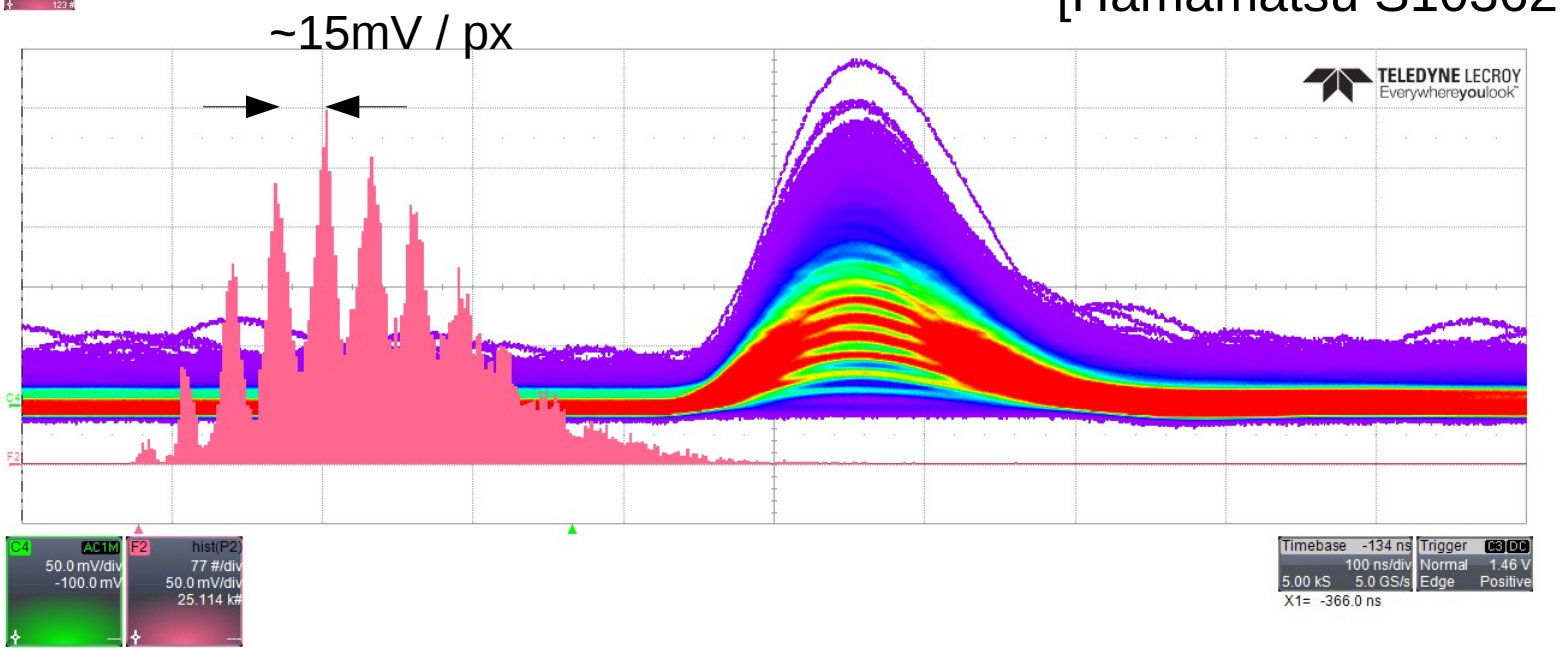
- Pulse shape after integration & shaping
- Dynamic range
  - Sufficient for single pixel spectra
  - Preliminary bias settings
  - Limited by off-chip driver dynamic range





Front-end measurements: test with sensors





Two SiPM models tested

10µm pixel device [Gain ~1.5x10^5]
[Hamamatsu S12571-010C]

25µm pixel device [Gain ~2.75x10^5]
[Hamamatsu S10362-11-025C]

SAR ADC development for KLauS

1 ADC per front-end channel
→ Development of low power ADC

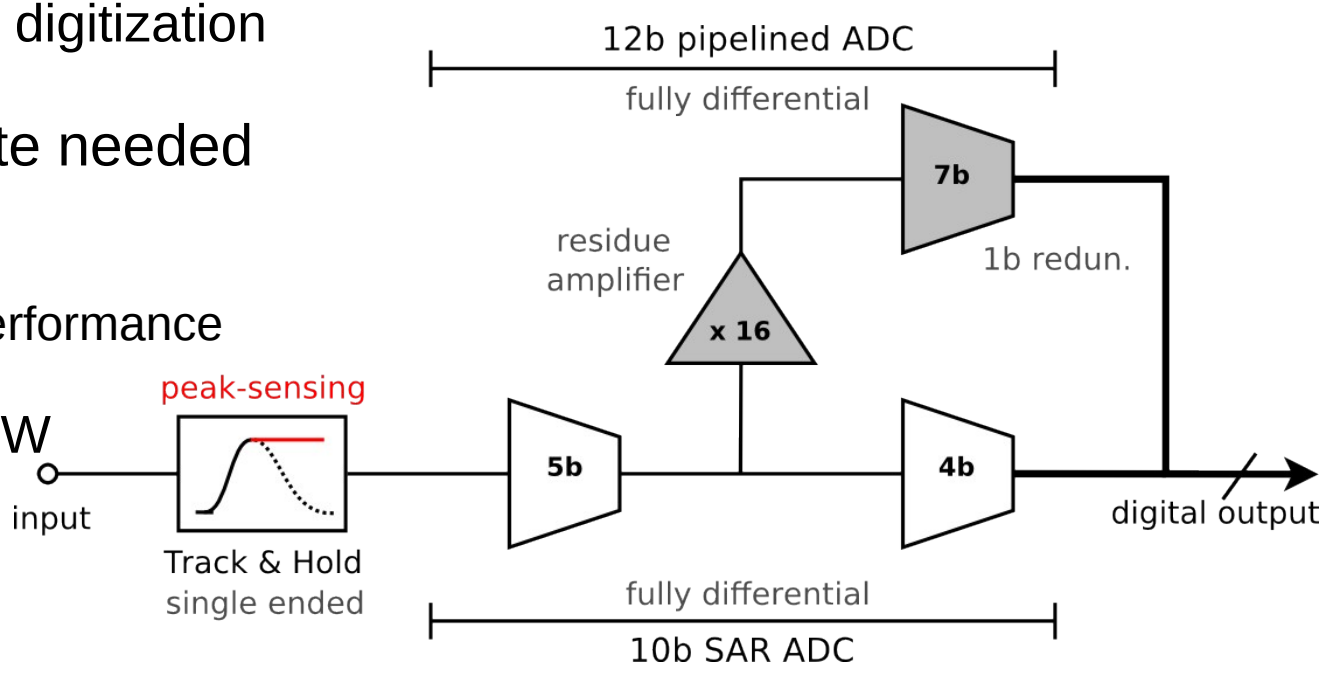
Two operation modes:

MIP quantization – **10bit resolution**
5+4bit SAR ADC

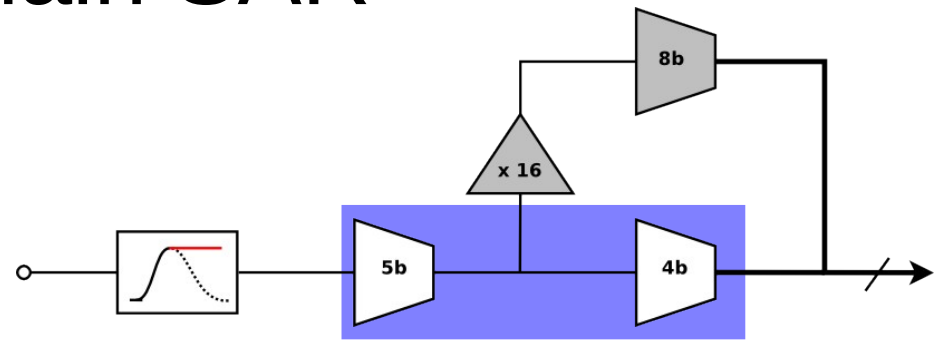
SiPM gain calibration – **12bit resolution**
Additional pipelined stage
Residual amplification & digitization

Relatively low Sampling rate needed
Peak voltage digitization
validated up to 3MHz
No constraint on dynamic performance

DC Power consumption < 1mW

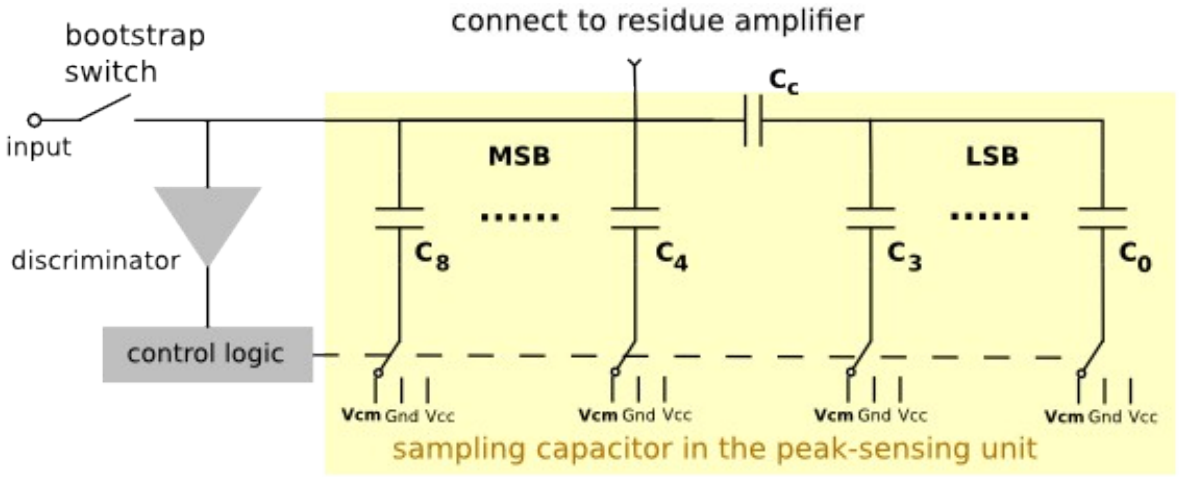


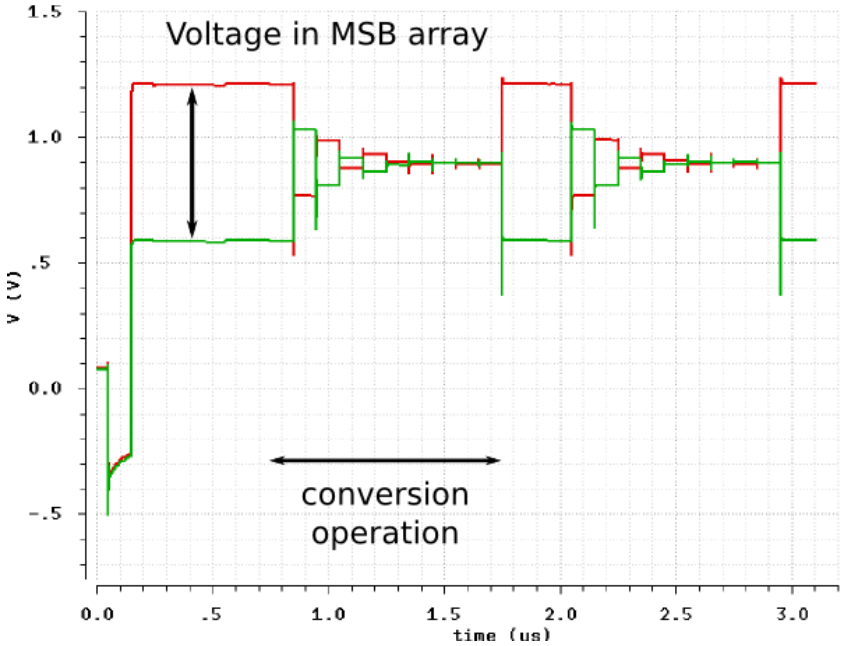
ADC – 10bit main SAR



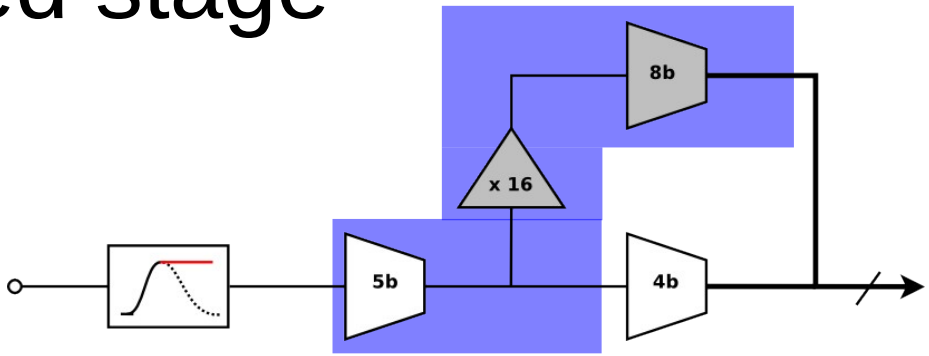
SCA:
5+4bit binary MIM capacitor array
Unit capacitor ~ 34fF

Other blocks:
Dynamic comparator
Bootstrap sampling switch
Control logic in digital part





ADC: Pipelined stage



12b resolution operation mode
for SiPM spectrum digitization

<u>3 digitization steps:</u>

(1) 5b digitization in main SAR

(2) Amplification of residual error

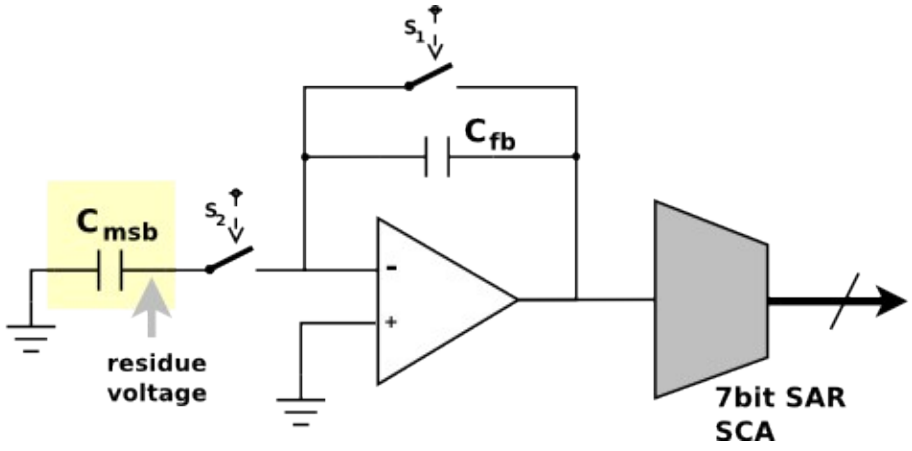
Fully differential folded cascode amplifier

(3) 8b digitization in pipelined stage

5+4 split MIM capacitor array

Unit capacitor ~ 34fF

remaining bits saved for redundancy



(1) (2) (3)