Calorimeter Trigger Algorithms on a Xilinx Virtex-5

John Jones

Department of High Energy Physics
Princeton University

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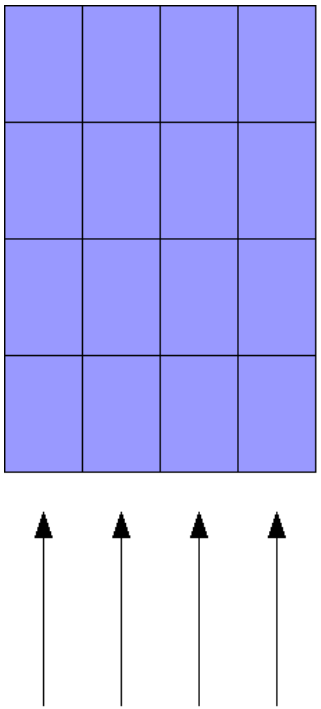
Outline

- Effect of serial links & pipelining
- Take current calorimeter trigger algorithms and merge into unified system
- Proposal for a new μTCA card
- Performance summary

- Serial links add significant latency per stage in a system
- Combinatorial logic fanout in Xilinx devices can limit performance and cause large device usage
- Performance tends to be dominated by `wire` delays
- Instead of using combinatorial fanout, use deep pipelining

- Reduce RCT & GCT operations to micro-operations
- Interlock each one with a register
- Maximise pipeline speed and minimise resource usage in FPGA to stay in chip as long as possible (fewer ‘hops’)
- Minimise combinatorial fanout
- Pipelined bitonic sort in last stage

Serialisation of data



4 towers, 3.2Gbit/s

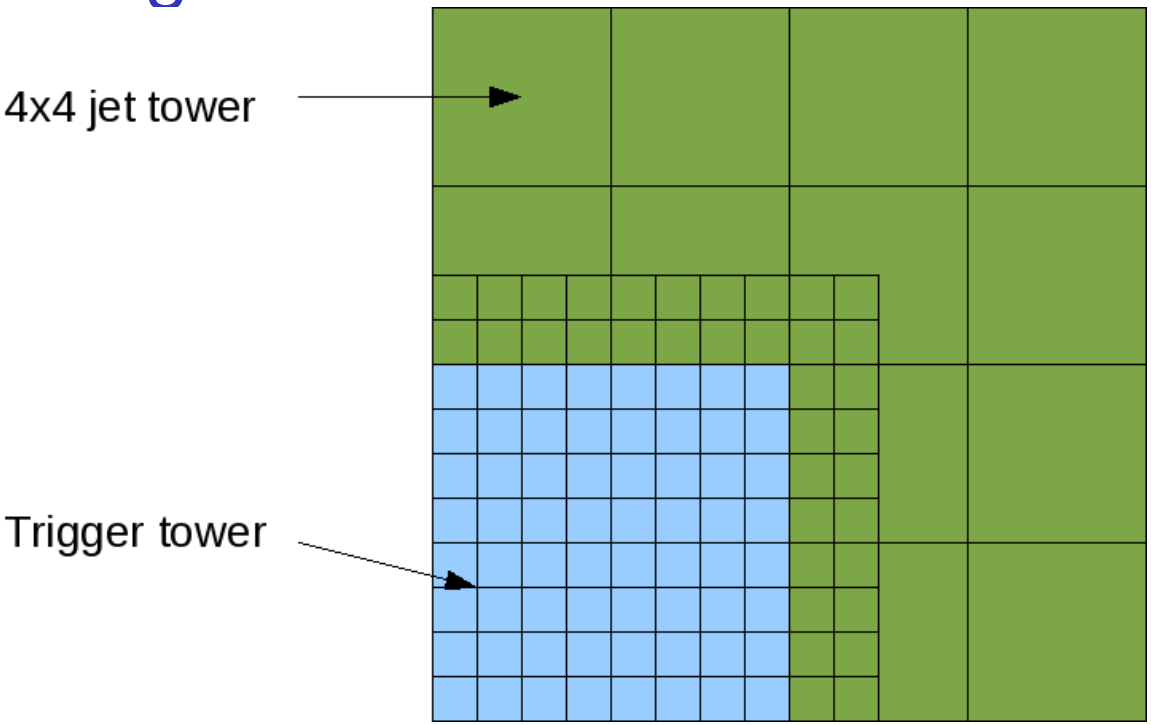
32 electron finders, combinatorial (A. Rose, Imperial College)

- 20% of slice LUTs, minimal register usage
- Estimated maximum clock speed: 17MHz
- Not necessarily what we want...

One jet finder & 144 electron finders, deep pipelining

- Selected Device : 5vlx110tff1136-3
- Number of Slice Registers: 2540 out of 69120 (3%)
- Number of Slice LUTs: 3264 out of 69120 (4%)
- Not including some boundary cases (resource usage will increase approximately 50%)
- Estimated maximum clock speed: 184MHz (could easily be improved - electron finders alone were 260MHz w/o significant optimisation)
- Current total latency approx. 8BX (internal, mostly sort, can be halved easily)
- I/O usage (assuming 16bits per tower, 3.2Gbit/s): 49 links (!)
- So now we have another problem...

I/O Usage

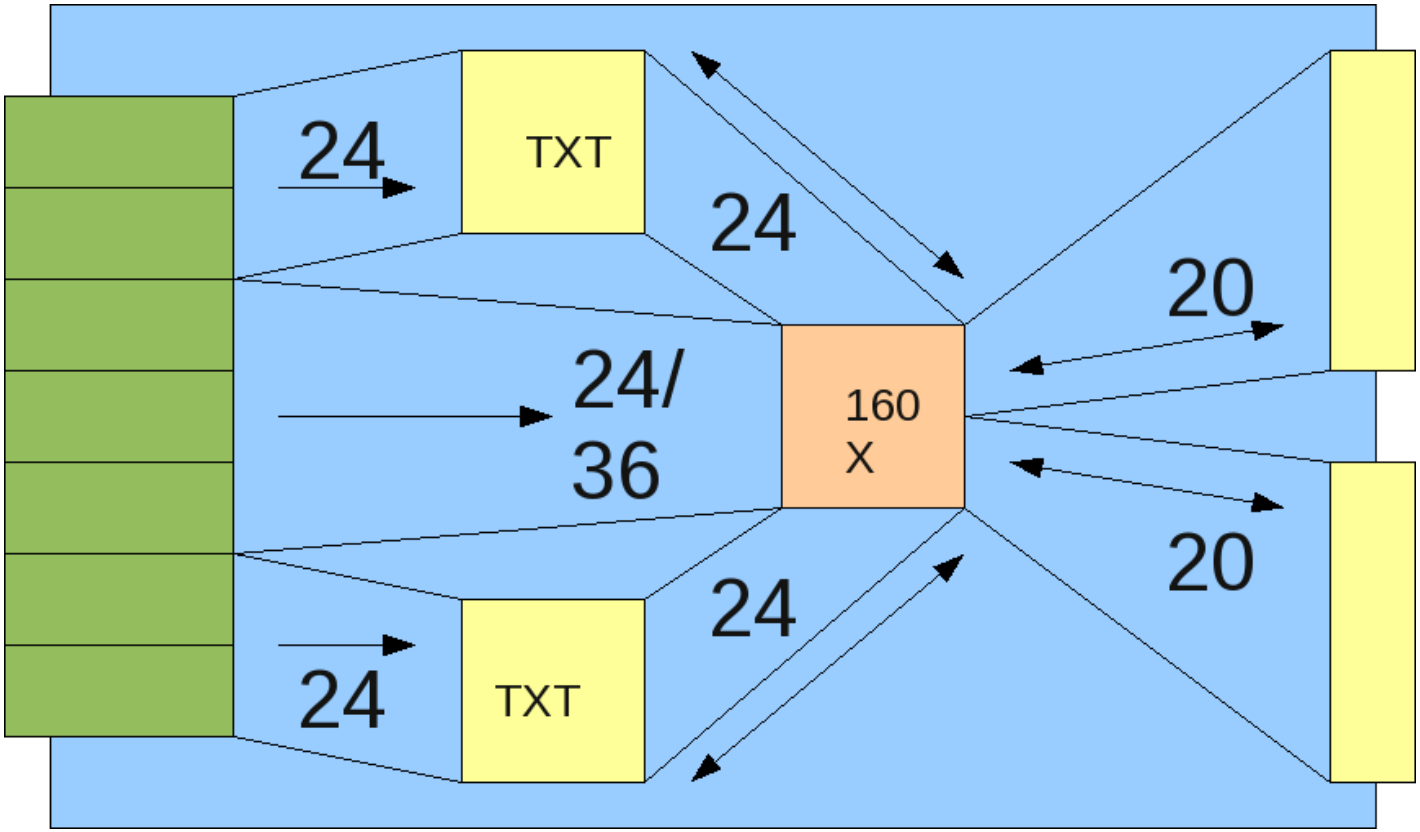


- Jets are the problem (non-compact)
- If we use more than one data granularity, we can reduce the I/O usage
- e.g. 4 jet finders, 64 electron finders => 28 links 3.2Gbit/s

Proposal

- What we need is a highly asymmetric processing card (far more inputs than outputs)
- Largest Xilinx FPGA (I/O) is now the 48-input TXT (6.5Gbit/s)
- Maximise the number of inputs to provide a reasonable data reduction

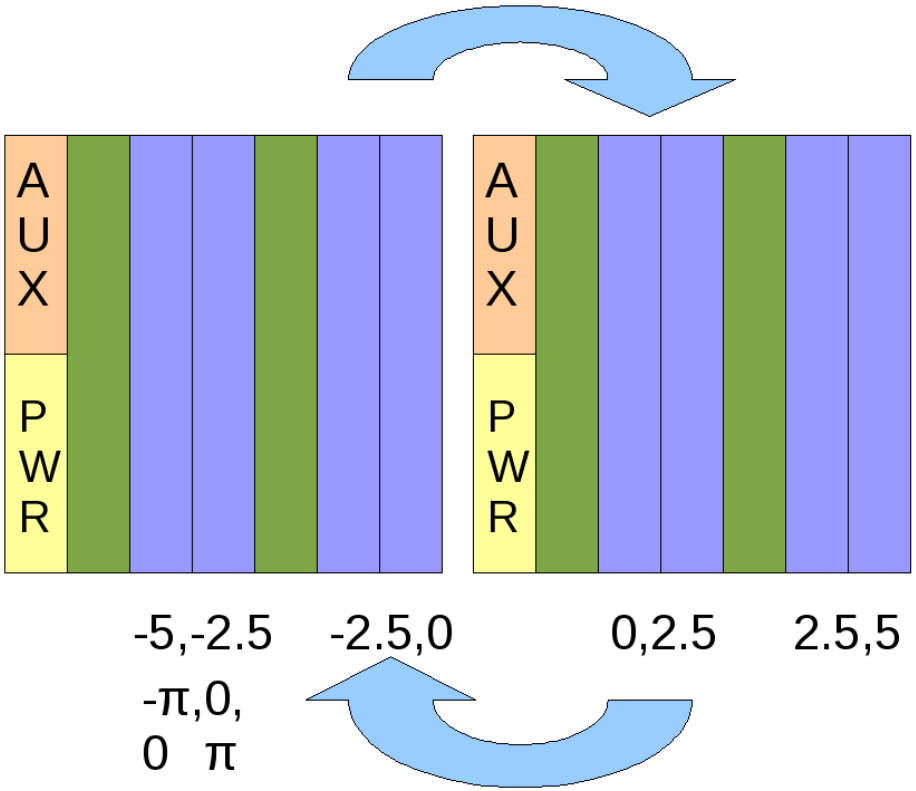
Proposal II



Consequences

- Matrix card has 16 links, 3.2Gbit/s, this card would have 72-84 optical links (6.4Gbit/s)
- This increases the bandwidth by 9-10.5x
- Would result in e.g.: 59 full-granularity + 5 jet links (some spare for future)
- Should provide more ‘reasonable’ balance between logic & I/O
- This is a half-barrel in ϕ, approx. 2.5 in η
- Should need approximately 8 cards for whole GCT/RCT (i.e. a 6U crate)

Crate layout



- At full granularity, we are massively I/O constrained
- We are not going to be able to fill the current generation of devices
- We may well end up being able to fit the entire CT in a single chip within 3-5 years, provided link density increases
- It's feasible to go to full granularity for e.g. jets, but this does increase bandwidth usage
- The logic pipeline speed must keep up with the links...