Minnesota uTCA Project Status

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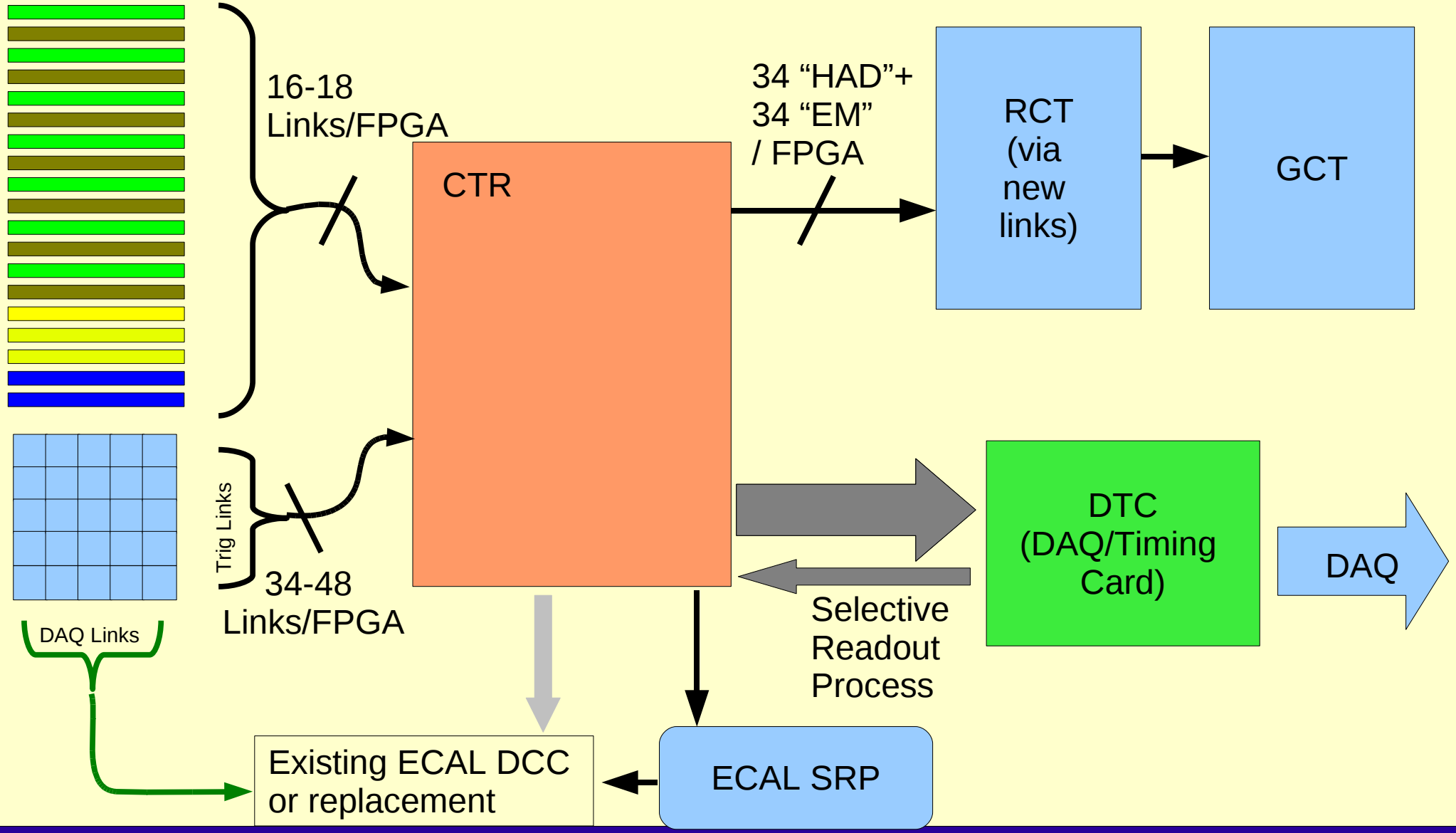
Project Goals

- Evaluate uTCA technology
  - Initial focus on “large-front-panel” (double width)
  - Achieve familiarity with necessary design principles and control system architecture
  - Create simple test station for technology evaluation
- Evaluate high-speed link performance (latency and stability) for potential HCAL upgrades
- Proceed toward design appropriate for CMS HCAL Readout and Calo Trigger upgrade

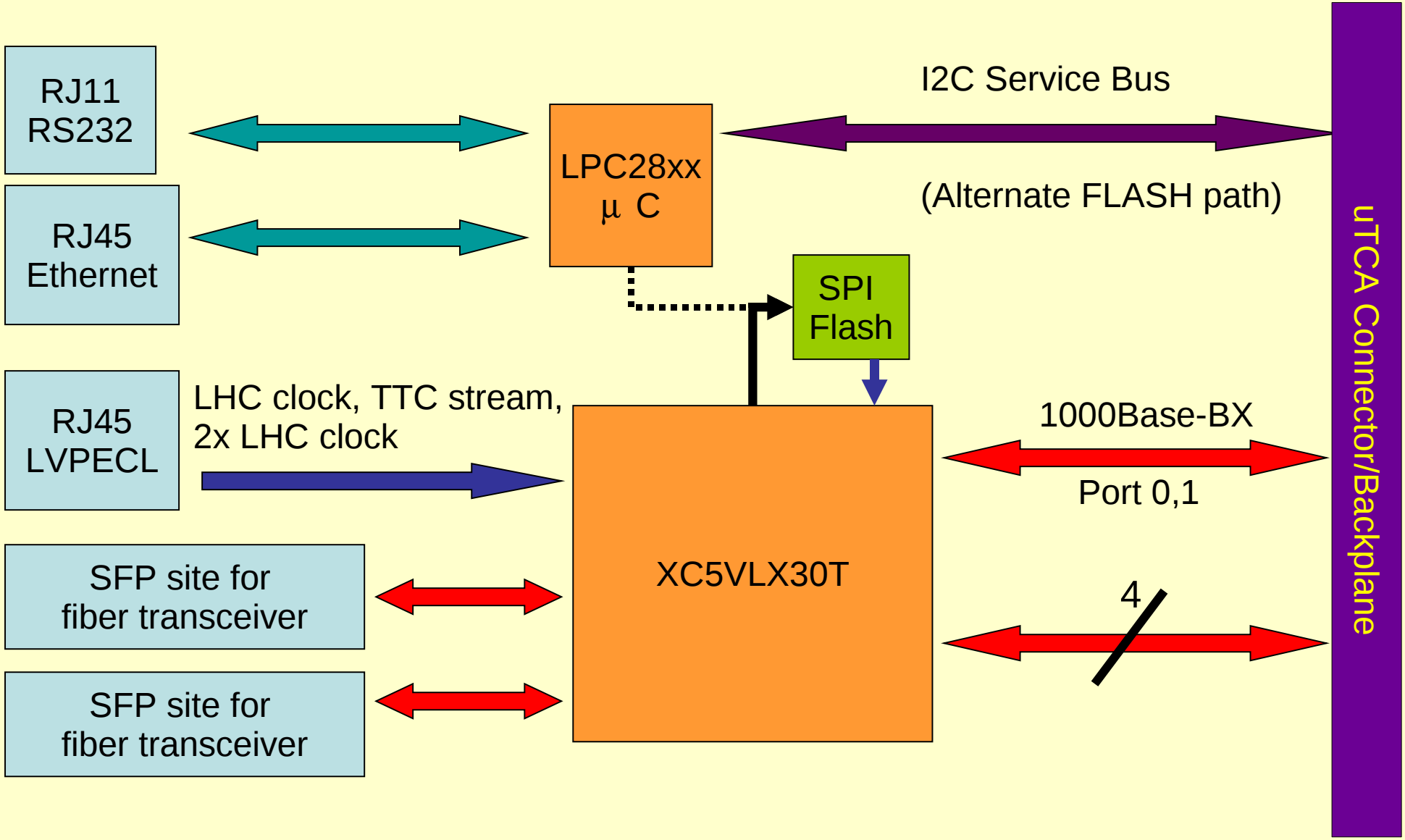
Editorial: Calo Trigger/Readout Design

- Considerations
  - Highest value will be achieved by combining ECAL and HCAL inputs as early as possible
  - Inclusion of HO from Ring Zero may be necessary for controlling MET triggers at high occupancy
  - Selective readout is likely to be necessary for the *calorimeters* as a whole under SLHC conditions
- Implications
  - Counting rooms electronics should be ready to receive both new generation links O(3-5 Gbps) and legacy links (800Mbps) => large front panel and multiple technologies required

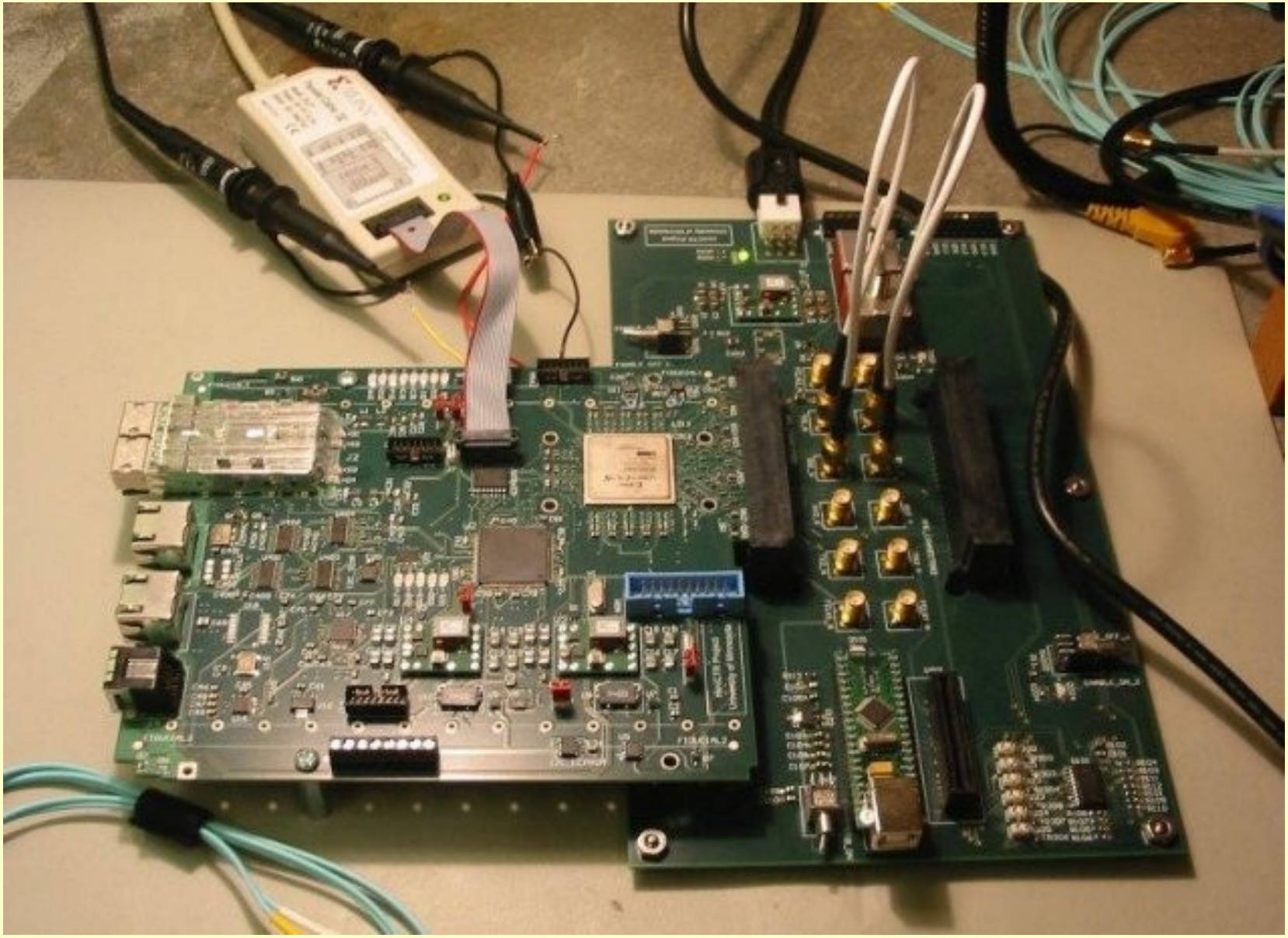
Possible Initial Upgrade Architecture



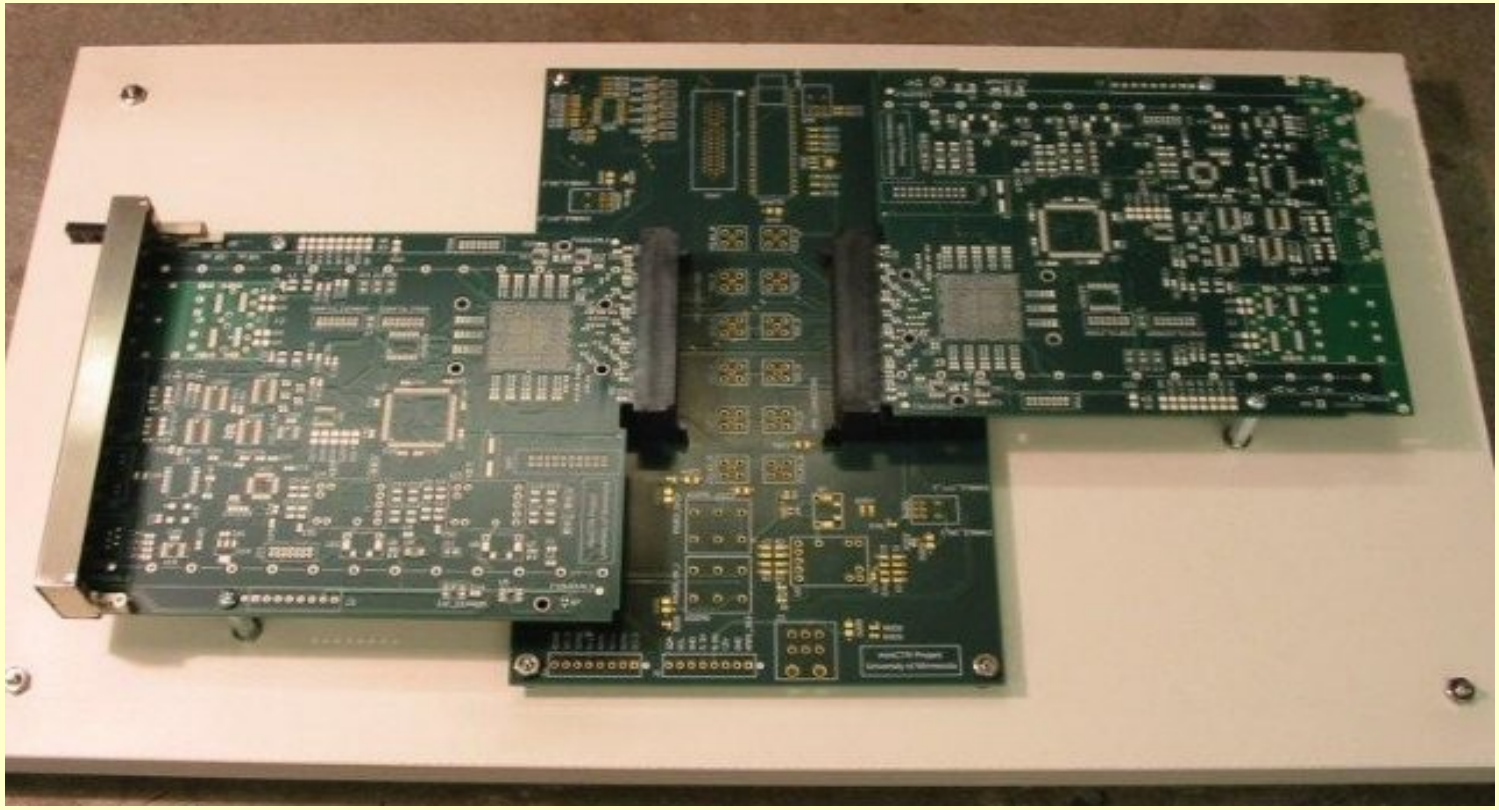
"miniCTR" Architecture



“miniCTR” card + teststation



Test Station Overview



- Test station supports two cards with port interconnects as well as SMA connector sites for other tests
- Host board provides power, I2C interface, ethernet interface, card resets, etc

Status of Project

- Boards received mid July
- FPGA commissioned
  - Programming of FPGA by FLASH and directly by JTAG working fine
  - All I/Os functional
  - Optical links up to 2.5 Gbps (optical device limit)
  - Electrical links tested up to 3.125 Gbps
  - Clock MUXes/crosspoint-switches work well
- Latency measurements
  - TX+RX : 104 ns for a 90cm fiber connection timing on external pins in loopback mode
- Testing firmware TTCrx decoder

Plans

- Currently testing reception of copper GLINK for ECAL trigger link integration
  - Expect to make second revision board in near future to allow full evaluation with optical links
- Test reception of HCAL data from “legacy front ends”

- Commission I2C controller system
  - Question: shared design development project here? The uTCA spec makes a lot of requirements. We could benefit from a standard C library which handled most of this, with limited customization for the details of a given board
- Test integration in a standard uTCA crate with a standard MCH
  - Expect to order a small crate in the near future for such tests

Thoughts on SLHC Electronics Formats

- Development of a uTCA board has been somewhat more complex than a classic VME card, but not overwhelming
  - Reasonable space on a “double width” format for layout
- Backplane links seem to “just work” with Virtex 5
- Main concern for subdetector-level electronics is probably front-panel space for the many connectors required (recall large number of low-speed ECAL links)
- Possible alternative: use of ATCA standard without hosting AMC cards
  - Allows 8U space usage with high speed connections on backplane, but fewer connections/rack unit
  - Optimization depends amount of on-board data reduction possible