Some ideas for a tracking and timestamp pixel detector suitable for CLIC

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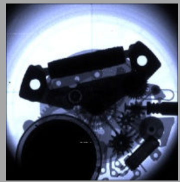
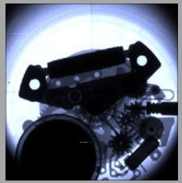
CERN ESE



Outline

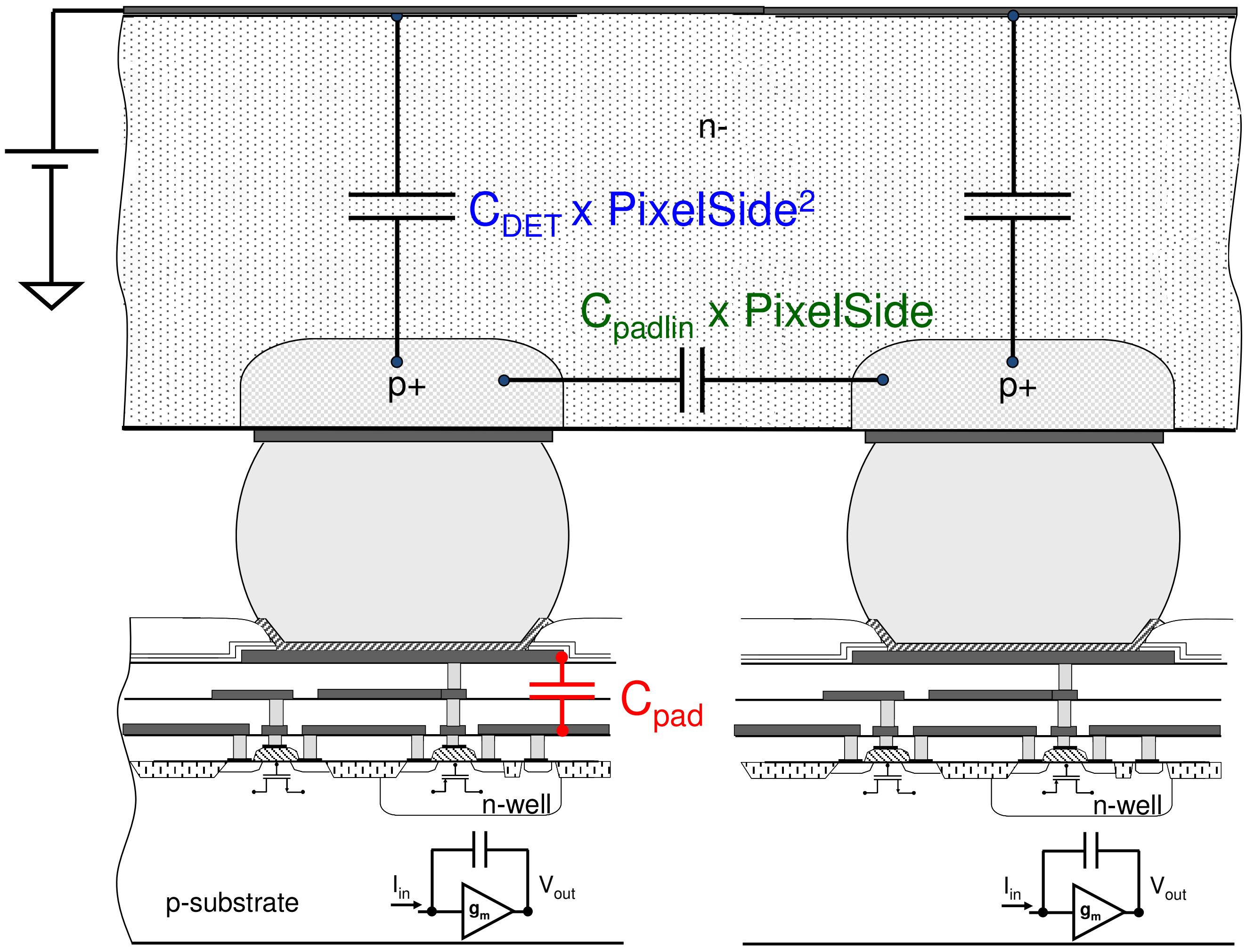
- Assumptions for CLIC
- The effect of segmentation on performance (noise and jitter)
- The Timepix architecture and how it could be improved
- Low mass bump bonding

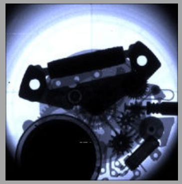


Assumptions for CLIC

- ~312 bunches per train spaced by 0.5ns
- 50Hz bunch rate
- Pixel size <= 15 μm
- Detector diameter 3cm
- Detector length ~20cm
- Physics hit occupancy ~20 hits/train
- Background ~2M hits/train
- Pixel occupancy on inner layer ~ 10^{-2}??
- Total power budget ~ 100mW/cm^2
- Power cycling allows at least x10 more during up time
- Each pixel records bunch number (or a multiple thereof) for a given train
- Full readout between trains

Geometry for readout chip bump-bonded to Si Sensor

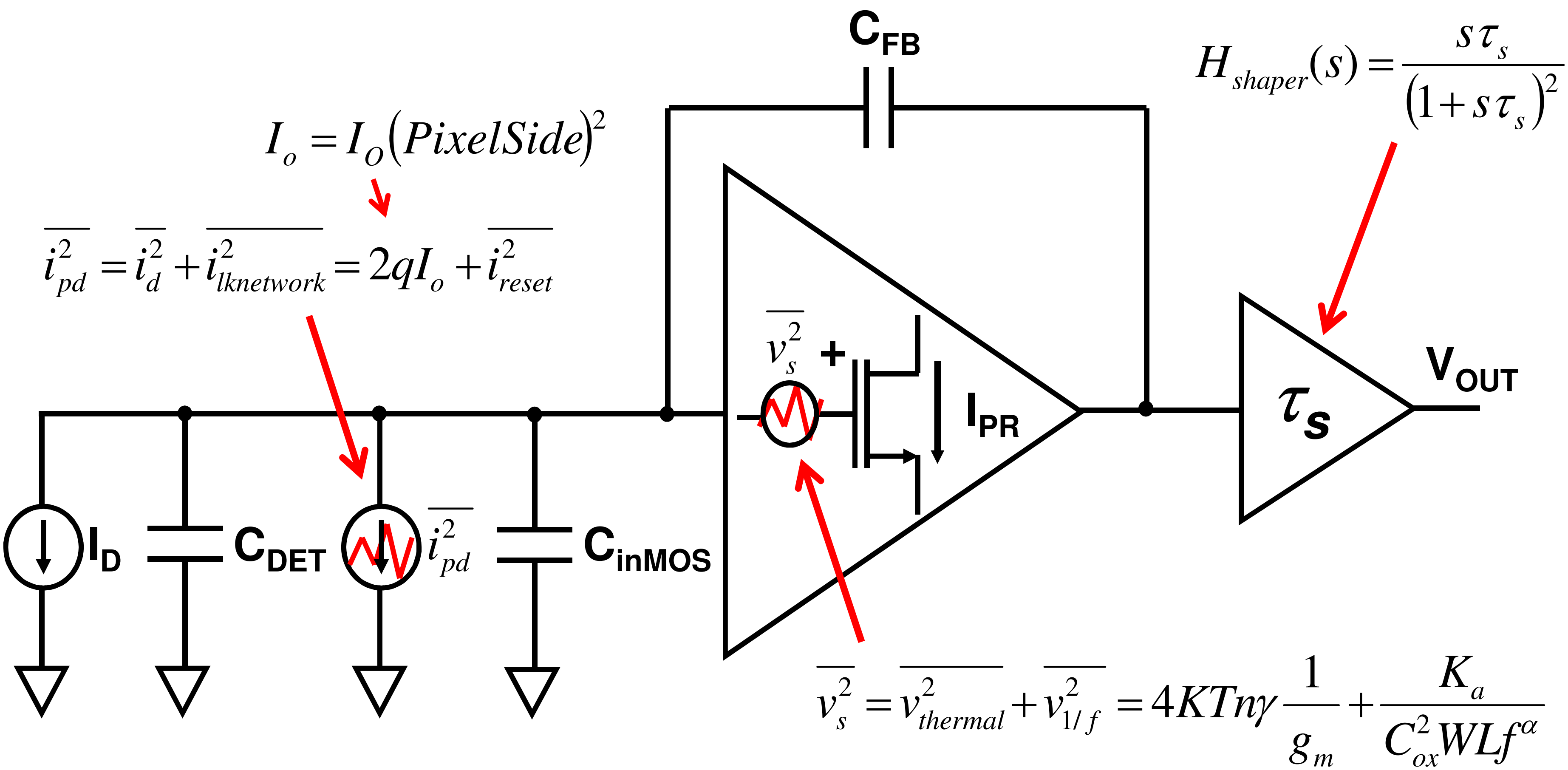




Assumption for noise and jitter calculations

- Constant power dissipation 1W/cm^2
- 70% of the power dissipated in the input stage (differential)
- Collection time must be faster than shaping time
- Charge sharing not taken into account
- The input transistor size is calculated for optimal ENC (Equivalent Noise Charge) for a given pixel size and shaping time
- First order CR-RC shaper

System schematic



Noise equation

Noise Equation:

$$ENC^2 = \left(C_{\det} + C_{inMOS}\right)^2 \left[\frac{\overline{v}^2_{thermal}}{\tau_s} a_w + A_f \, 2\pi a_f \right] + \overline{i}^2_p \tau_s a_p$$

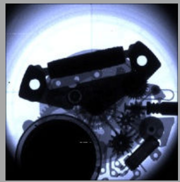
$$\overline{v^2_{thermal}} = 4KTn\gamma \frac{1}{g_m}$$

Calculated from EKV model

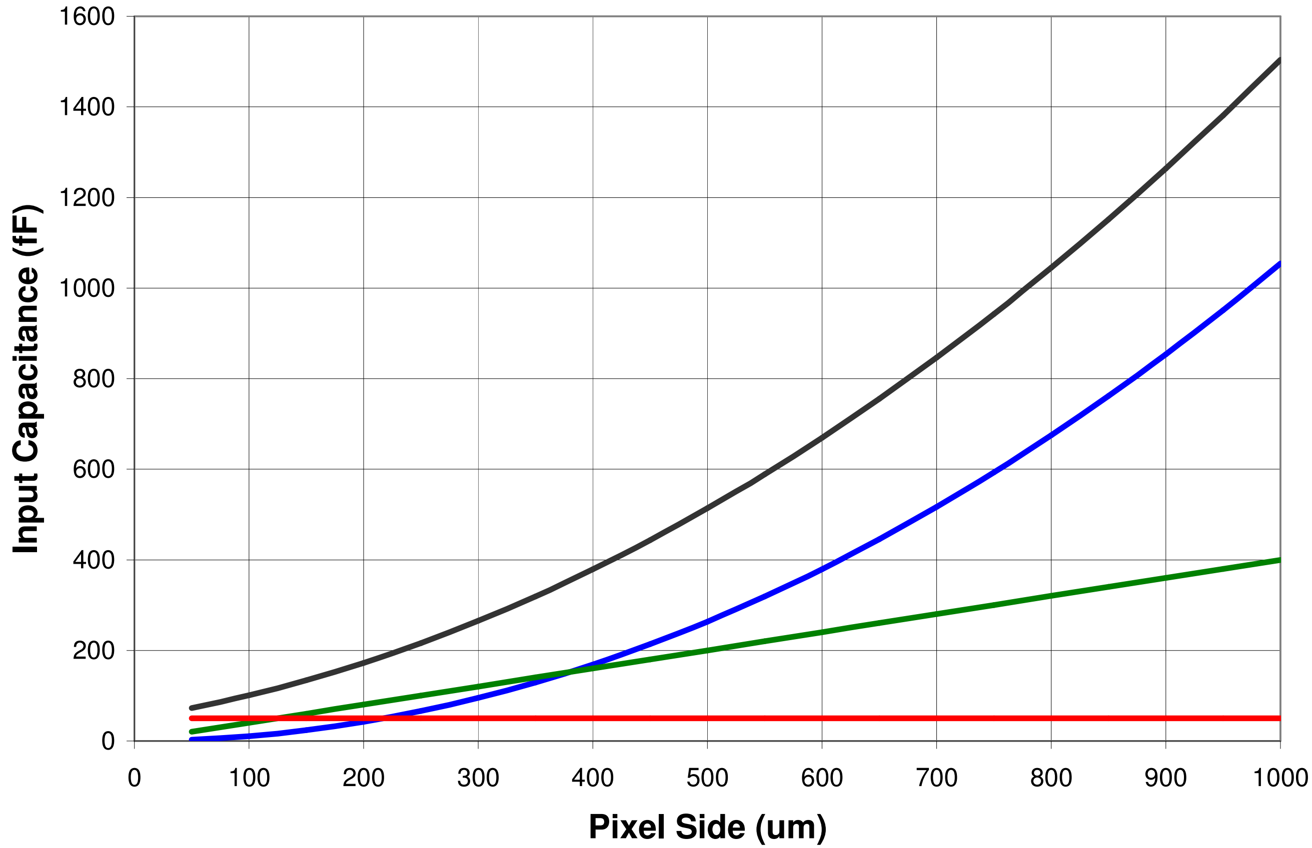
$$A_f = \frac{K_a}{C^2_{ox} WL}$$

$L = 200nm$

W=OptimumW(Pixel Side)



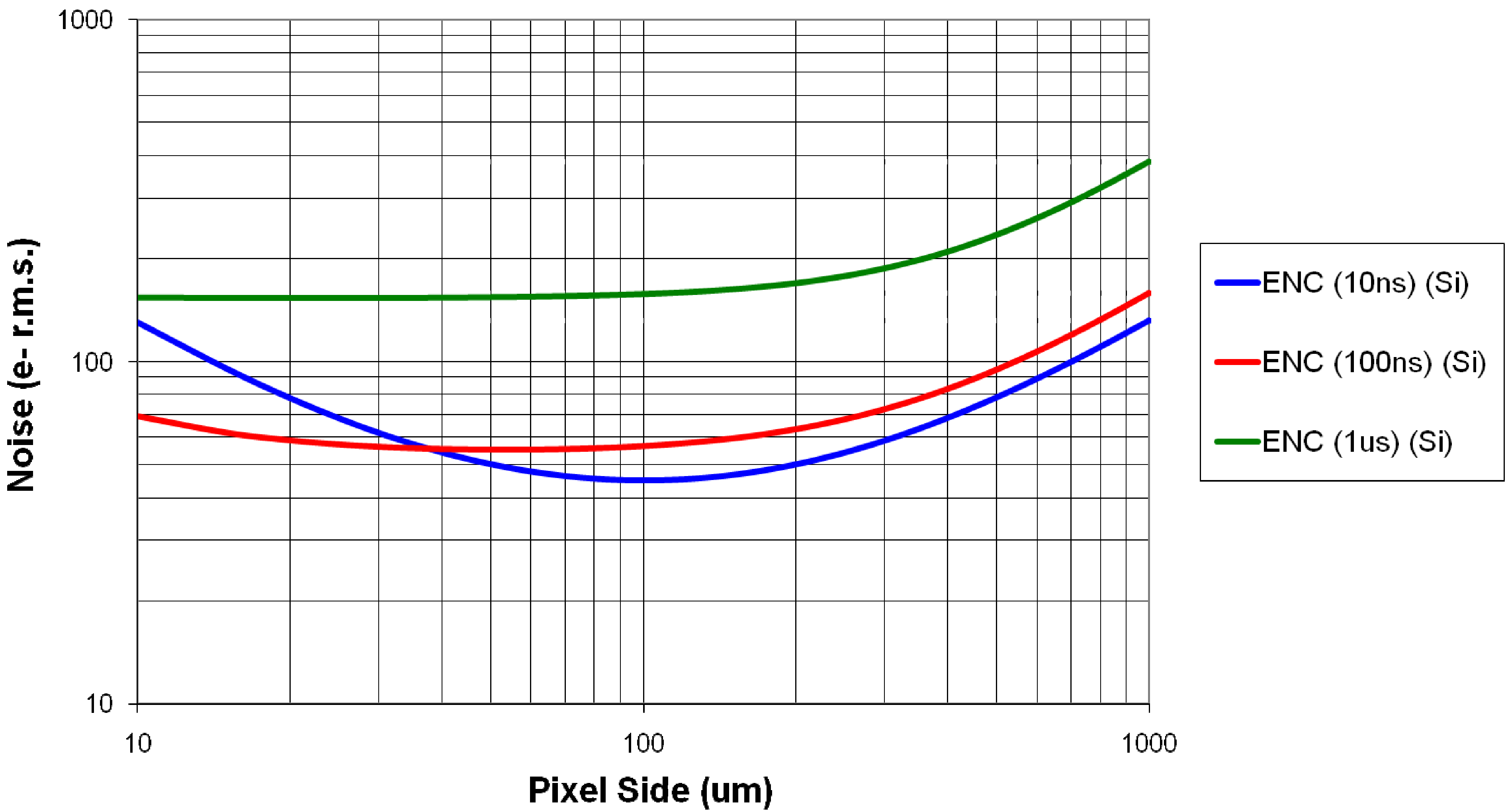
Geometry for readout chip bump-bonded to Si Sensor (input capacitance)



$C_{DET} = \varepsilon / x_D$ C_{padlin}=1pF/cm C_{pad}=50fF (25μm diameter pad)

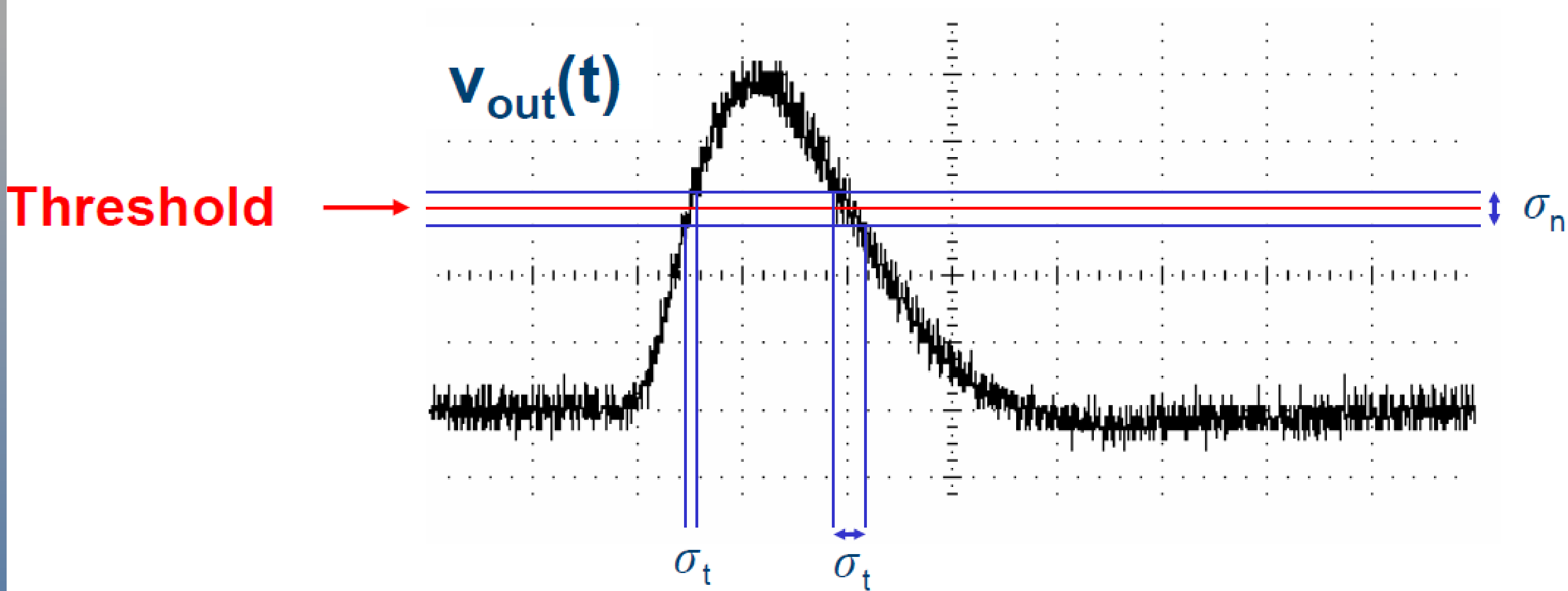
ε is the permittivity (1.054 10^{-12} F cm^{-1} for Si) and x_D is the thickness of the depletion region (x_D equals 100μm in the results presented in this report)

ENC as a function of shaping time



ENC as a function of the pixel side for different shaping times. (1W/cm^2, Si sensor I_{leak} = 1μA/cm^2)

Timing



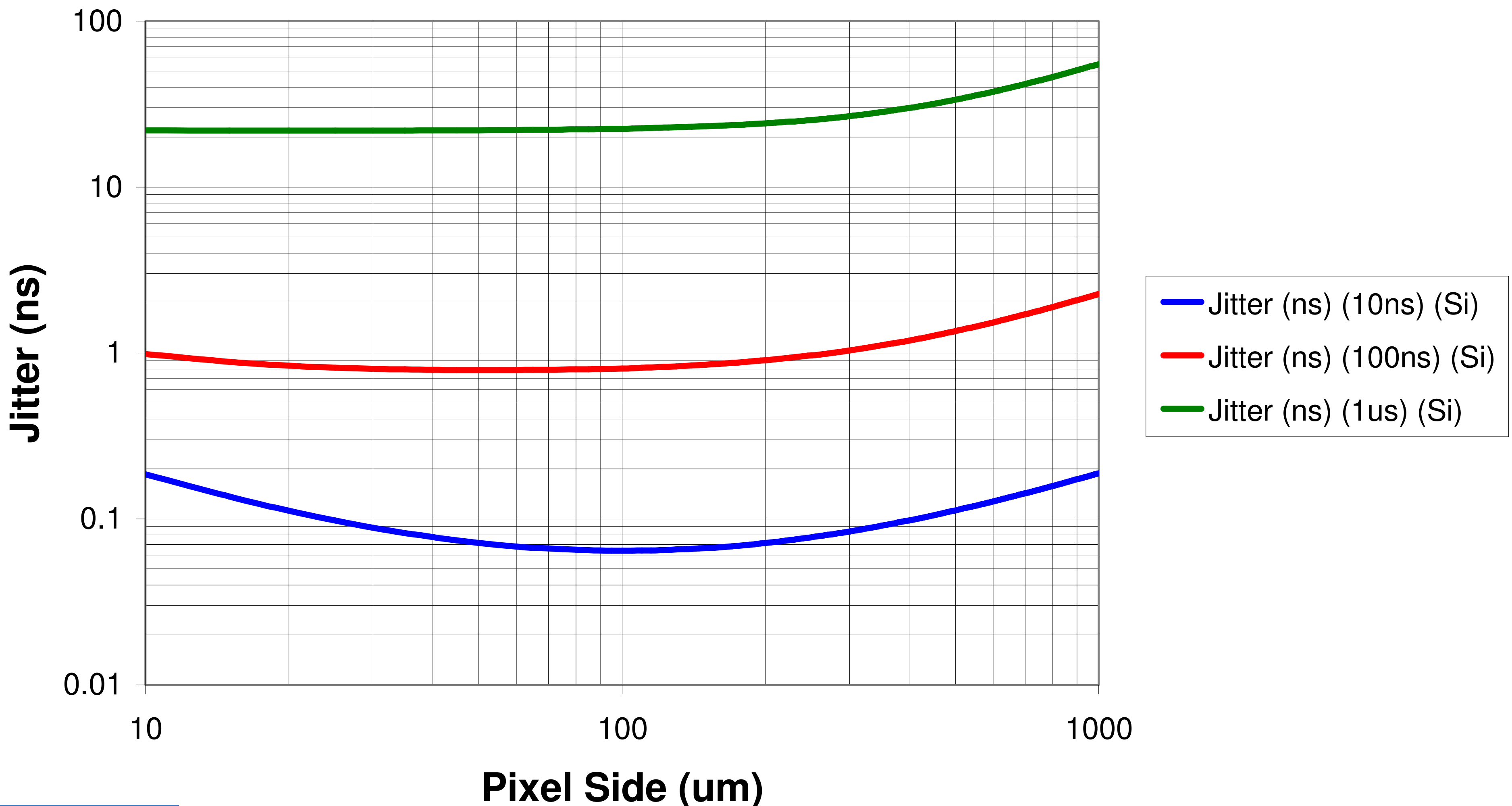
- Triangular signal, Q_{in}=7000e$^-$

$$Jitter(ns) = \frac{ENC \cdot \tau_s}{Q_{in}} \qquad Flux_{max} = \frac{1}{10\tau_s PixelSide^2}$$

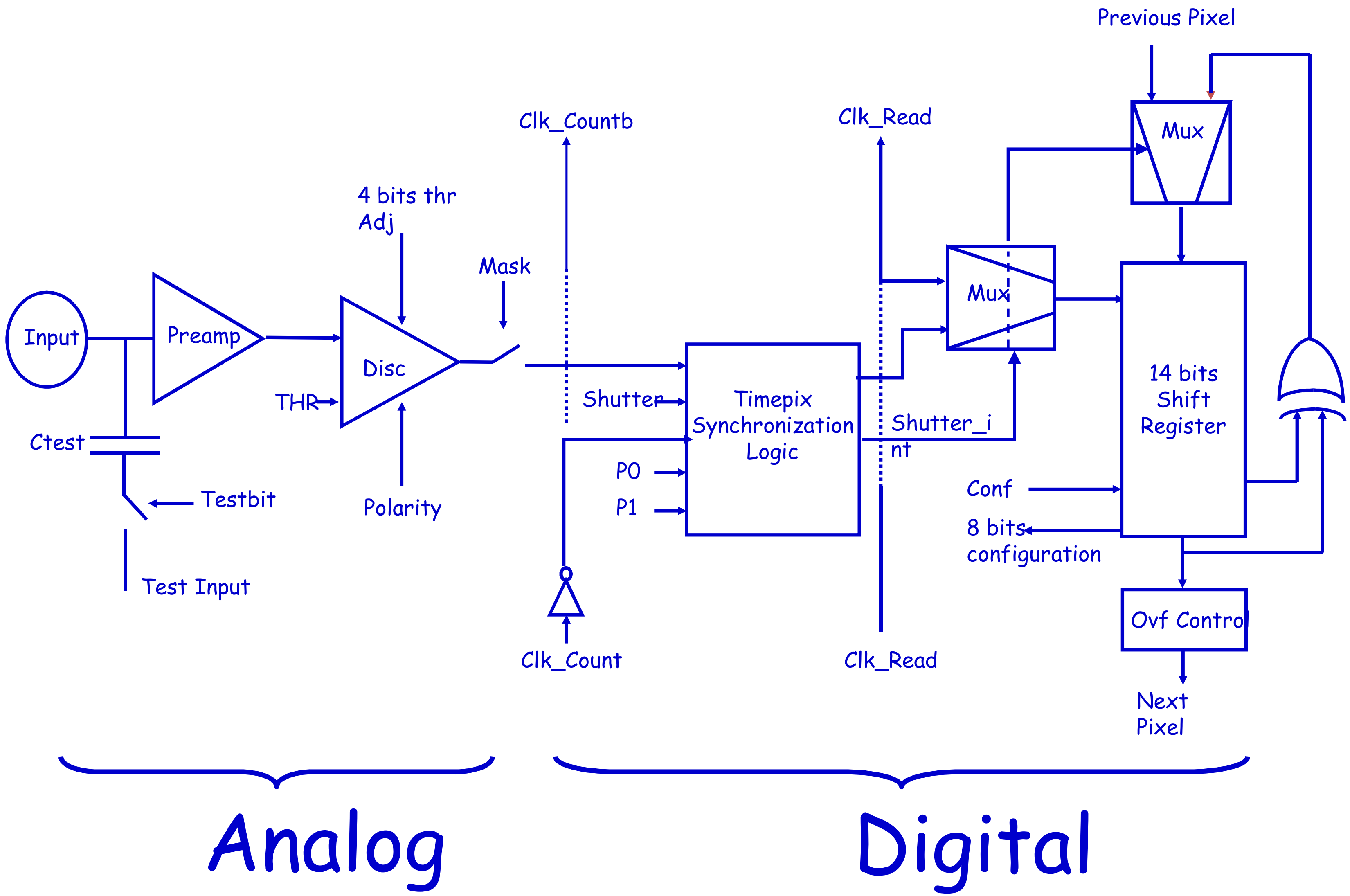
Giovanni Anelli, FEE 2006 Perugia

Jitter

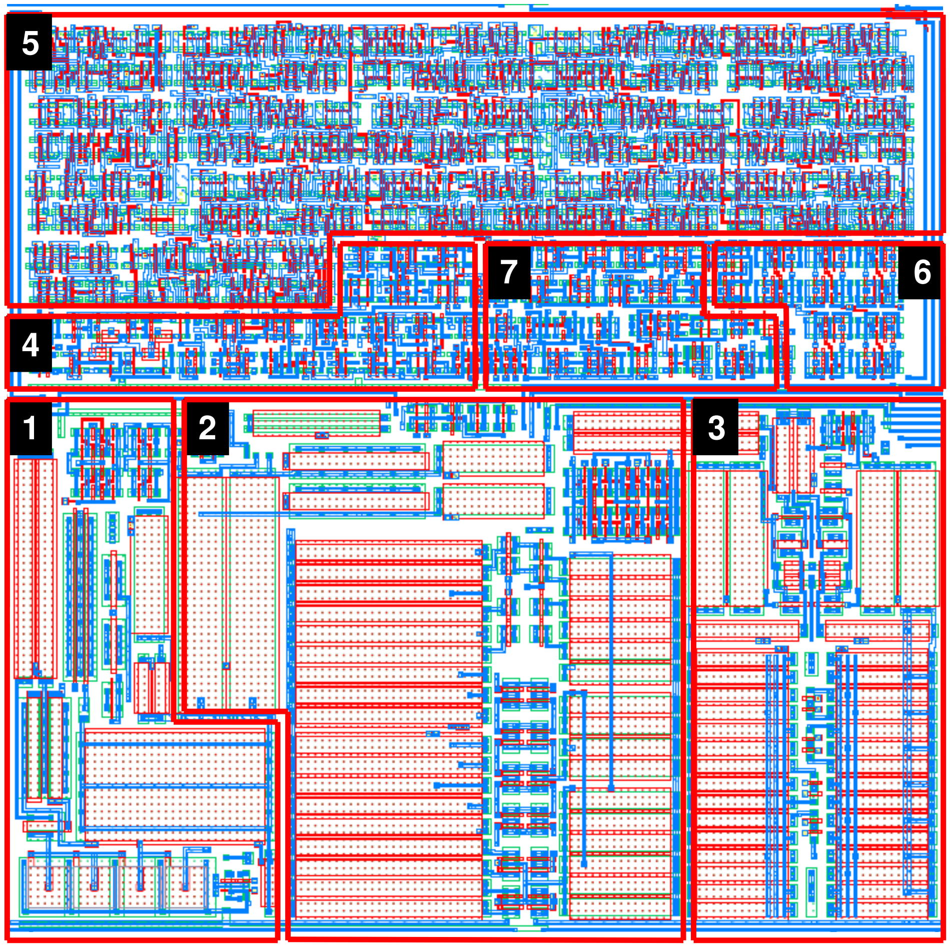
$$Jitter(ns) = \frac{ENC \cdot \tau_s}{Q_{in}}$$



Timepix Pixel Schematic



Area use in Medipix3 pixel



Area pixel: 55x55μm^2

Preamplifier~1/8 pixel surface

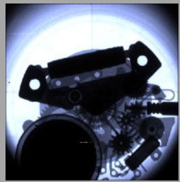
Analog part~30x30μm (if charge summing is not needed)

(130nm IBM CMOS process)

1. **Preamplifier**
2. **Shaper**
3. **Two discriminators with 4-bit threshold adjustment**
4. **Configuration bits**
5. **Arbitration logic for charge allocation**
6. **Control logic**
7. **Configurable counter.**

CLICpix readout architecture

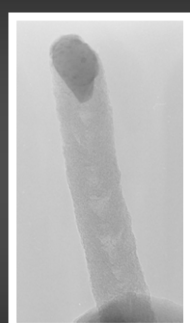
- Pixels 15 μm x 15 μm
- 65nm technology or less
- Matrix 1024 x 1024 pixels
- 1W/cm^2 analog on power (100mW/cm^2 DC)
- Each pixel records bunch number (or multiple thereof)
- Timing precision 10ns or better
- ToT in each pixel
- All data read out at end of train



Assembly

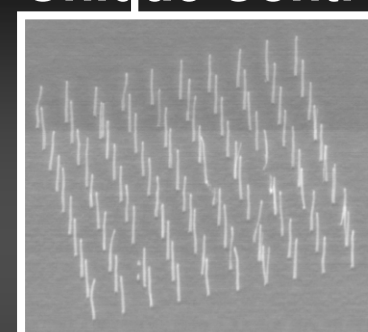
- Hybrid pixel with thinned readout chip (50μm thick) and thin sensor (100μm thick)
- Carbon nanofibre bumps
- Carbon nanofibre heat sink

Carbon Nanofiber*



- Electromigration occurs at $>10^6 A/cm^2$
- 100 % Yield
- diameter of 20-200 nm
- height from 50 nm-3 μm
- Compatible with CMOS-processes

Unique Control



Smoltek's technology enables control of the morphology and properties of carbon nanofibers