Report from WP8

SLHC-PP Steering meeting, Nov 24, 2008
Marc Weber, RAL

- Power distribution is a very active and growing field
- RWTH Aachen is new member of WP8
- Regular informal meetings between WP8 members within ATLAS and CMS, at TWEPP, CERN, etc.
- List of talks
- Deliverables and progress looking rather good

List of talks at ATLAS Nikhef ATU meeting

Power distribution with custom DC-DC converters (F. Faccio)
Plug-In Card with Commercial Buck Converters (S. Dhawan)
DC-DC integrated gain 2 converter (M. Garcia-Sciveres)

Constant Current Source (J. Stastny)
Stave electrical results update (C. Haber)
Serial Powering Architecture (J. Matheson)
Real Time and Slow Control Power Protection for Staves (D. Lynn)
Module Bypass Transistor for Serial Powering (A. Eyering)
Serial Powering Development in Bonn (L. Gonella)

AC Coupled LVDS Drivers (D. Nelson)
HV Power Specifications and Distribution (Y. Unno)

List of WP8 workshop and conference talks

NEWCAS-TAISA 2008, Montreal, Canada

S.Michelis, F.Faccio, P.Jarron and M.Kayal, **Air core inductors study for DC/DC power supply in harsh radiation environment**; S.Michelis, M.Kayal, **Feedback loop conception methodology for step-down continuous switching DC/DC converter**.

TWEPP 2008

B.Allongue, S.Buso, G.Blanchot, F.Faccio, C.Fuentes, P.Mattavelli, S.Michelis , S.Orlandi, G.Spiazzi, **Custom DC-DC converters for distributing power in SLHC trackers**; B. Allongue, F. Anghinolfi, G. Blanchot, F. Faccio, C. Fuentes, S.Michelis, S. Orlandi, A. Toro, **Noise susceptibility measurements of front-end electronics systems**; B. Allongue, G. Blanchot, F. Faccio, C. Fuentes, S. Michelis, M. Perez, **Characterization of the noise properties of DC to DC converters for the sLHC**; S. Michelis, F. Faccio, B. Allongue, G. Blanchot, C. Fuentes, M. Kayal, **A prototype ASIC buck converter for LHC upgrades**; J. Kaplon, F. Anghinolfi, W. Dabrowski, N. Dressnandt, D. La Marra, M. Newcomer, S. Pernecker, K. Poltorak, K. Swientek, **The ABCN front-end chip for ATLAS Inner Detector Upgrade**; K. Klein, L. Feld, R. Jussen, W. Karpinski, J. Merz, J. Sammet, **System test with DC-DC converters for the upgrade of the CMS silicon strip tracker**; P.W. Phillips, G. Villani, M. Weber, R. Holt, C. Haber, **Serial Powering of Silicon Strip Modules for the ATLAS Tracker Upgrade**; M. Karagounis et al., **Development of the ATLAS FE-I4 pixel readout IC for b-layer Upgrade and Super-LHC.**

IPRD08 Siena 2008

G. Villani, **Serial Powering of Silicon Strip Modules for the ATLAS Tracker Upgrade.**

IEEE NSS, Dresden, Germany

M. Weber, C. Haber et al., **Performance of large, serially powered, integrated silicon tracking elements for the SLHC**; L. Feld, **Novel Powering Schemes for SLHC Tracking Detectors**.

Deliverables

Deliverables task 8.1	Description	Nature	Delivery date
8.1.1	Evaluation report on DC-DC conversion technologies	R	M12
8.1.2	Prototypes and viability report	P, R	M30
8.1.3	Integration in full-scale detector modules	D	M36

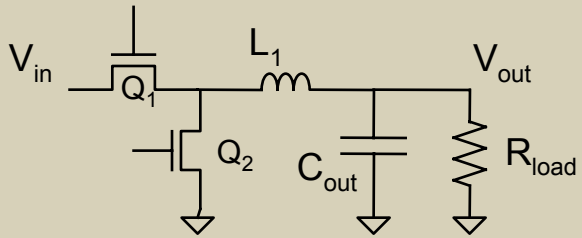
Deliverables task 8. 2	Description	Nature	Delivery date
8.2.1	Evaluation report on generic serial powering studies and specification of serial powering components	R	M12
8.2.2	Custom serial powering circuitry and evaluation of generic high-current serial powering ASIC	P,R	M24
8.2.3	Full-scale super-module with custom serial powering circuitry	D	M36

First deliverables in M12. We are in good shape. For illustration a few slides with results below.

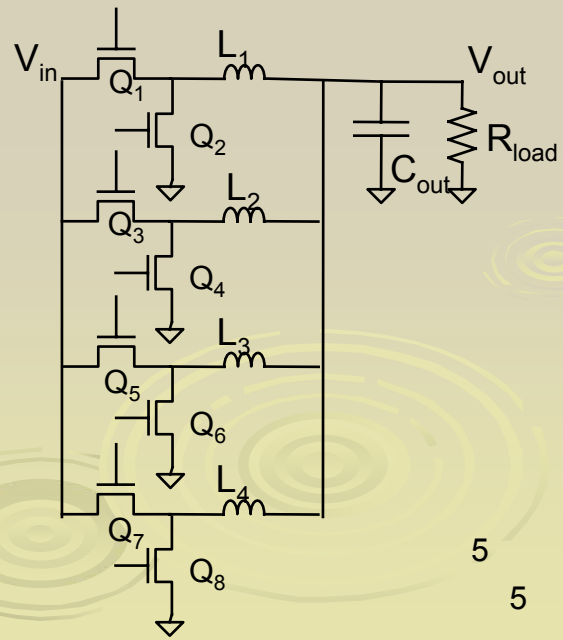
Different converter topologies (1/3)

The following DC/DC step down converter topologies have been evaluated and compared in view of our specific application.

1. **Single phase synchronous buck converter**
   - ↑ Simple, small number of passive components
   - ↓ Larger output ripple for same C_{out}
   - ↓ RMS current limitation for inductor are output capacitance



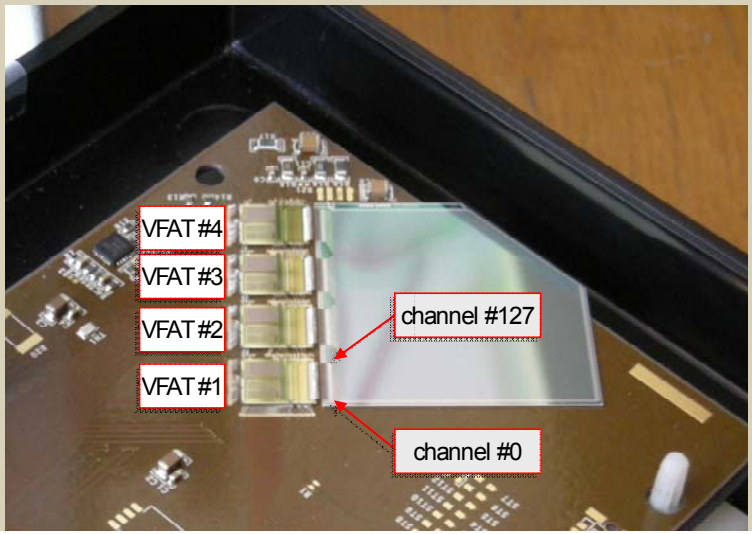
2. **4 phase interleaved synchronous buck converter**
   - ↑ Complete cancellation of output ripple for a conversion ratio of 4 (with small C_{out})
   - ↑ Smaller current in each inductor (compatible with available commercial inductors)
   - ↓ Large number of passive components
   - ↓ More complex control circuitry



Powering a detector module

TOTEM Front-End system supplied with DC-DC converters

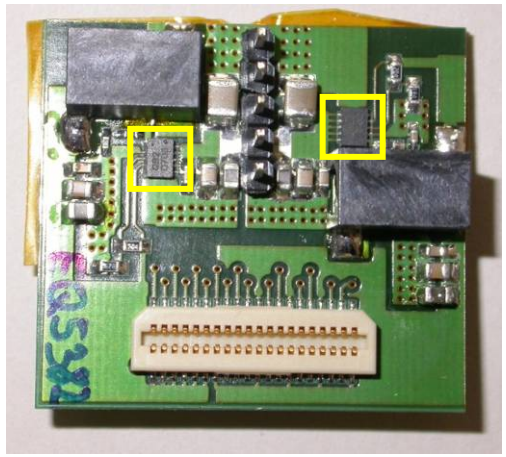
Expose the front-end system to the DC-DC converter conducted noise (Common Mode and Differential Mode currents)

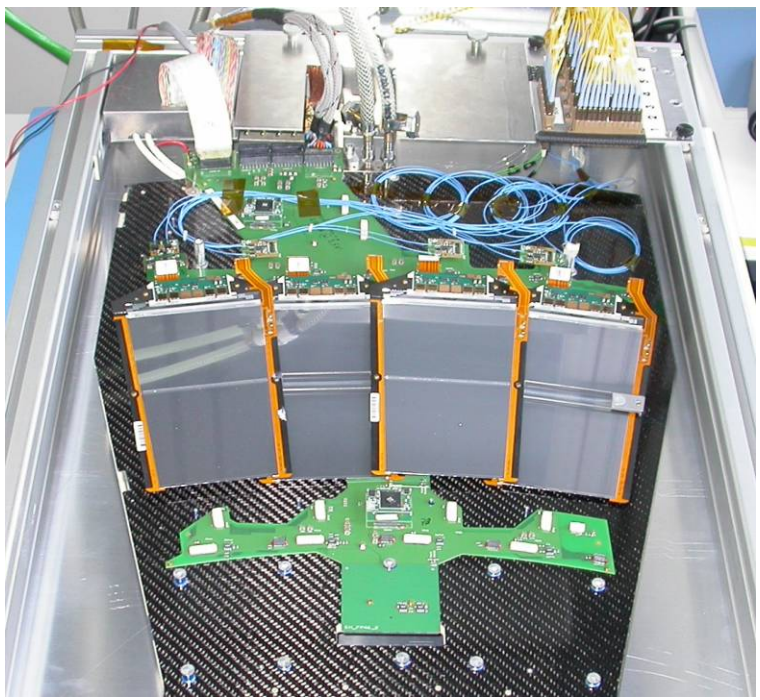


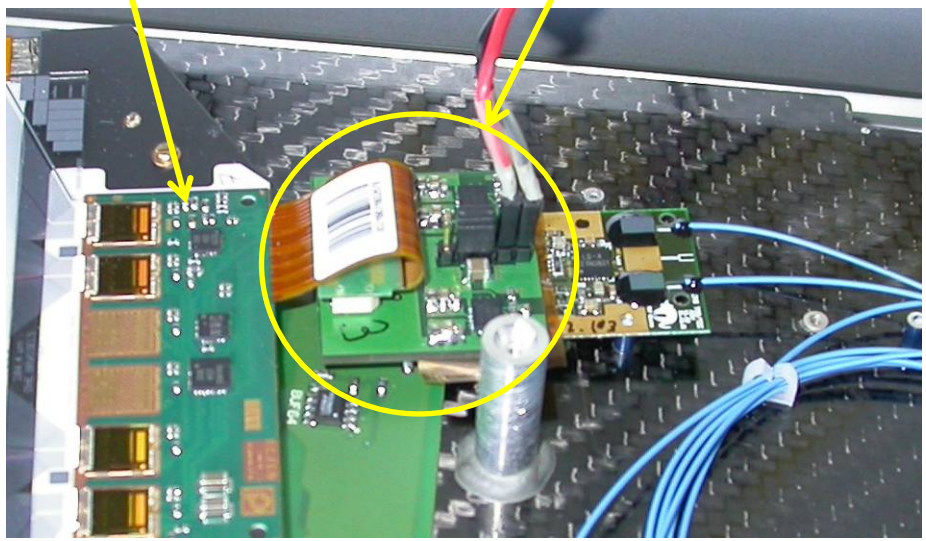
	Nominal noise	Proto #3 with long cables	Proto #3	Proto #4
VFAT #1	1.76	1.76	2.00	1.81
VFAT #2	1.81	1.73	2.00	1.77
VFAT #3	1.68	1.62	1.69	1.55
VFAT #4	1.56	1.59	1.93	1.67

System Test with commercial buck converters at Aachen

- Selected device**: Enpirion EN5312QI**
  - Small footprint: 5mm x 4mm x 1.1mm
  - $f_s \approx 4$ MHz
  - V_{in} = 2.4V – 5.5V (rec.) / 7.0V (max.)
  - I_{out} = 1A
  - Integrated ferrite inductor or external air-core coil
- Two chips integrated on PCB provide APV supply voltages
- System test set-up: end cap substructure with 4 strip modules

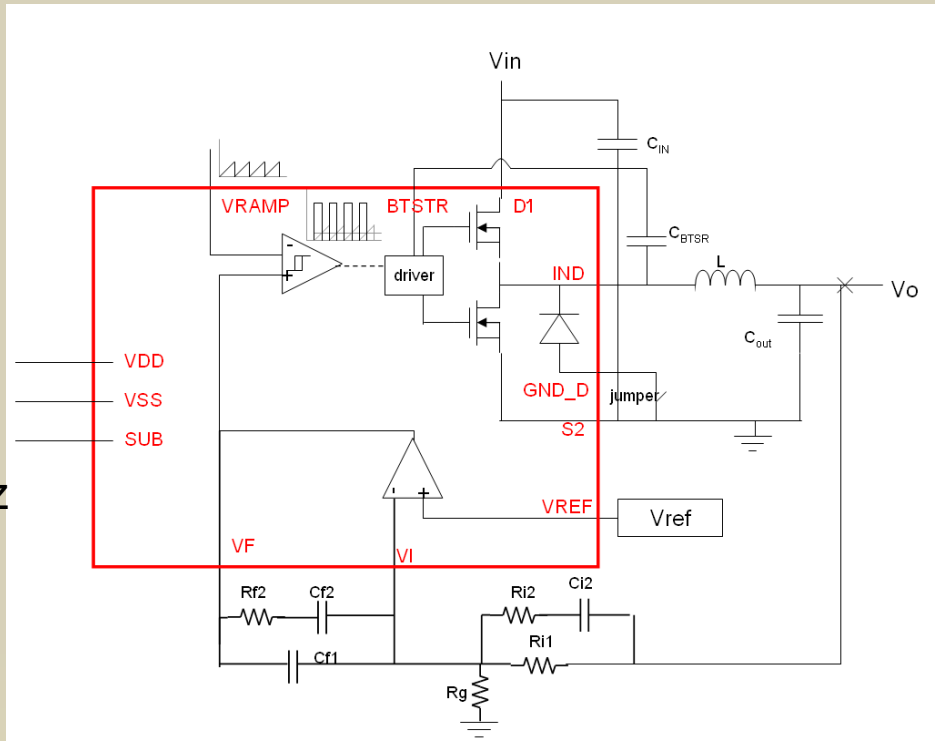


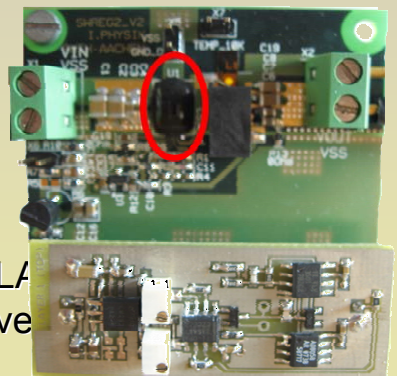


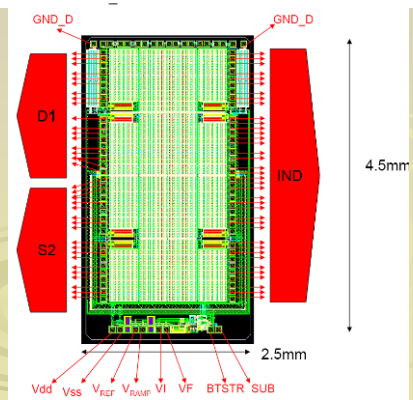


ASIC development

- Prototype for “conversion stage 1”
- First prototype designed and manufactured in AMIS I3T80 technology
- Simple buck topology
  - V_{in} up to 10V
  - V_{out}=2.5V
  - I_{out} up to 1.5A
  - switching frequency 0.3-1.2 MHz
- ASIC included main functions only (switches, control circuitry)
- External compensation network, reference voltage and sawtooth generator required



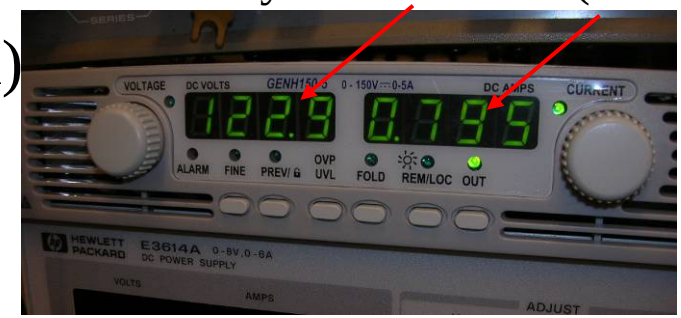




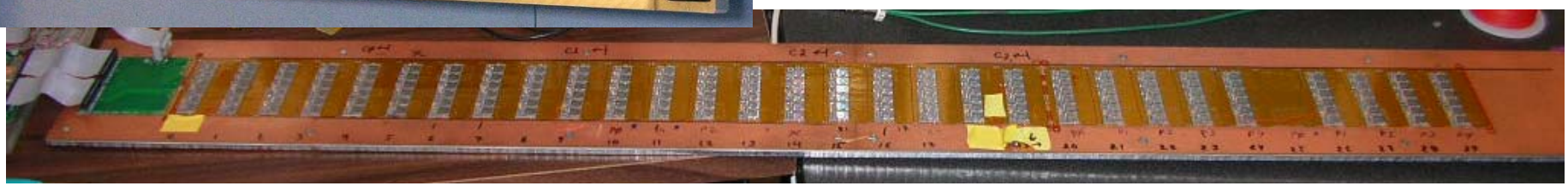
System tests with commercial components: serial powering

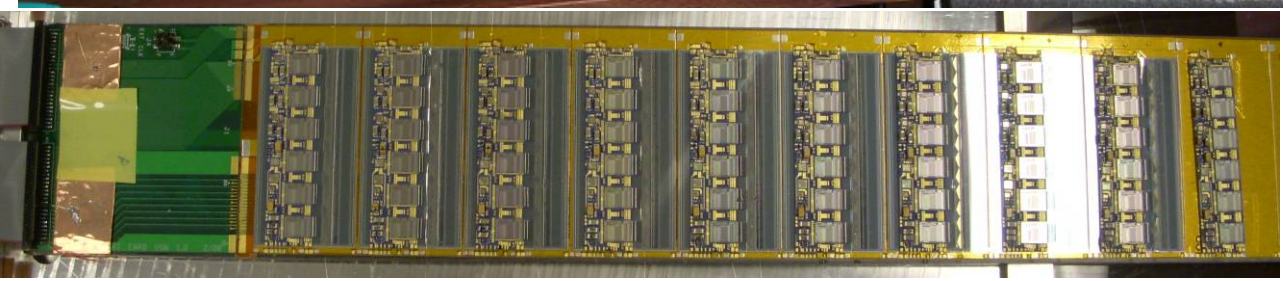
1) Pixel stave with FE-I3 (old, published)
2) 6 SCT modules in series with ABCD (old)
3) 6 module stave with ABCD
4) 30 module stave test vehicle and stave

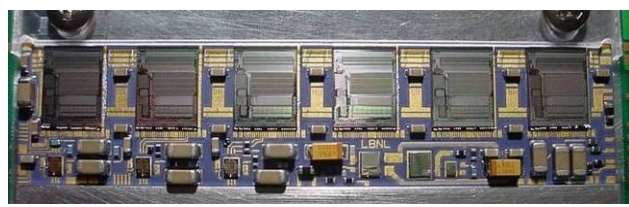
4 V x 30 hybrids = 120 V (0.8 A)



In future: 1.5 V x 20 hybrids = 30 V



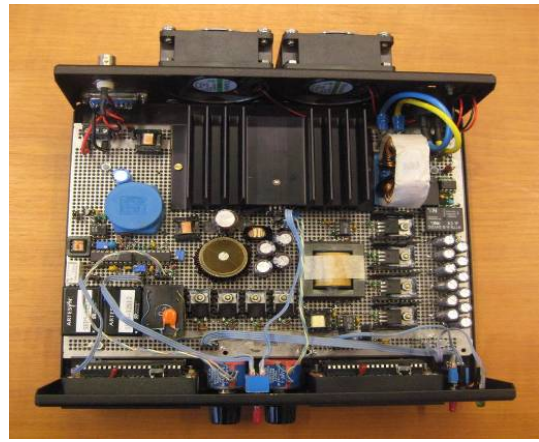




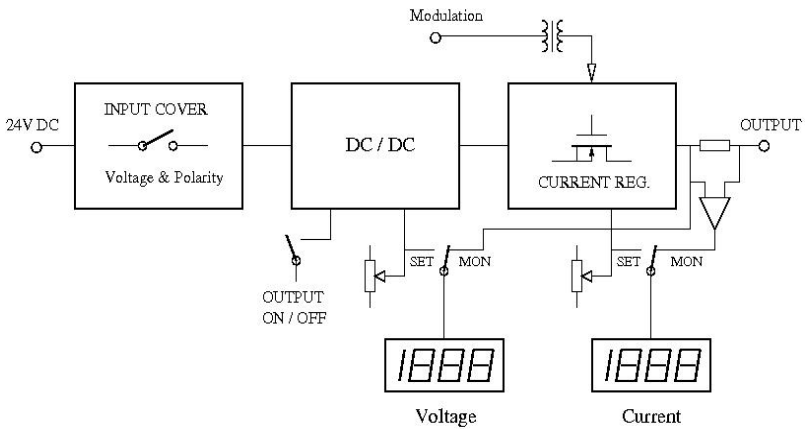
Electrical performance is excellent in all tests. Multi-drop AC- LVDS coupling is working (thanks to Dave Nelson)

Custom Constant-current source (ASCR, RAL)

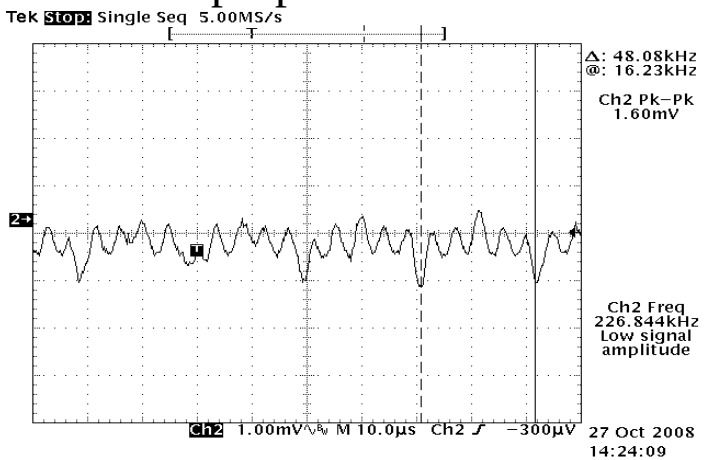
First prototype designed by Jan Stastny (ASCR)
Functional and encouraging performance. Second prototype will be good enough to drive stave safely



Current Source Block Diagram



ΔI=16mA pk-pk for load 2.2A / 4V



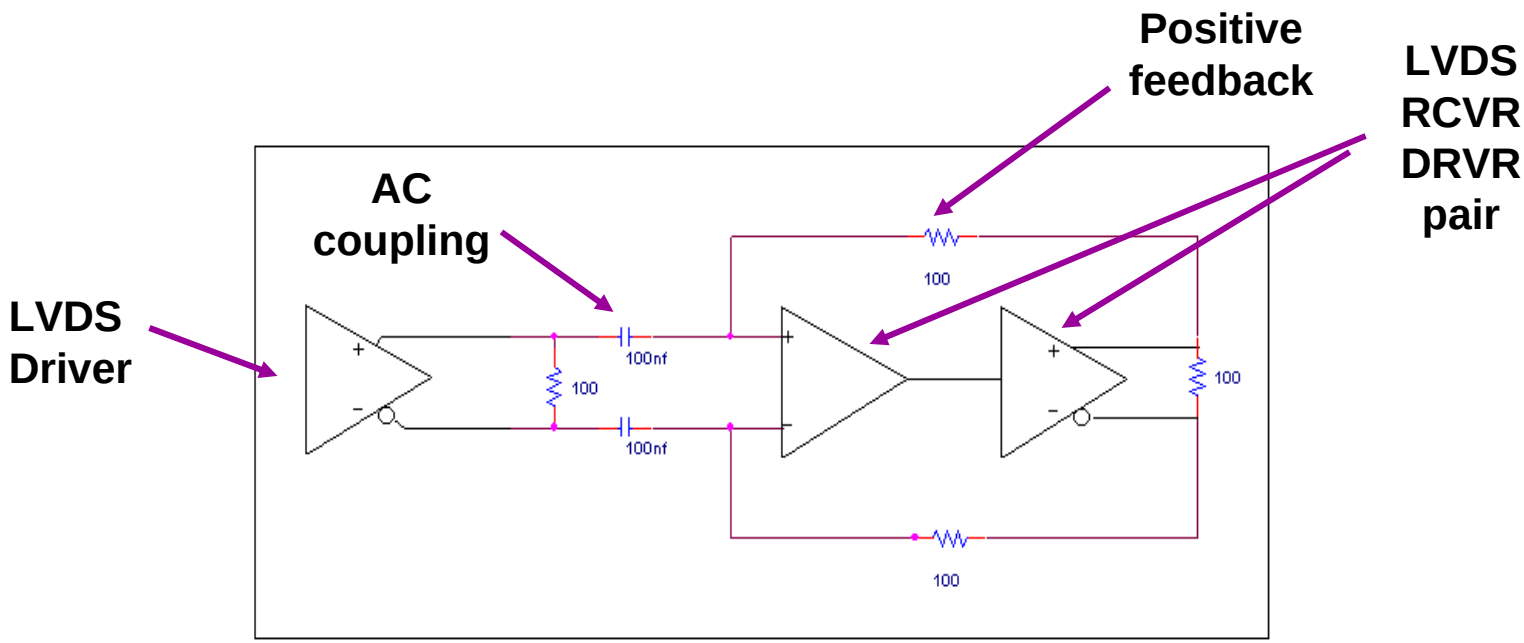
Attractive engineering challenge. Two feed-back loops: one for current control, one for voltage.

Q&A:

Do we need custom constant current source? Yes, there are no commercial devices.
Should we have a commercial partner? Could be considered, but not yet.

Example of AC Coupled LVDS Driver

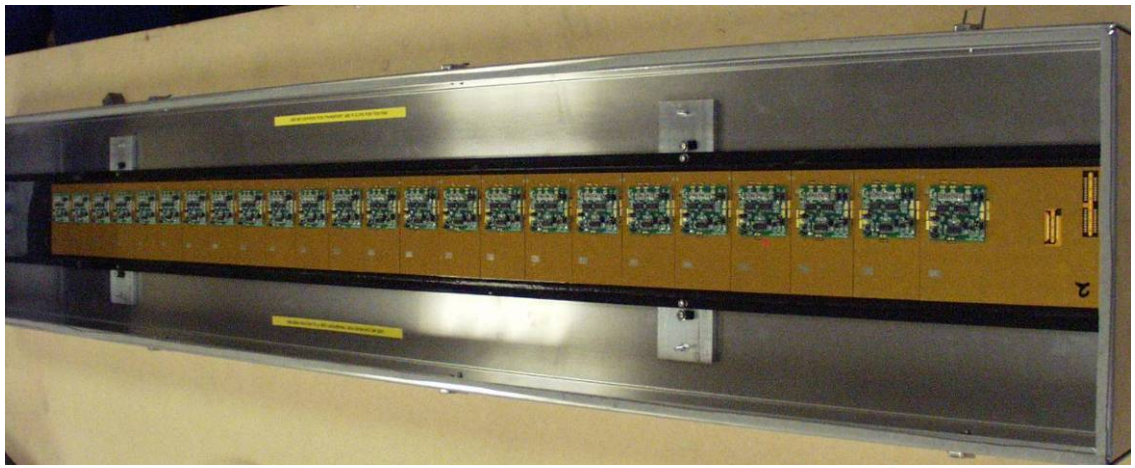
- The AC Coupled LVDS driver is actually an AC coupled latch.
  - This circuit doesn't need DC Balance.
- There are some problems & suggested fixes that will be presents in later slides

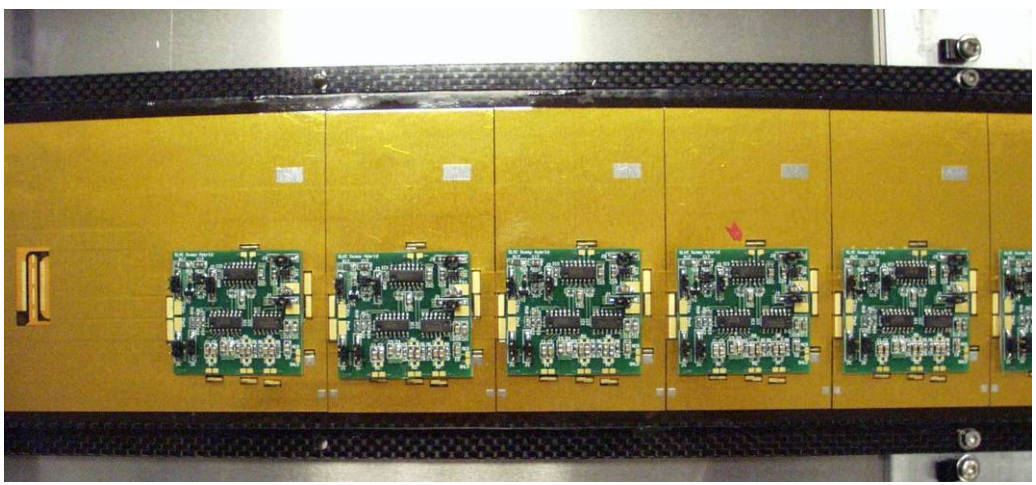


More studies to come on AC LVDS coupling

Test structure built at RAL. Design Liverpool and Oxford, tests Oxford.

Similar studies and many results elsewhere





Custom IC for Serial powering

1) ABC_Next shunt regulator and transistors (Cracow; ATLAS strips)
2) SPi (generic serial powering interface) (FNAL, Penn, RAL)

These two chips will enable us to test 3 SP architectures. SPi will also be useful for multi-drop transmission line studies. ABC_Next is being tested, SPi delivery is expected within two weeks.

3) FE-I4 shunt regulator and transistors (Bonn, ATLAS pixels)

FE-I3 custom circuitry provided proof of principle of serial powering for pixels *(Nucl. Instr. Meth. A557 (2006) 445-459)*

Also LVDS receivers and in future custom protection circuitry

Q&A:

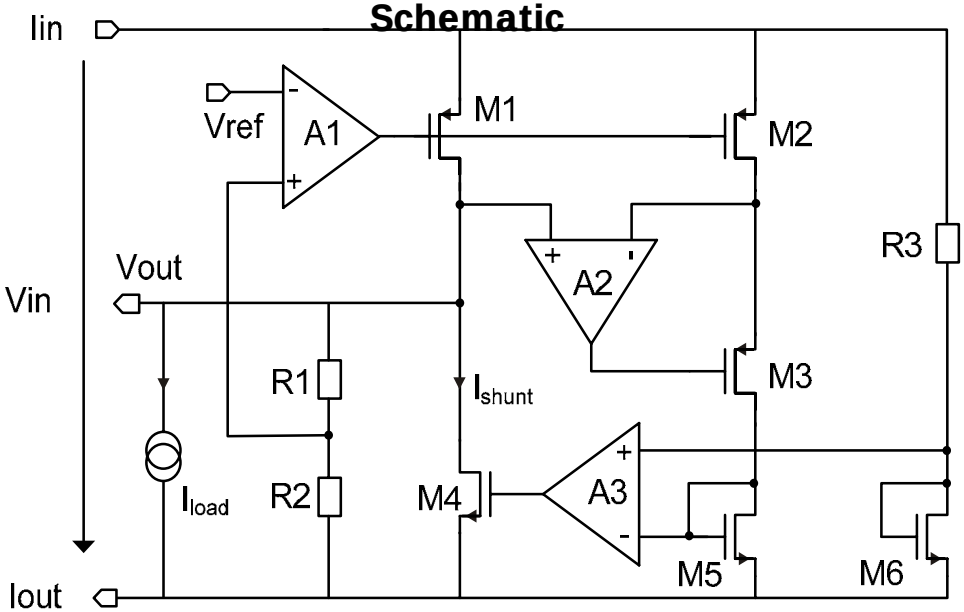
Why not take commercial devices? There are none

What are the three SP architectures? See appendix slides.

Why investigate all three architectures ? It just happened, exploits synergy between SLHC and ILC and requires only two ICs. Can not discriminate "on paper"

LDO Regulator with Shunt Transistor (ShuLDO)

Simplified Schematic

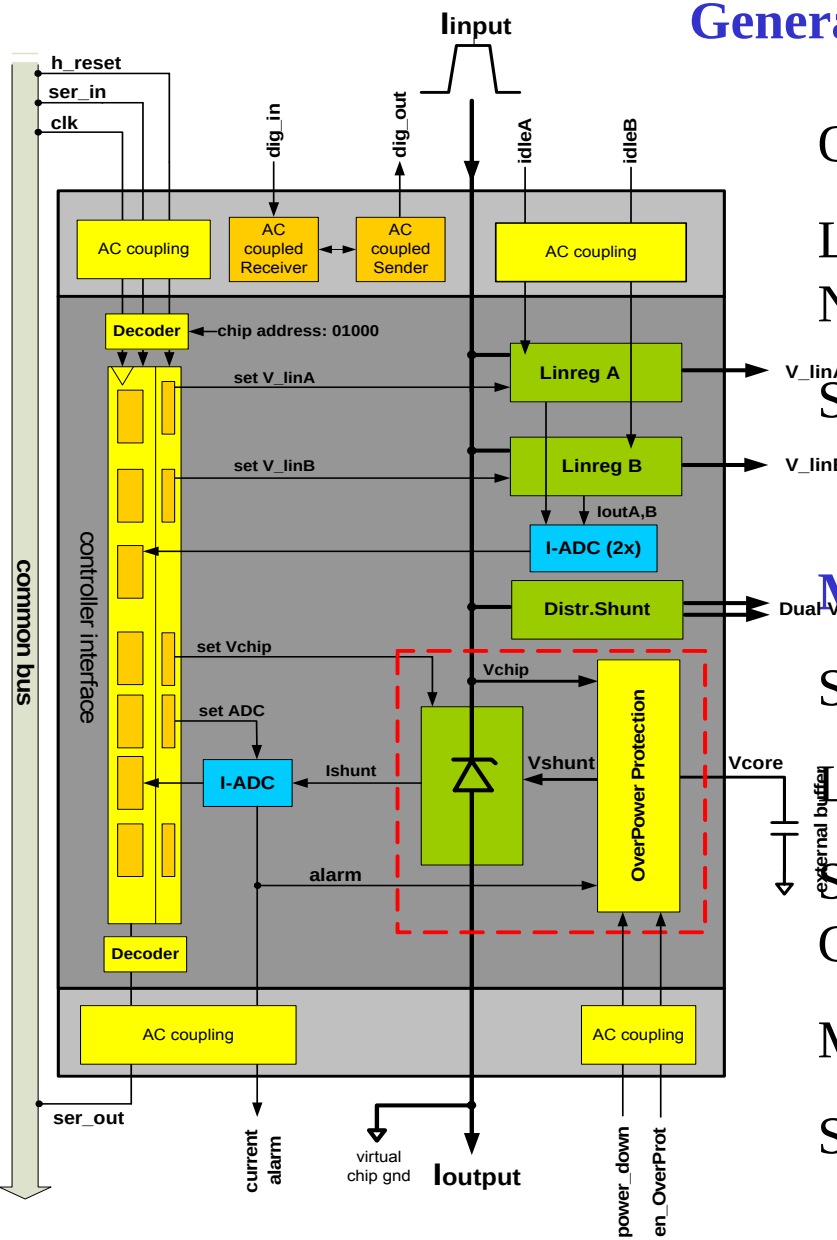


- Combination of LDO and shunt transistor
- M4 shunts the current not drawn by the load
- Fraction of M1 current is mirrored & drained into M5
- Amplifier A2 & M3 improve mirroring accuracy
- Ref. current defined by resistor R3 & drained into M6
- Comparison of M5 and ref. current leads to constant current flow in M1
- Ref. current depends on voltage drop V_{Iin} which again depends on supply current Iin

- „Shunt-LDO“ regulators having completely different output voltages can be placed in parallel without any problem regarding mismatch & shunt current distribution
- Resistor R3 mismatch will lead to some variation of shunt current but will not destroy the regulator
- „Shunt-LDO“ can cope with an increased supply current if one FE-I4 does not contribute to shunt current e.g. disconnected wirebond → ref current goes up
- Can be used as an ordinary LDO when shunt is disabled

SPi chip

General purpose SP interface



Overall layout and design: Marcel Trimpl, FNAL

LVDS comports and stand-alone SR: Mitch Newcomer and Nandor Dressnandt, Penn

Specification and KE: Giulio Villani, RAL

Main blocks and features:

Shunt regulator(s) and shunt transistors;

LVDS buffers; over current protection;

Shunt current sensing ADC; TSMC 0.25µm CMOS with almost rad-hard layout;

Max. shunt current: 1 A design, “expected” >3 A;

Size: ~ 14 mm^2; flip-chip

Appendix

Description of work

Task 8.1: DC-DC conversion

The development aims for radiation-hard components operating in magnetic fields up to 4 Tesla. The following alternative solutions will be explored: buck converters based on air core inductors and on-chip conversion for small current applications.

The R&D program shall be structured as follows:

"Evaluation phase"

An evaluation of different conversion approaches will be made, singling out the critical difficulties and developing conceptual solutions to overcome them. Exploration of partnerships with industry. Commercially available air-core converters (while not being radiation-hard) will be used to study the behaviour and characteristics of detector systems powered through DC-DC conversion. This will include studies on the electromagnetic interference between the converters and the sensors with their read-out electronics

"Prototype phase"

Development of custom prototype converters for the alternative solutions. Although this generation of prototypes are intended to be demonstrators only, the air-core inductor converter will have the same level of integration as the final product. All active components will be embedded in ASICs and the number of passive components shall be minimized to be compatible with the real application. The on-chip DC-DC converter, integrated in modern CMOS technologies, will also be prototyped to assess the feasibility of this solution. Prototypes will be integrated in detector modules multi-module structures and be tested at the system level. A report will detail the performance of the prototypes, with conclusions on the final viability of each conversion approach and recommendation for LHC upgrades.

CERN will play the major role in the inductor-based converter development, with contributions from RWTH Aachen in device testing and integration and contributions from STFC and RWTH Aachen in the system-level testing. PSI will be in charge of the evaluation and first prototyping of the on-chip DC-DC conversion.

Task 8.2: Serial Powering

Serial powering is a novel and highly promising concept for power distribution in silicon particle detectors. It involves a constant current source feeding a chain of silicon strip or pixel modules combined with shunt and linear voltage regulators on the module. This reduces the number of cables, minimizes the total current brought into the detector volume and therefore the power losses in the cables.

In serial powering schemes, each module sits at a different potential; thus control, clock and data signals must be AC-coupled or use optical signal transmission. Apart from the challenges of designing radiation-hard power electronics, serial powering systems require the development of over-current protection and redundancy schemes and exploration of grounding and shielding techniques.

The serial powering R&D programme consists of three phases:

" Generic studies"

Specification and development of AC-coupling or opto-decoupling elements; investigation of grounding and shielding techniques for serial powering schemes; system evaluation of serial powering systems based on commercial shunt regulators.

"Development of custom radiation-hard power electronics"

Design, submission and characterization of custom radiation-hard shunt regulators, power devices and AC–coupling circuitry. Several design iterations in different technologies are foreseen. The concept of a generic high-current serial powering ASIC, with various protection and slow-control features, capable of powering S-ATLAS and CMS2 pixel and strip detectors, will be evaluated.

"System design and characterization of super-modules"

Implementation of custom electronics in tracking detector super-modules. A super-module will consist of a significant number of detector modules powered in series. The super-module performance will be fully characterized.

AGH-UST, RAL and UBONN will be responsible for this task. AGH-UST will contribute predominantly to the design of the radiation-hard electronics. STFC and UBONN will work on all sub-tasks.

Implementation example