Thin n-in-p planar pixel sensor productions at MPP

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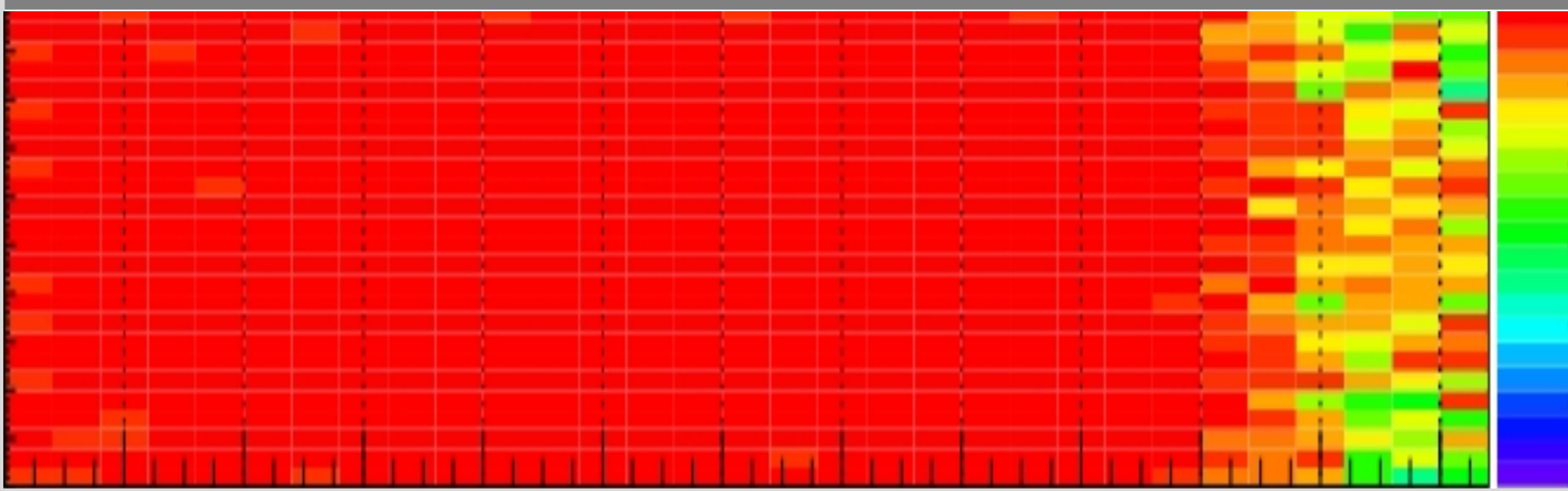
(Werner-Heisenberg-Institut)

27th RD50 Workshop, CERN
December 2nd-4th 2015



Overview

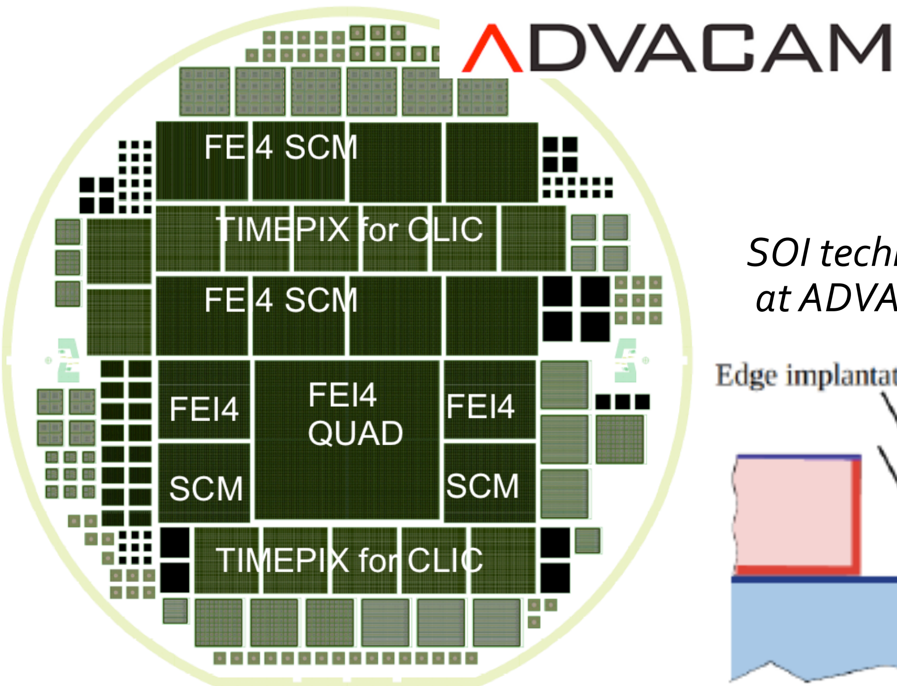
- **New ADVACAM production for thin n-in-p planar pixels sensors with active edges**
  i. sensor thicknesses: 50, 100 and 150 μm
- **Test-beam studies with n-in-p planar pixels in (un-) irradiated modules**
  i. with different implementations of punch-through designs
  ii. with 25x500 μm^2 pitch pixels with external punch-through structure
- **Grazing angle studies with n-in-p planar pixels**
  i. (un-) irradiated module at high Φ (80° incidence angle (η~2.4))

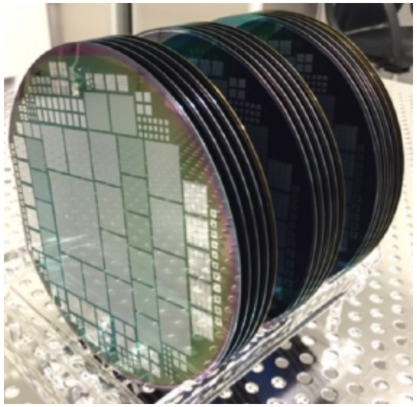
New ADVACAM production

ADVACAM Production

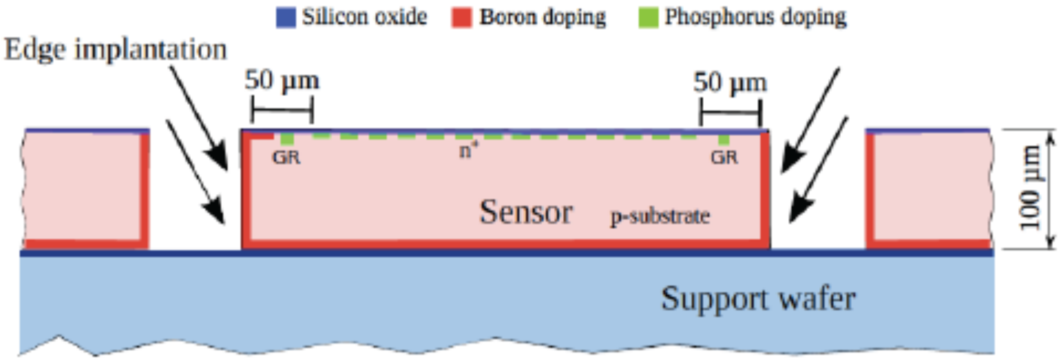
- Second production of active edge pixels at ADVACAM
- 15 6" wafers on p-type FZ material
- Thickness 50, 100 and 150 µm

- In collaboration with Glasgow, Göttingen, LAL, CLIC CERN-LCD and Geneva University for medical applications





SOI technology with active edges at ADVACAM

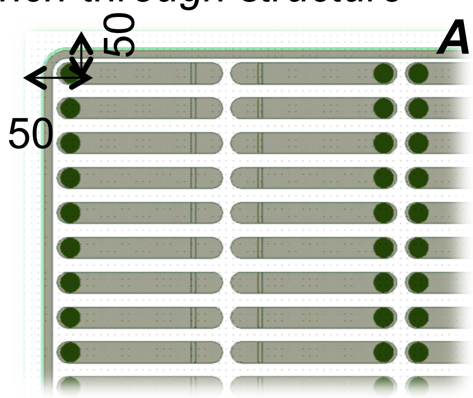


RD50 project: 2014/03

Different structures of bias ring and punch-through

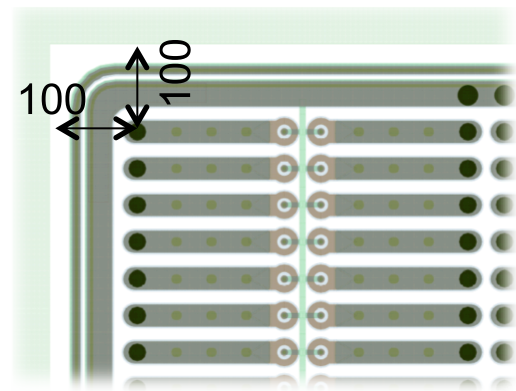
FE-I4 with
50 µm edge,
one GR,
no punch-through structure

Active edge



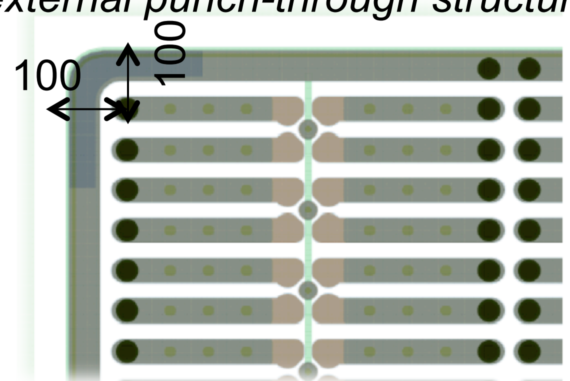
100 µm edge,
Bias Ring + Guard Ring,
std punch-through structure

Slim edge



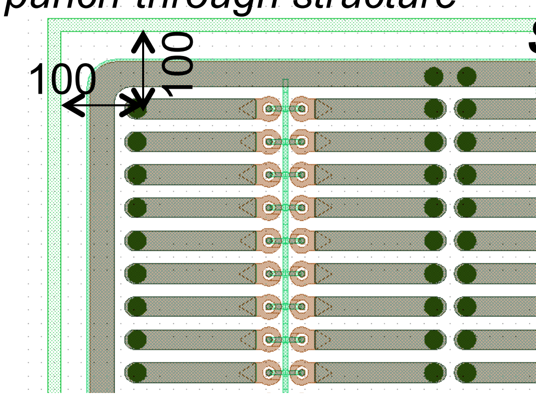
100 µm edge,
Bias Ring,
new external punch-through structure

Slim edge



100 µm edge,
Bias Ring,
std punch-through structure

Slim edge



Measurements of slim edge sensors of different thickness

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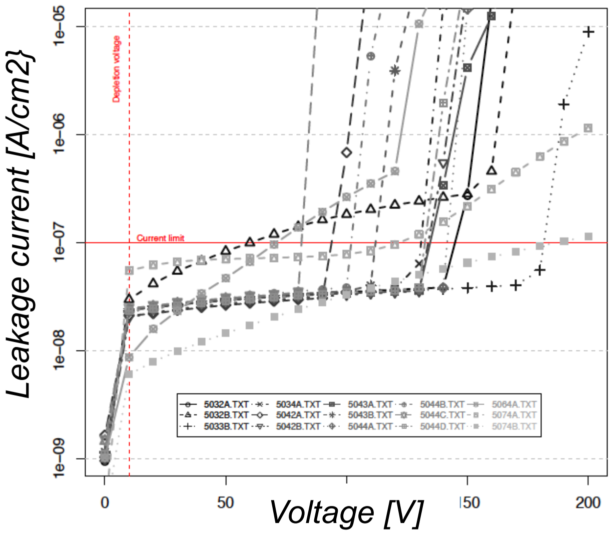
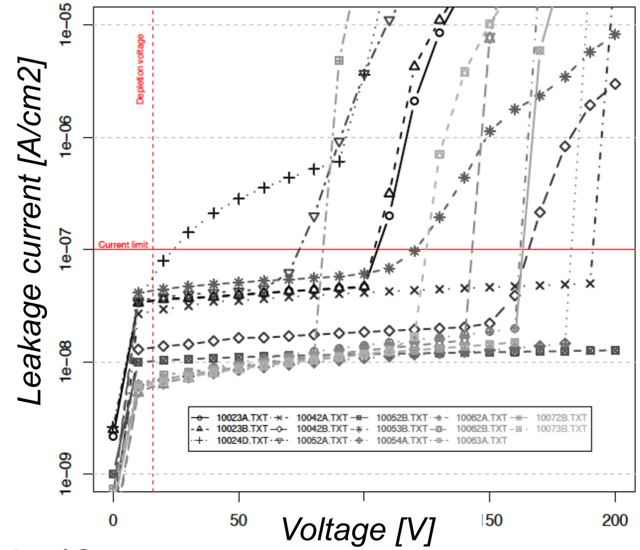
FE-I4 sensors, 50 µm thickness

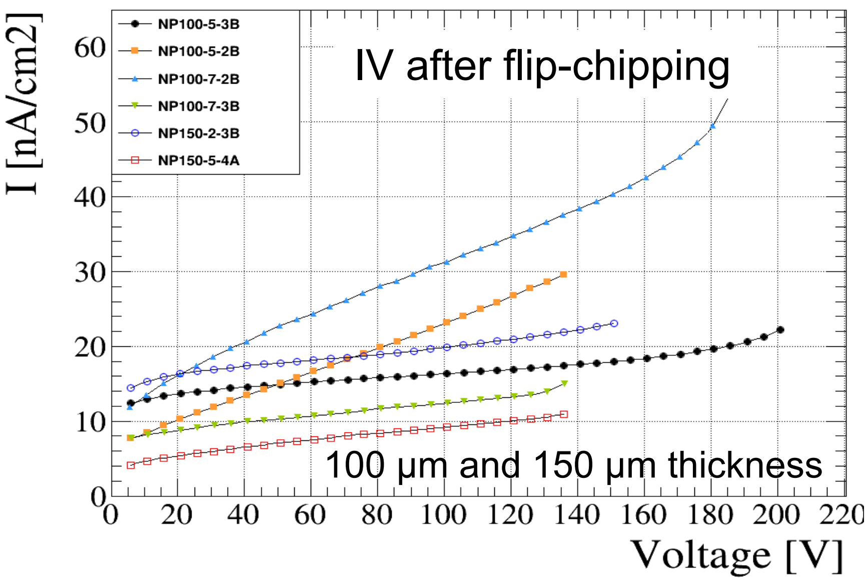


- Inactive edge = 100 µm
- V_{depl} ~10 V for d=50 µm
- V_{depl} ~ 15 V for d=100 µm
- IV measured on bare FE-I4 sensors with 100 µm edge at ADVACAM

ADVACAM

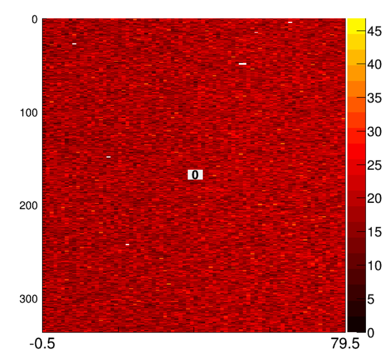
FE-I4 sensors,100 µm thickness





- Modules with Au/Cu UBM showed best performance
- Plan production of several other modules in addition with
  - i. 50 µm thick sensors
  - ii. active edge sensors

Cadmium scan

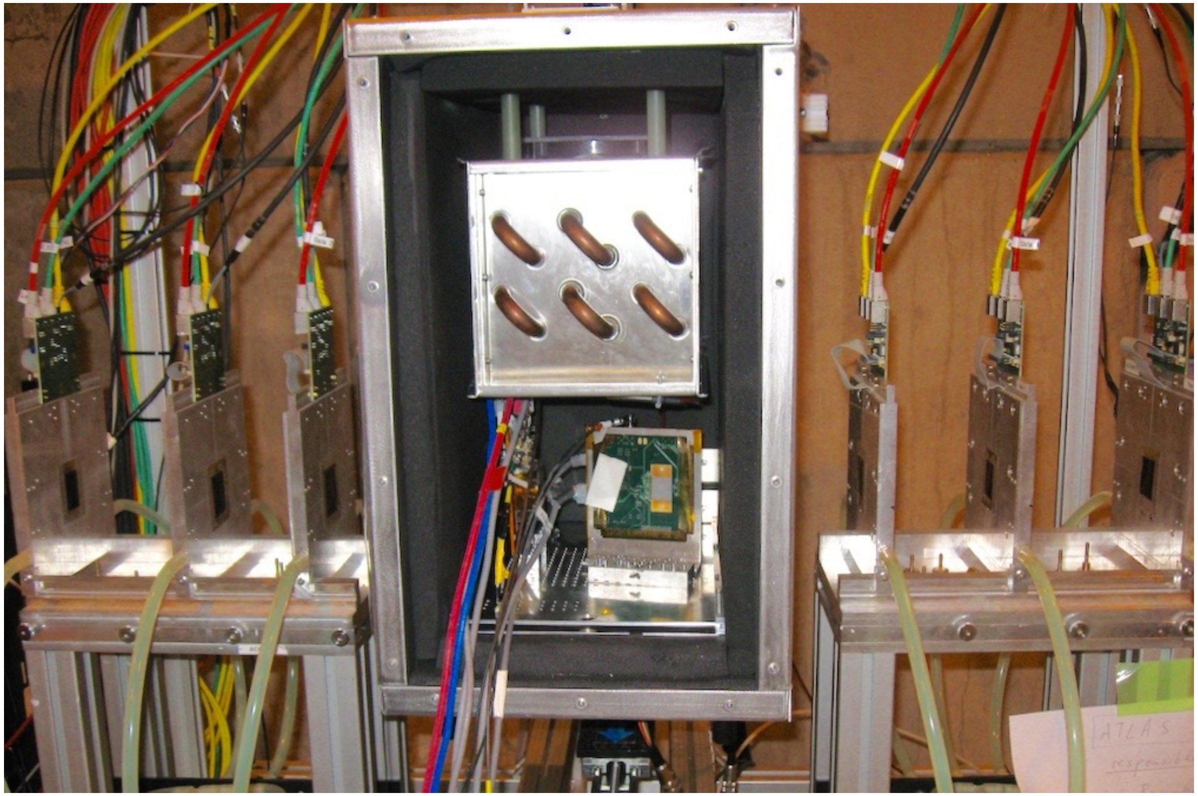


Optimization of different punch-through designs

Test-beam studies of different sensor designs

Test beam set-up of ITK test-beam July 2015

ACONITE telescope of the AIDA/EUDET family

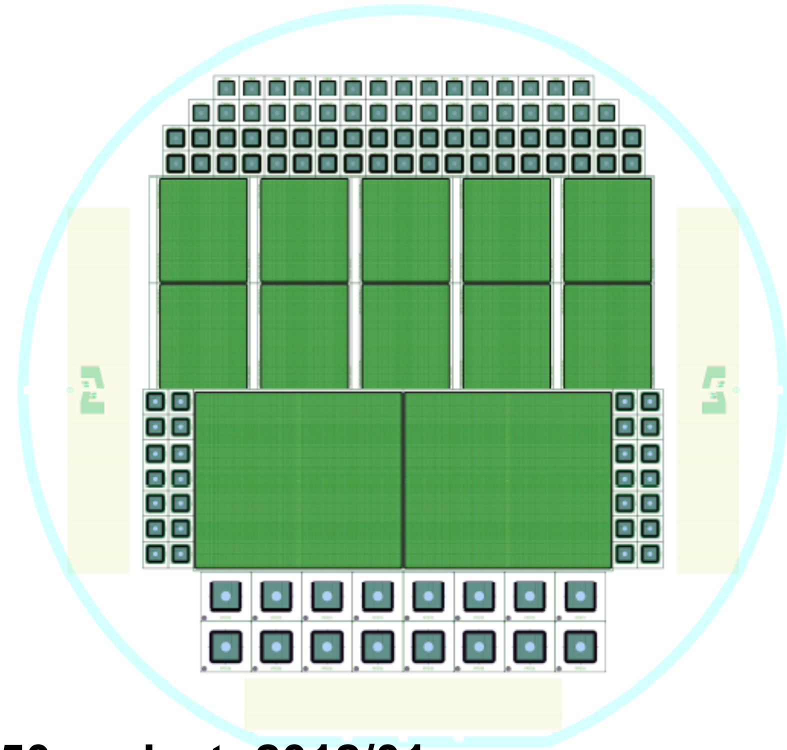


Data analysis sequence

- Test-beam at CERN with 120 GeV protons
- Track reconstruction done with EUTelescope software
- Track analysis done with Tbmon2

CIS3 Production

- First 6'' production at CiS
- 6'' wafers on p-type FZ material
- Thickness : 265 - 270 µm



RD50 project: 2012/01

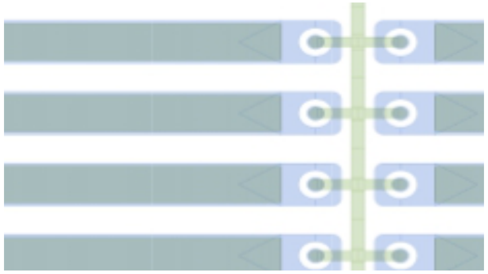
- **CiS3** standard FE-I4 pitch with modified punch-through structures
  - Pixel size : 50x250 µm²
  - Pixel matrix : 80x336

- **CiS3** modified FE-I4 with 25 µm r-Φ pitch
  - Pixel size : 25x500 µm²
  - Pixel matrix : 40x672

Different punch-through designs

50x250 µm² pixel pitch

Standard punch-through



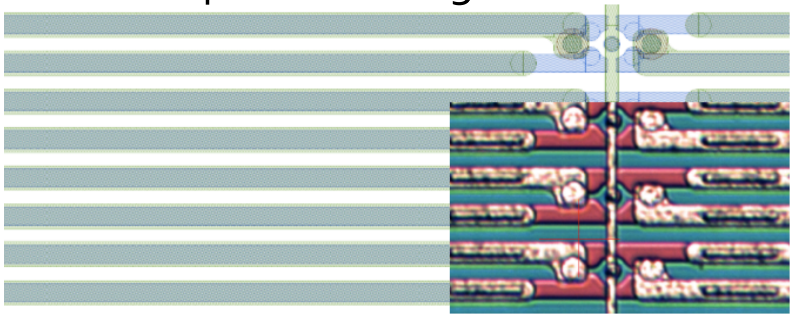
Bias line over punch-through dot

Bias line over center of pixel implant

individual p-t

25x500 µm² pixel pitch

Common punch-through

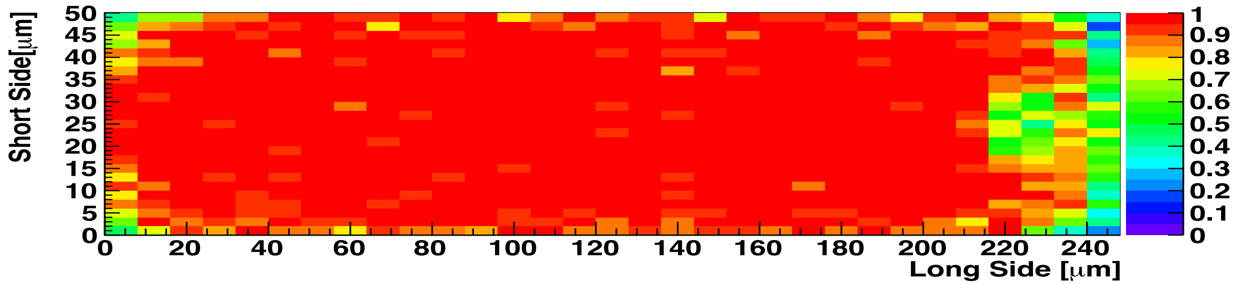


combined p-t

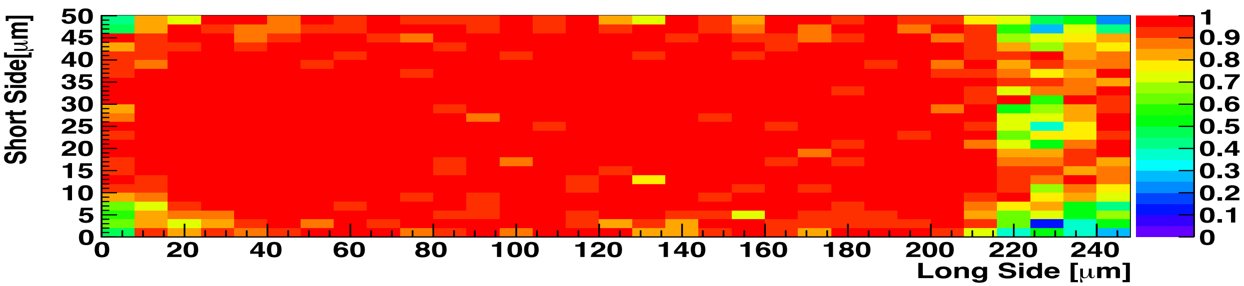
Different punch-through designs- in-pixel hit efficiency

- **Irradiated at 5 ·10^{15} n_{eq}/cm^2, U=500 V**

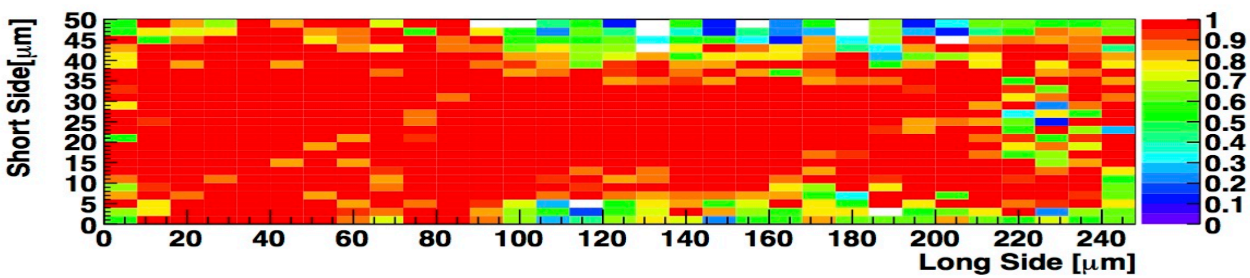
100 % hit efficiency before irradiation



Standard punch-through



Bias line over punch-through dot



Bias line over center of pixel implant

Third design less efficient due to horizontal bias rail between pixels

Novel punch-through design for 25x500 µm pitch

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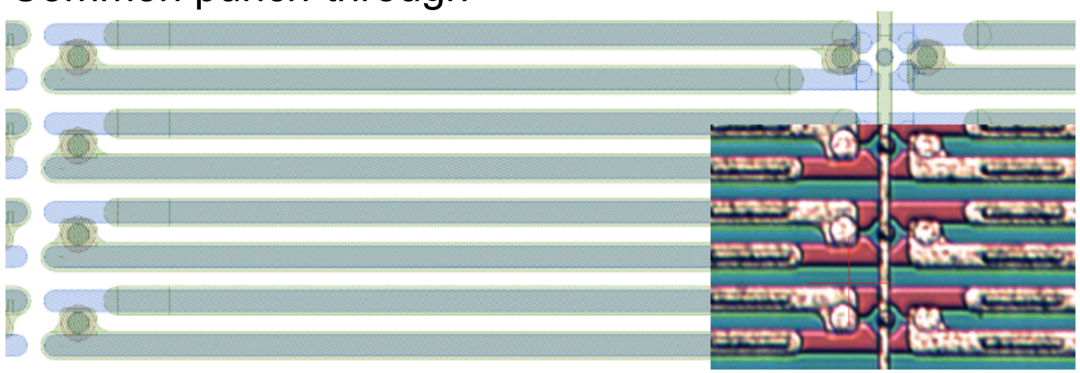
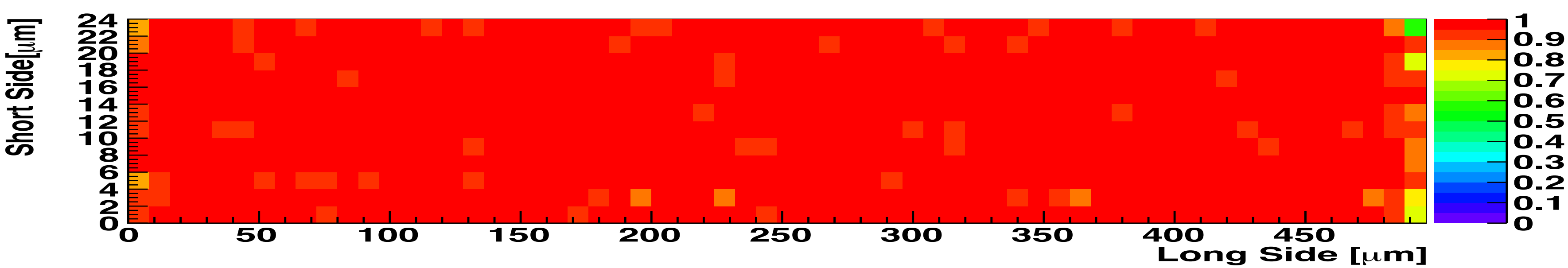
- In-pixel hit efficieny of irradiated CiS3 at 5 $\cdot 10^{15}$ n_{eq}/cm^2 Module with common punch through structure for 4 pixels
- Efficiency obtained at highest voltage (800 V) : **98.0 ± 0.3 %**

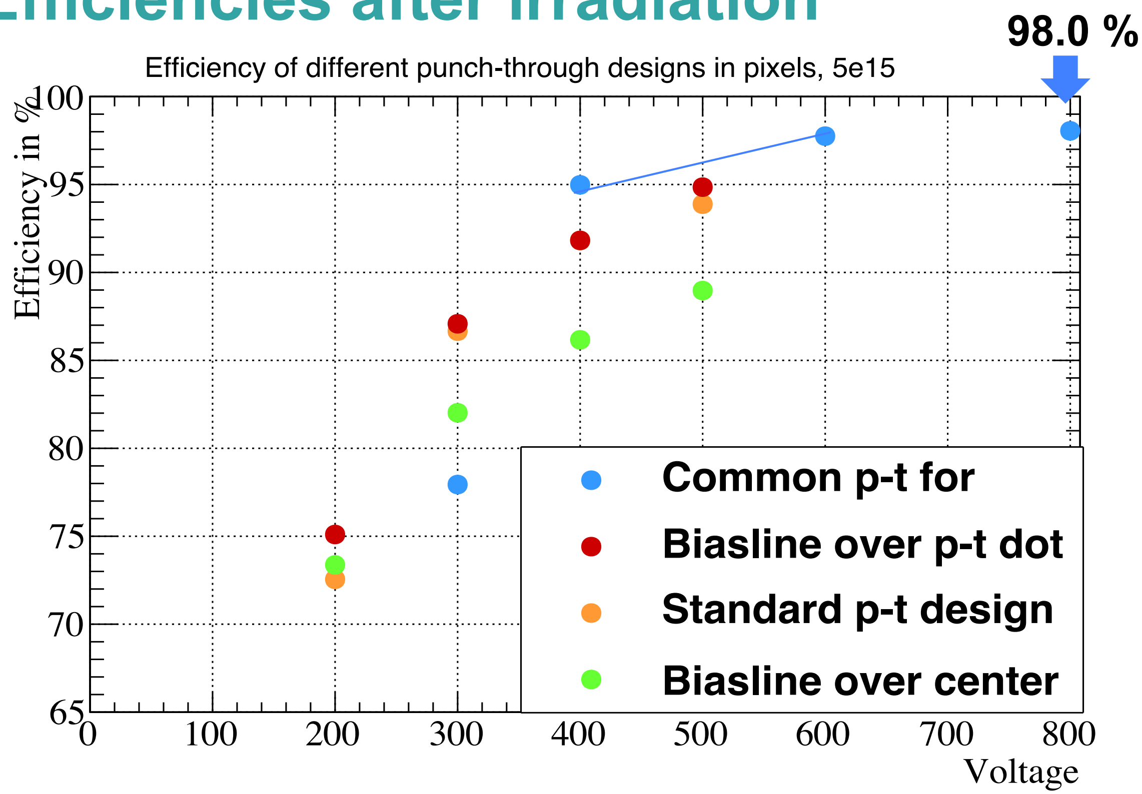
Common punch-through

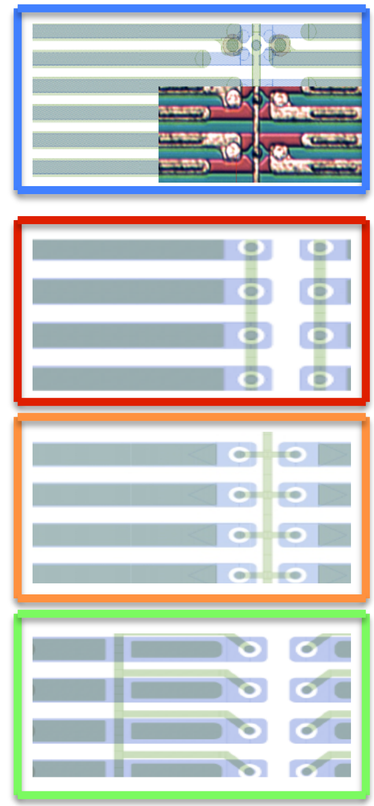


Module thickness: 270 µm



Efficiencies after irradiation





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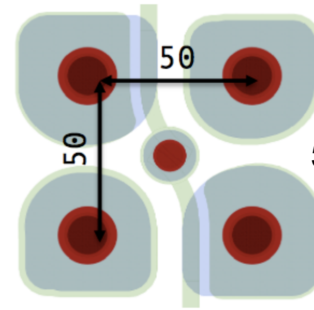
- Efficiencies of different punch-through designs at 500 V :

		at $5 \cdot 10^{15}$	at $3 \cdot 10^{15}$
i.	Standard pt :	**93.9 %**	(96.5 %)
ii.	Bias line over pt dot :	**94.9 %**	(97.3 %)
iii.	Bias line over center :	**89.0 %**	(92.7 %)
iv.	*Common pt for four pixels* :	***96.0 %***	*(99.0 %)*

$\Delta\varepsilon = 0.3$ %

New design for sensors compatible with the RD53 chip

- Punch-through design adopted from the two best performing ones: combination of biasline over p-t dot and common p-t



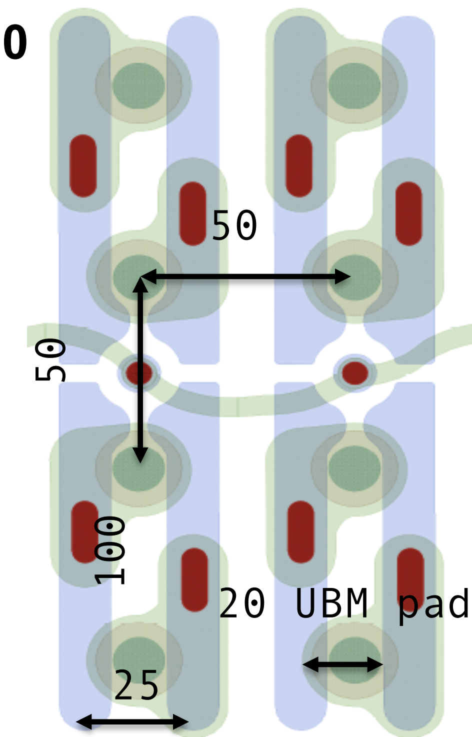
50x50

25x100 µm² pixel pitch

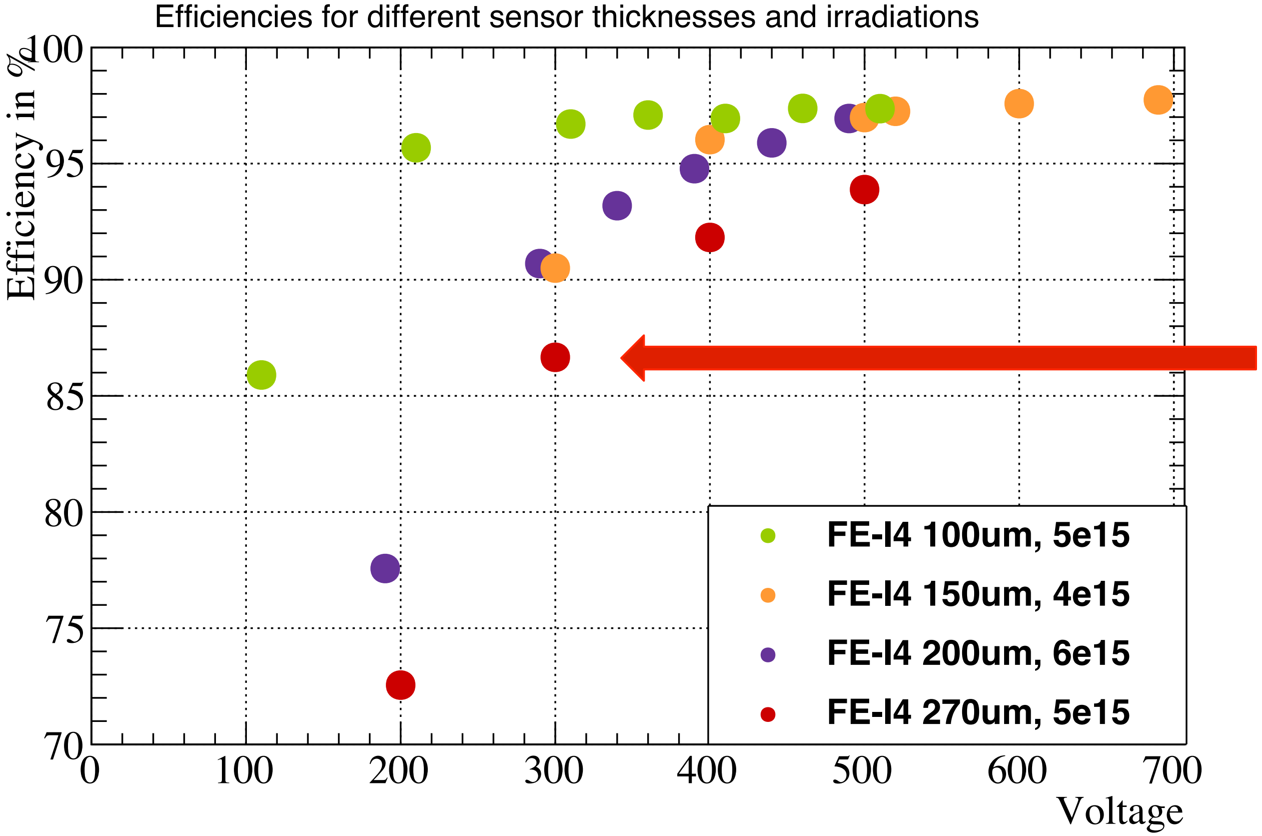
- Pixel staggered in such way to be compatible with a regular 50x50 µm² grid on the chip
- Design based on the existing prototype with 25x500 µm² pitch (results shown before)

New production on SOI wafers starting at MPG-HLL with 100 and 150 µm active thickness

25x100



Efficiencies at different thicknesses

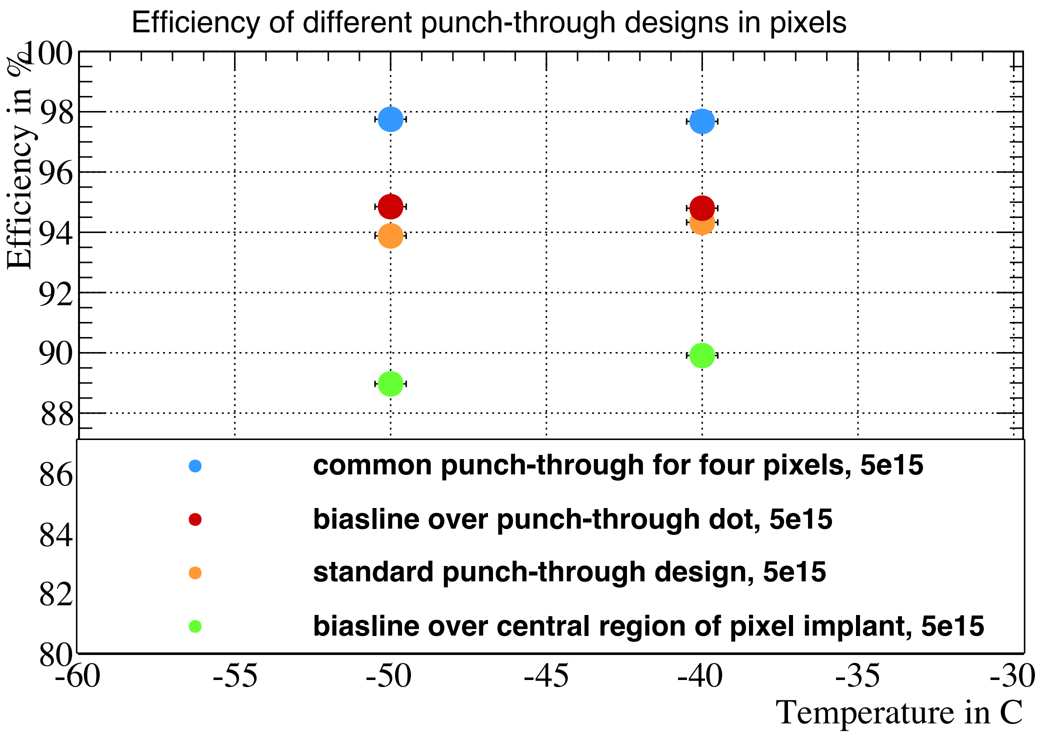


Standard pt-t design in FE-I4 with different thicknesses

Newly added! Sensor thickness of 270 µm

- Thinner sensors show higher efficiency at same level or irradiation
- Saturation of hit efficiency at higher voltages for thicker sensors
- Newly tested thickest FE-I4 (270 µm thickness) appears to be least efficient

Efficiencies at different temperatures



- Efficiencies of different punch-through designs at 500 V :

		at -50°C		at -40°C
i.	Standard pt :	**93.9 %**	(94.8 %)	
ii.	Bias line over pt dot :	**94.9 %**	(94.3 %)	
iii.	Bias line over center :	**89.0 %**	(89.7 %)	
iv.	*Common pt for four pixels :*	***98.0 %*** *(at 600 V)*	*(97.7 %)*	

Δε = 0.3 %

Grazing angle technique employing modules with a 50x250 μm² pixel pitch

Testbeam studies of tracking at high Φ

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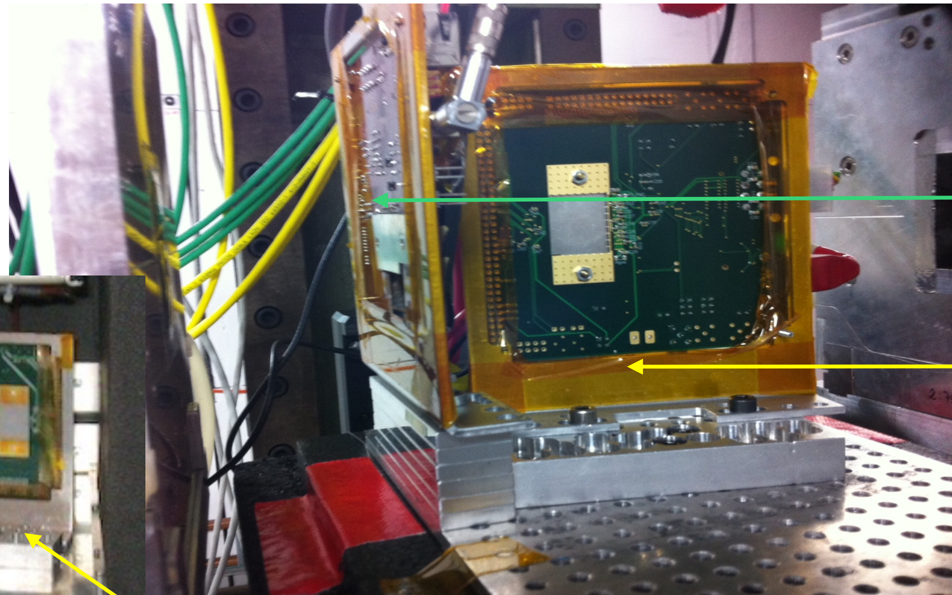
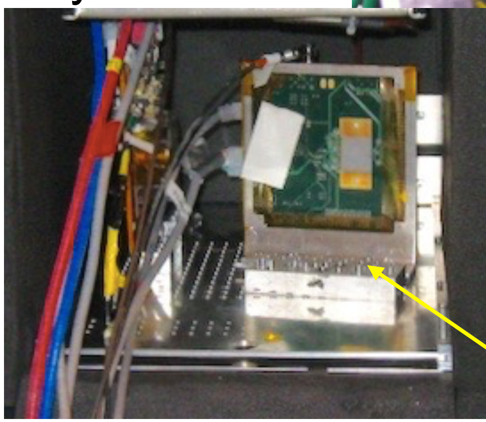
TB DESY
March ‘15

TB CERN
July ‘15



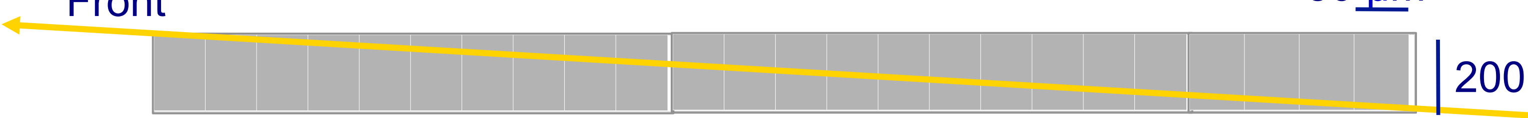


Not irradiated reference module

Irradiated DUT, 200 μm thick

Not irradiated DUT, 200 μm thick

- High Φ set-up with an n-in-p FE-I4 module at high Φ (80°), not irradiated and irradiated at 2 $\cdot 10^{15}$ n_{eq}/cm^2 at KIT and a reference plane, perpendicular to the beam



Distribution of cluster width

- Cluster size dependant on sensor thickness -> smaller cluster width for thinner sensors

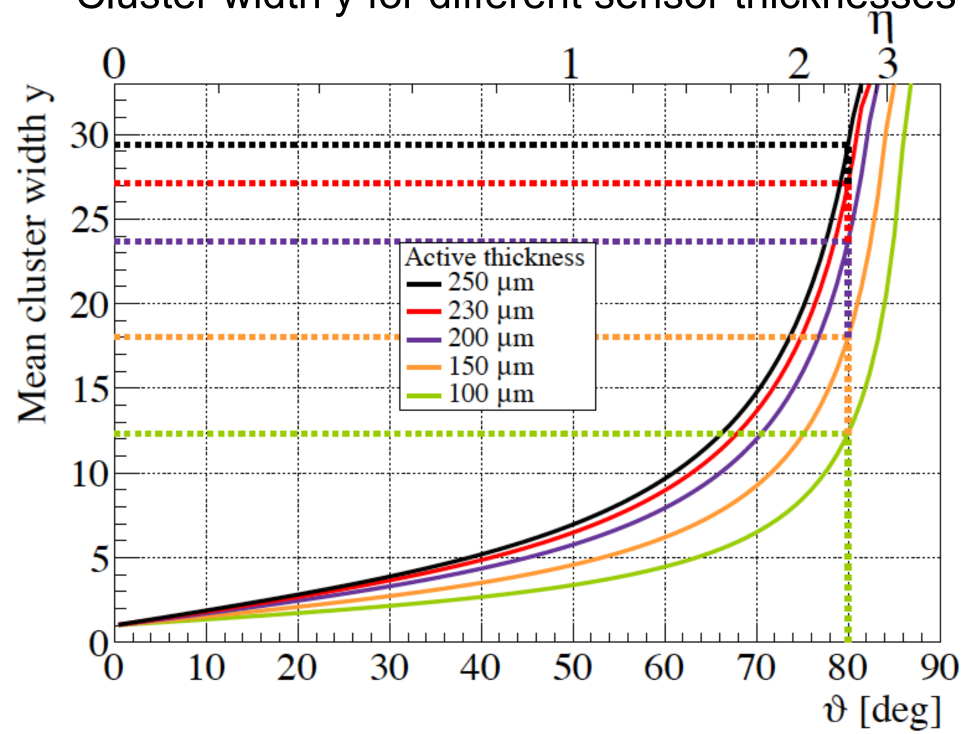
Example on cluster width for 200 µm thick sensor

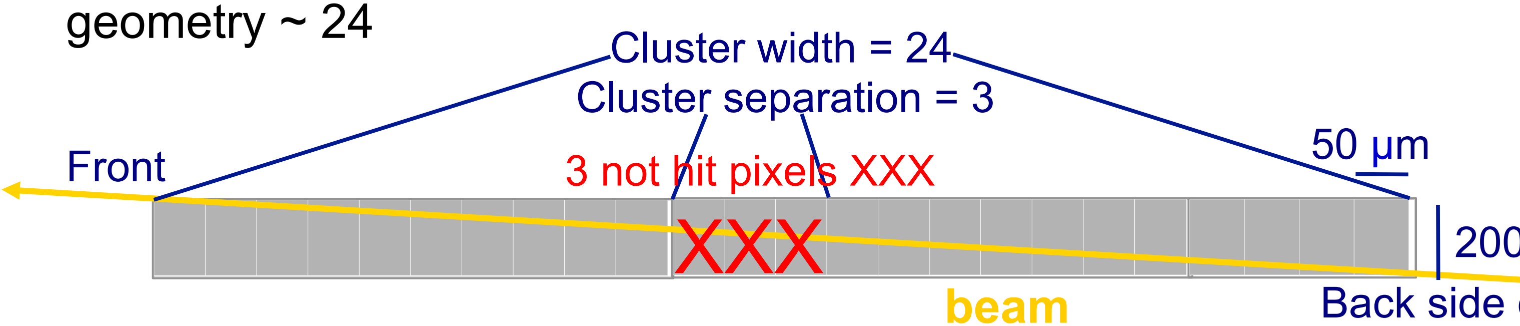
- Geometry :

  200 µm thickness,
  50x250 µm² pitch,
  placed at 80° in r-phi

- Expected cluster width from geometry ~ 24

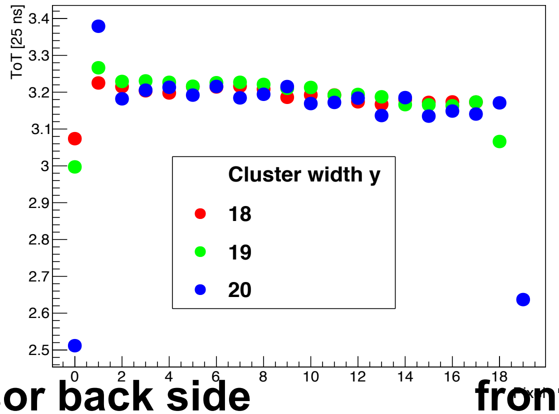
Cluster width y for different sensor thicknesses



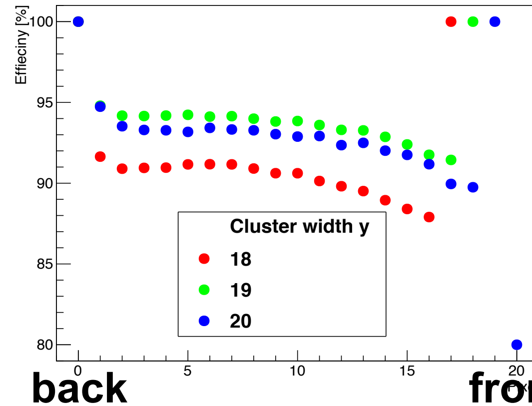


Charge Collection and Efficiencies at high Φ : not irradiated modules

Charge collection



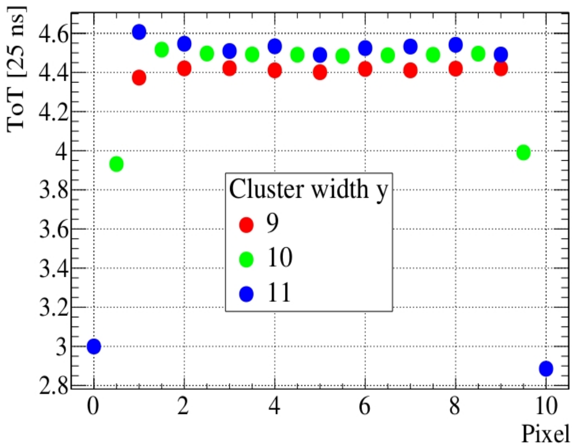
Pixel Efficiency



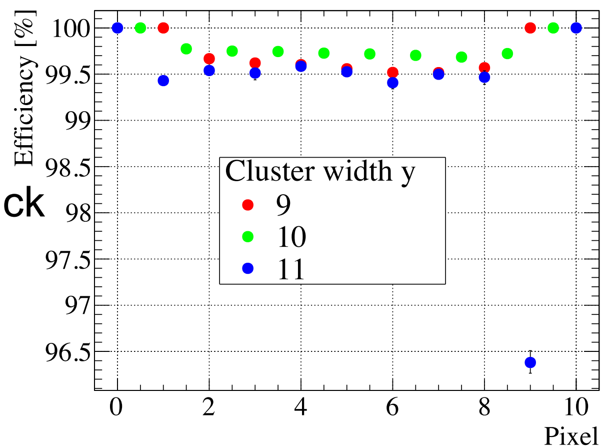
200 µm thick

sensor back side **front**

back **front**



100 µm thick



Decreasing cluster width for decreasing sensor thickness

- Constant charge collection for not irradiated modules
- Slight decrease of CCE and pixel efficiency on sensor front side for thicker module

Higher efficiency for thinner sensor

Charge Collection and Efficiencies at high Φ : irradiated module at 2 •10^{15} n_{eq}/cm^2

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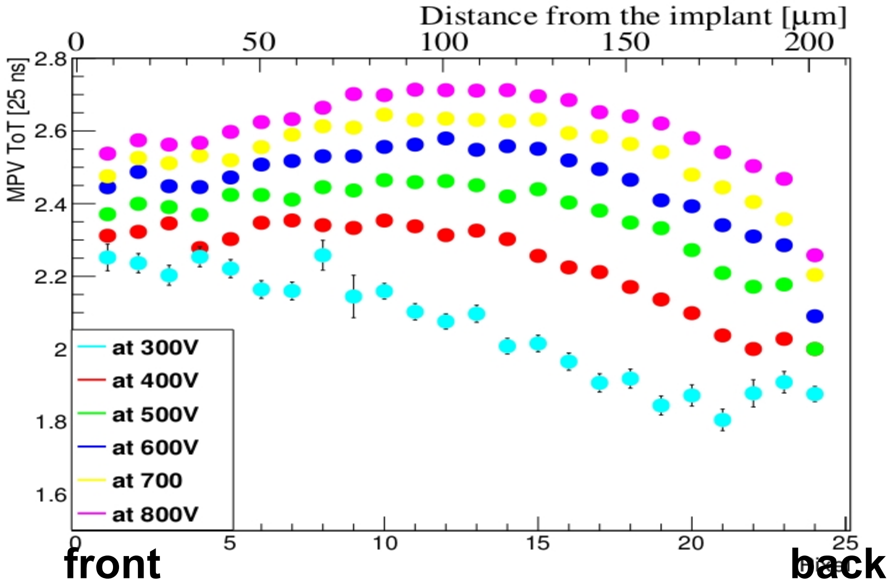
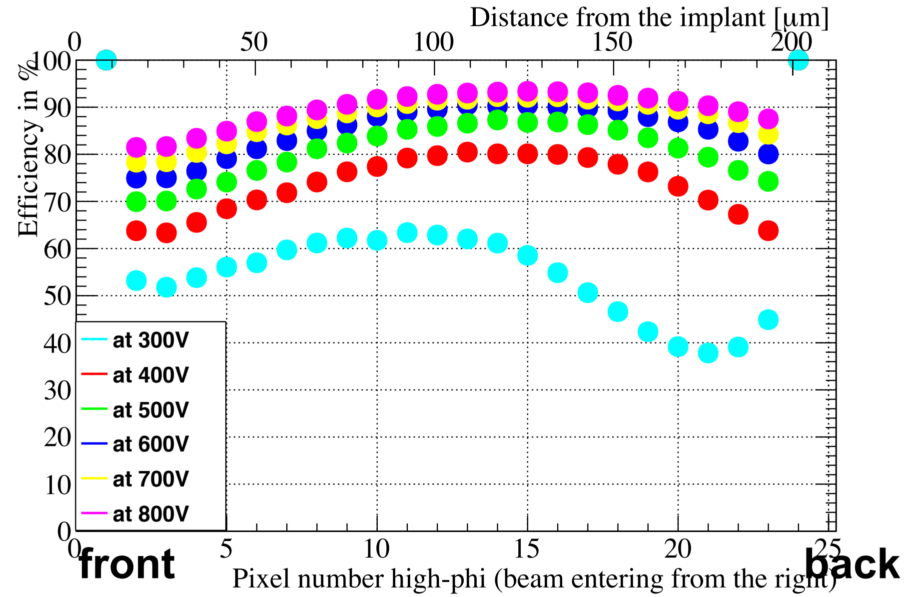
- Charge and Efficiency vs pixel number and depth at 300 V up to 800 V for a cluster width of 24 (module thickness **200 µm**)
- Tuning of CiS2 module : threshold 1000 e, 6 ToT @ 4 ke

Charge collection



Pixel Efficiency



- Flatter charge collection and pixel efficiency for higher voltages
- Decrease of charge collection and pixel efficieny on sensor back- and front side

Plan to repeat the measurements after irradiation for thinner sensors

Summary and Outlook

- New ADVACAM production for thin active edge sensors
  - Encouraging results up to now
  - Further characterization campaign in the upcoming weeks
- Testbeam studies
  - Different punch-through designs show different efficiencies :
    - Improved hit efficiency with respect to the standard design especially for the external p-t (99.4 % at 3 $\cdot 10^{15}$ n_{eq}/cm^2 and 97.75 % at 5 $\cdot 10^{15}$ n_{eq}/cm^2!) and the biasline over the p-t (97.3 % at 3 $\cdot 10^{15}$ n_{eq}/cm^2 and 94.9 % at 5 $\cdot 10^{15}$ n_{eq}/cm^2!)
- Grazing angle studies
  - Charge collection constant throughout the sensor depht
  - Plan to repeat the measurements after irradiation for thinner sensors

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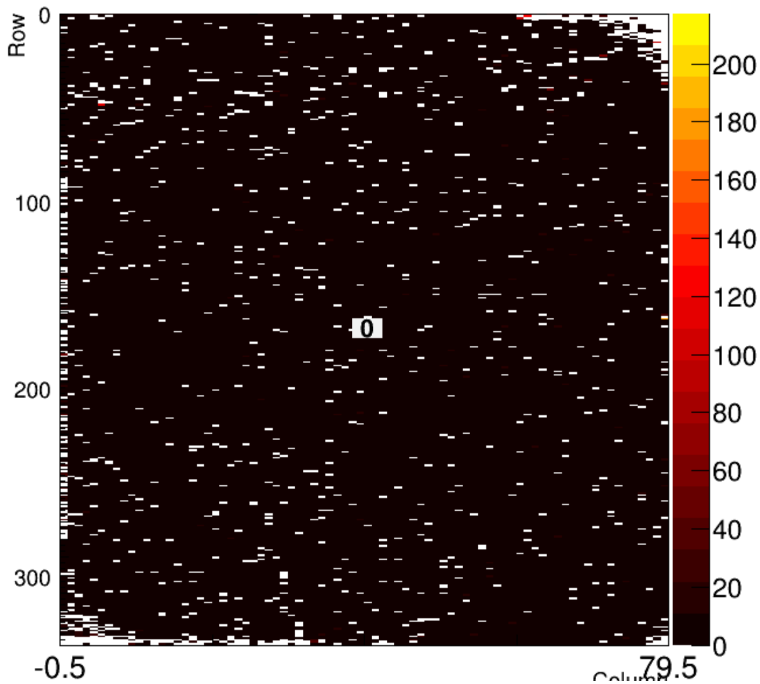
Thank you for your attention!

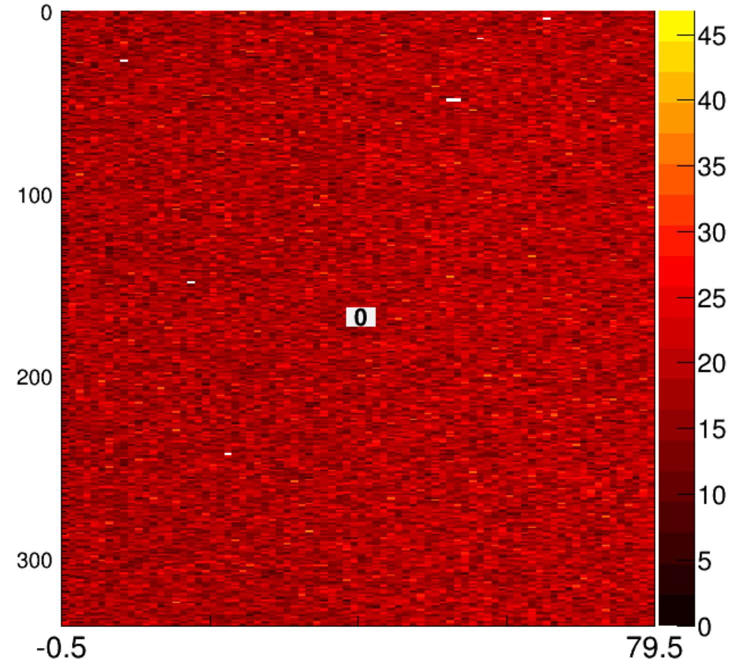
Back-up

Source Scans with Cadmium

- Modules with Pt UBM are more noisy and show disconnected corners
- Modules with Au/Cu UBM have very good performance
- No BCB implemented in this production
  - need parylene coating before irradiation



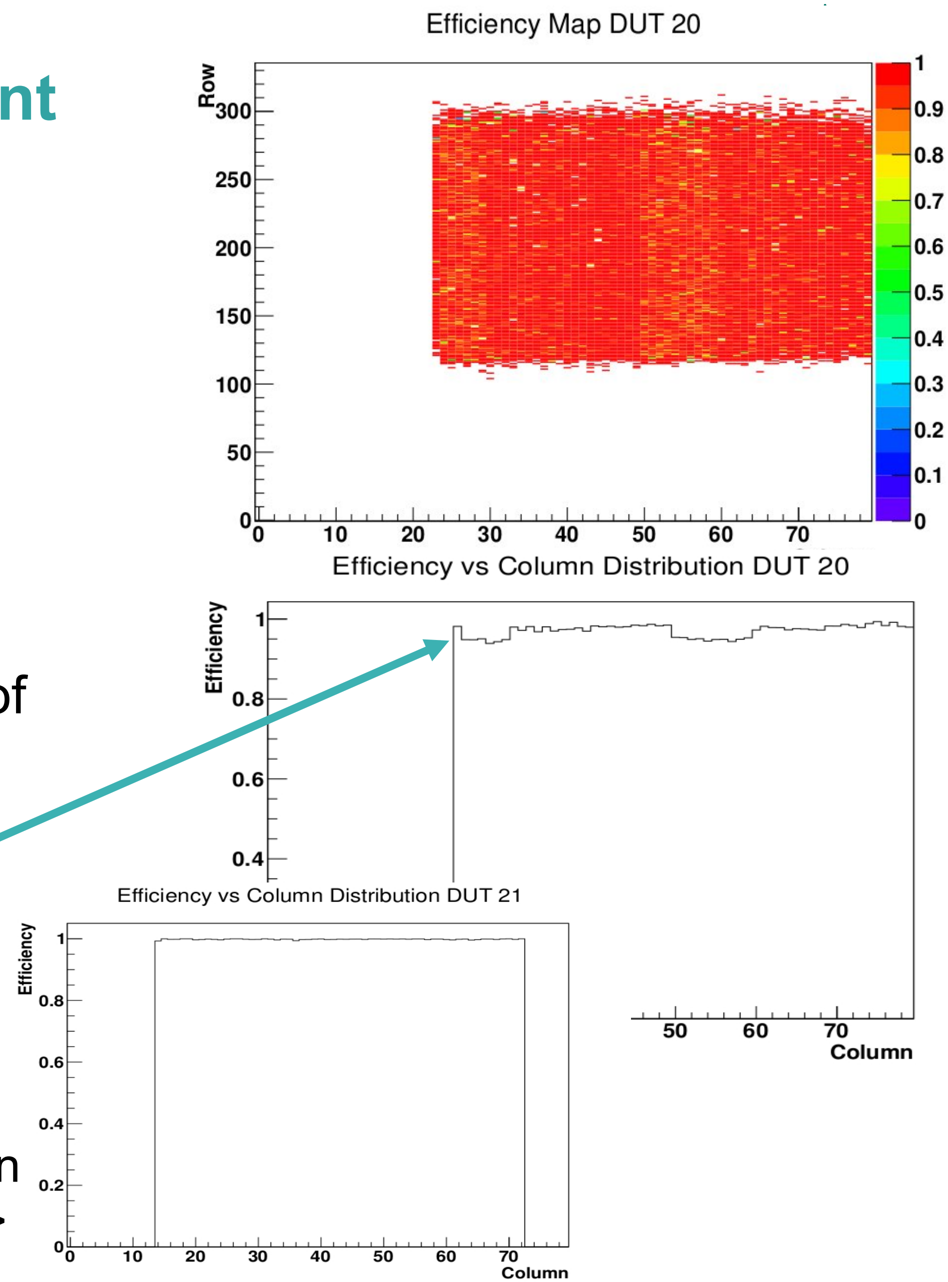
Thin film Pt UBM



Electroplated Au/Cu UBM

Hit efficiency map of different punch-through structures

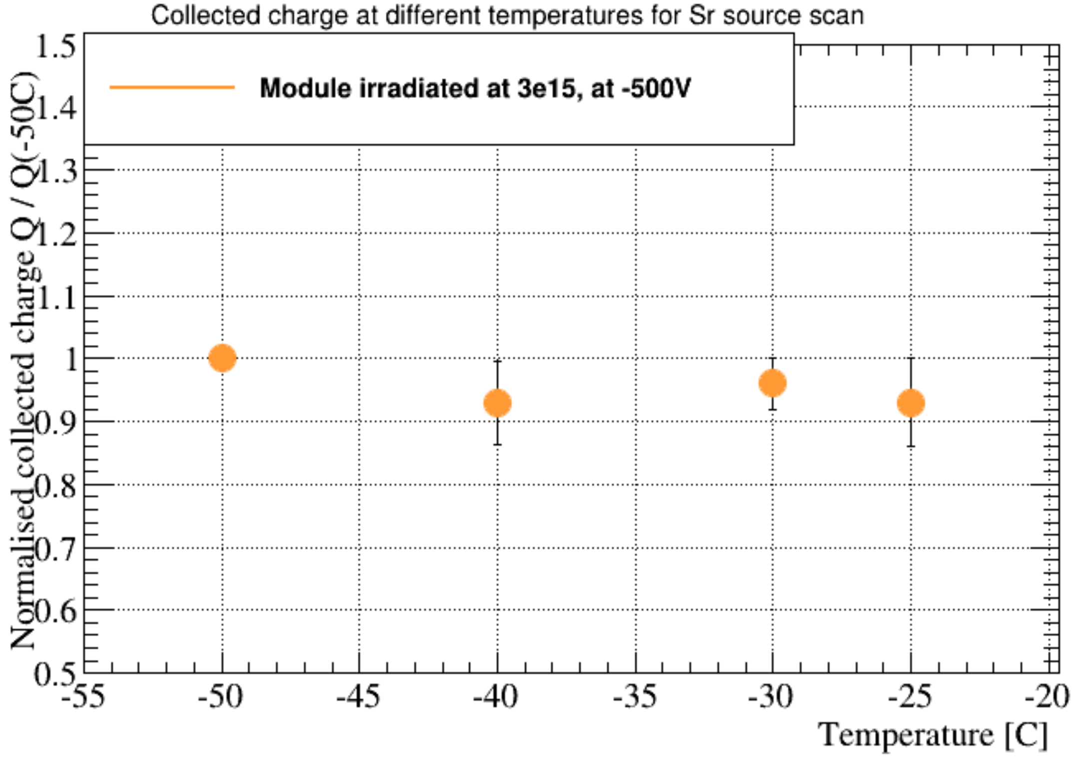
- Sensor with 3 different punch-through designs (every ten columns):
  - C30-40 : standard
  - C40-50 : bias line over punch-through dot
  - C50-60 : bias line over center of pixel implant
- Differing efficiencies depending on punch-through structure



For comparison: hit efficiency vs column of the same module, but unirradiated ->

Lab studies: Charge at different temperatures

- Charge collection of one module irradiated at a fluence of 3e15 n_{eq}/cm^2 at KIT and at temperatures of -50°C, -40°C, -30°C and -25°C (module retuned for each temperature step)
- Charge collection with Strontium source scan at a voltage of 500 V



→ **Collected charge does not vary with temperature**

Distribution of cluster widths

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- Cluster width distribution at 200 V to 800 V
- Expected cluster width from geometry ~ 24
- Geometry :

  200 µm thickness,
  50x250 µm² pitch,
  placed at 80° in r-phi