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PSI-ROC4SENS: A pixel-ROC for sensor tests

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Outline

- Introduction
  General Properties
  Dimensions
- Read Out
  Involved Signals
  Readout Chain
- Analogue Chain
- Calibration
  Test Pixel
  Calibration Signal
- Example: Measurement of the Lorentz Angle
- Status and Prospect

Introduction (1 of 2)

- Designed for sensor testing.
- Does not have a threshold.
- The output is analogue.
- A general purpose chip which is easy to operate and does not require programming.
  -->Implies high radiation hardness (> 500 Mrad)

- Can be controlled using a sequencer, reference voltages and an ADC.
- The periphery contains the I/O logic but no data storage beyond one hit.
- Fast trigger required:
  Hold switch must be opened ~50 ns after signal input.
- 0.25 µm technology by global foundries.

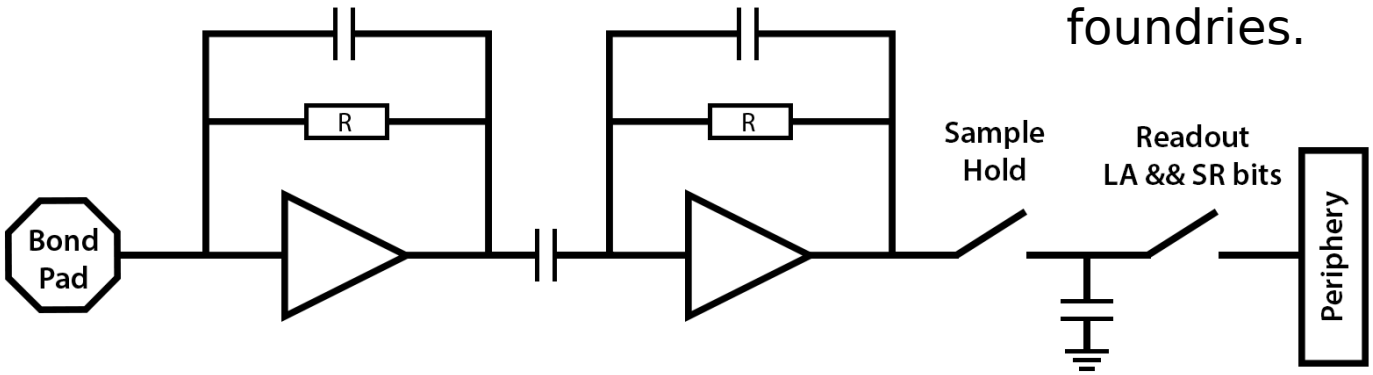


Figure 1:
Simplified schematic of a pixel cell.

Introduction (2 of 2)

- Total size:
  7.848 mm x 9.778 mm
- Pixel Cell size:
  50 µm x 50 µm
- 155 pixels x 160 pixels
- Alternating bond pad pattern to facilitate bonding of sensor strips with a width smaller than 50 µm.

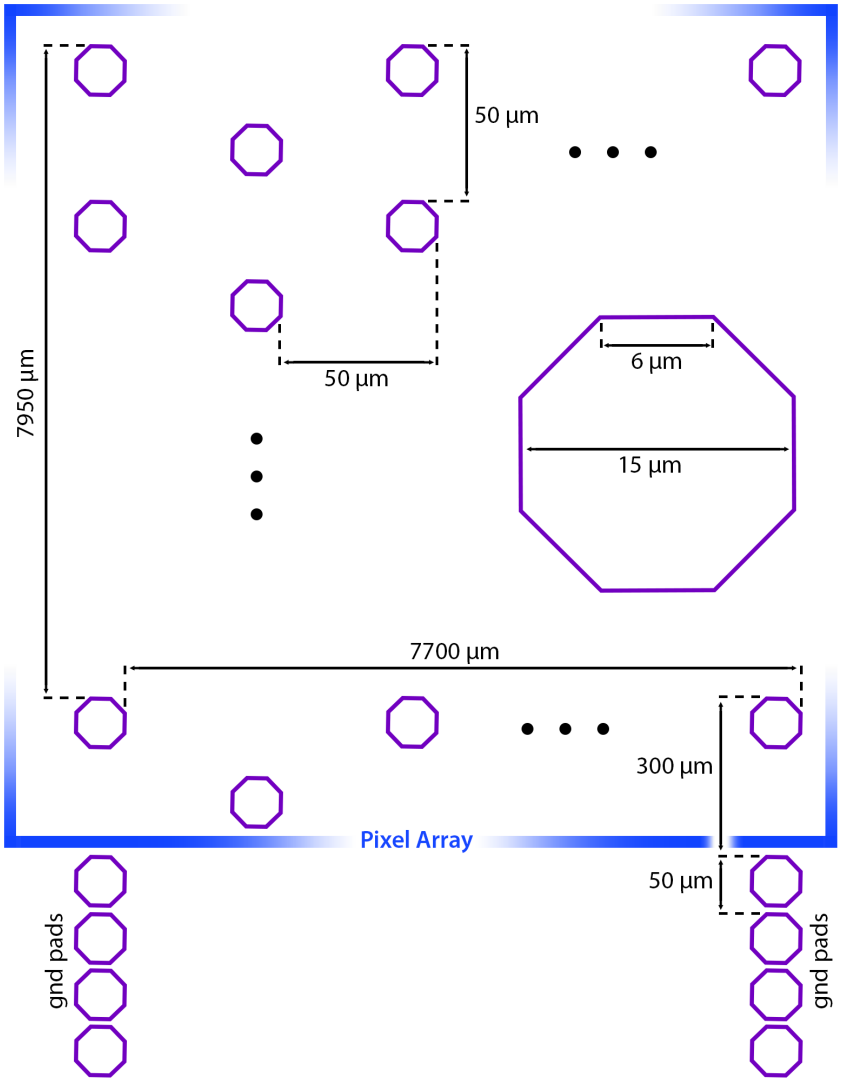


Figure 2:
Schematic bond pad pattern.

Read Out (1 of 4)

- Read out is enabled by bits in the shift registers (SR).
- Two clocks, φ1 and φ2, are used to clock the bits through the SR.
- The Reset signal corresponds to a input bit =0 being flushed through by setting
  φ1 = φ2 = 1 (in phase).
- The SRs are accessed separately. A switch signal controls which one is active.
- Latch active (LA) signal sends bits to the pixels.

  -->The effective bit sent to the pixels is:
  LA && bit in the SR.

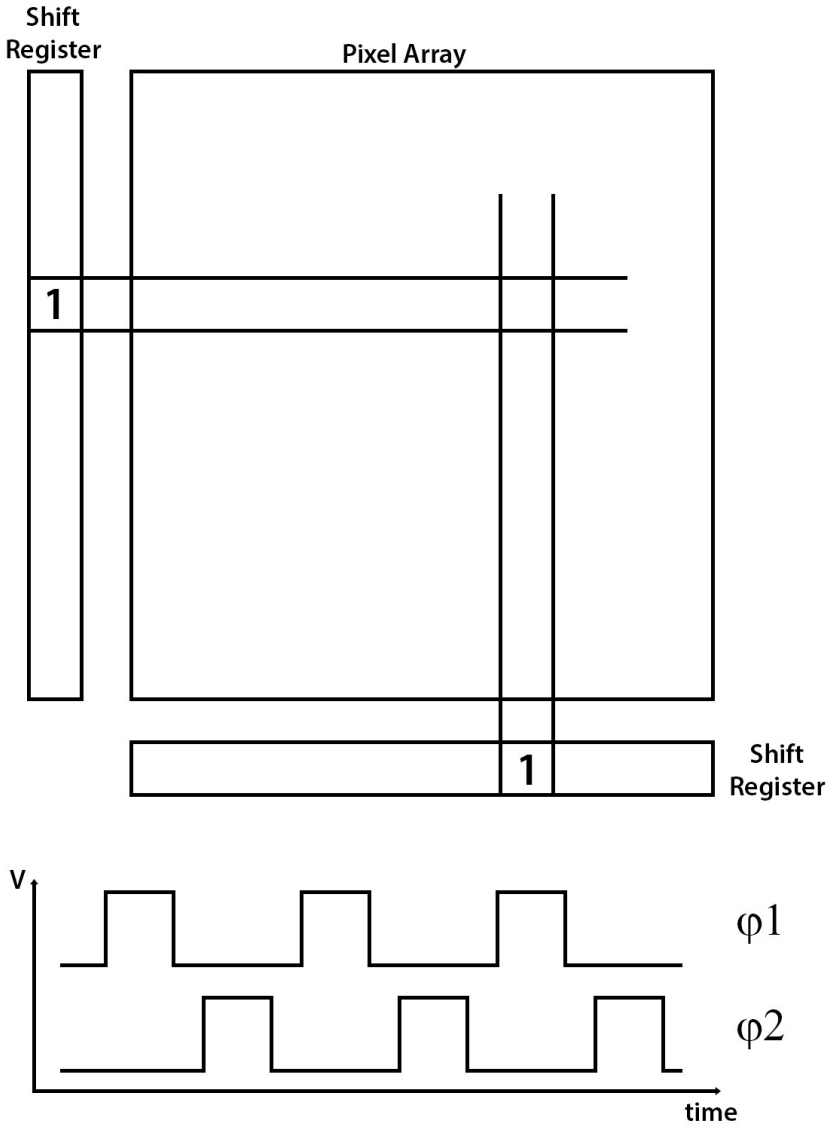


Figure 3:
Activating a pixel and clocking of the shift registers.

Read Out (2 of 4)

- Pre-readout:
  - Assuming incoming signal pulse at 0 ns.
  - Hold signal must open the switch at ~ 50 ns to store the signal in the pixels.
  -->A fast trigger mechanism is required to send the Hold signal.
  - The signal can remain stored for a comparatively long time (~seconds?).
  - The readout can be started immediately afterwards. However, a short (~10 – 50 ns) delay is recommended.

- After the readout procedure (next slide) the Hold signal must be deasserted before the next particle arrives.

Read Out (3 of 4)

- Readout procedure:
  - Reset the shift registers
  - Set (column) input bit
  - Clock the (column) SR
  - Switch the SR
  - Set (row) input bit
  - Clock the (row) SR
  - Assert LA
  - Read data out
  - Deassert LA
  - Switch the SR
  - … go through all columns …
  - Switch the SR
  - Set (row) input bit
  - Clock the (row) SR
  - Switch the SR
  - Repeat the procedure for the column SR
  - … repeat for all rows …

- Rough estimate of the time consumption of one full read out (20 MHz clocks and 50 ns sampling):
  5 ms (200 Hz)
- The sampling is decoupled from the shift register clock.
  -->Readout speed might be done faster as the SR might work at higher frequency.
- All input signals are differential (LVDS) with the exception of the (col/row) switch signal.

Read Out (4 of 4)

- There is one amplifier per pixel column.
- The outputs of all those amplifiers are connected together before reaching the differential amplifier.
- The output bits of the shift registers are also subject to the switch.
  → Only one SR can be read out at a time.
- The output signals (analogue output and shift register output bit) are both differential (LVDS).

Analogue Chain (1 of 2)

- The whole analogue chain from an example signal pulse to the output is shown in figure 4 & 5.
- The delay of the minimum in (2) w.r.t. the input signal can be varied by changing the analogue power.
  Up to 50 ns were tested in simulations.

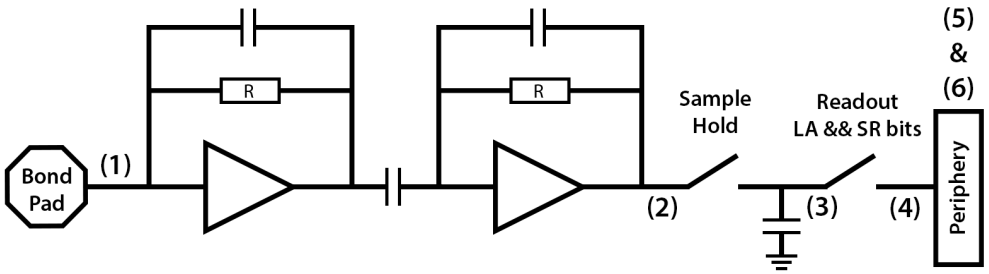


Figure 4:
Simplified schematic of a pixel cell.

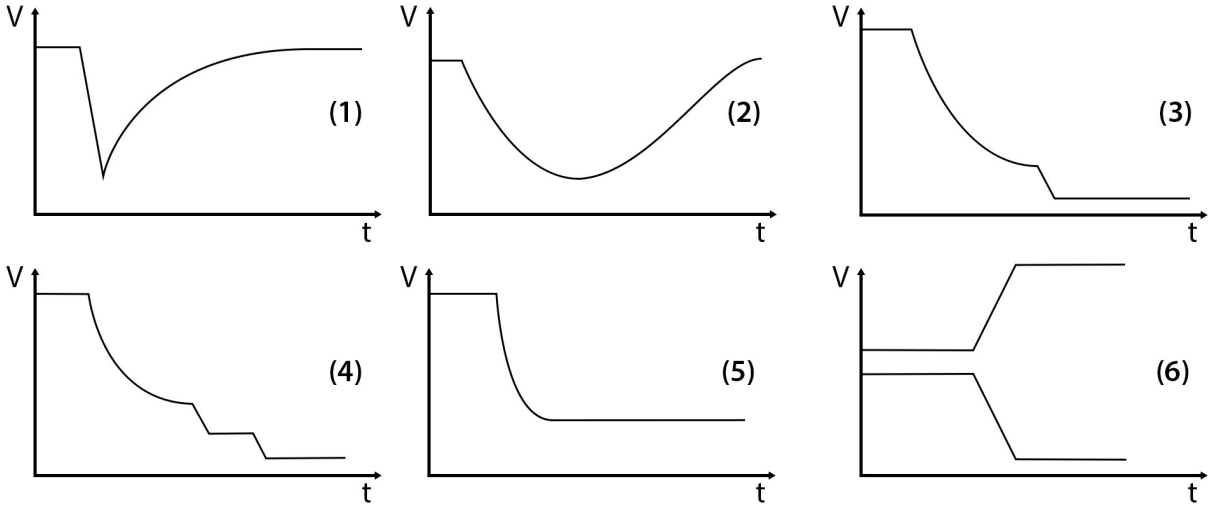


Figure 5:
Example pulse shapes at different stages of the readout. Each plot corresponds to a point in figure 5.

Analogue Chain (2 of 2)

- Simulation:

  The amplitude of the output signal as a function of the amplitude of the input signal is shown in figure 6.

- One Volt of the input signal was tuned such as to correspond to the charge of 10k electrons.

- Beware:
  The tuning implies that the pixel does not (and should not) see exactly these voltage values.

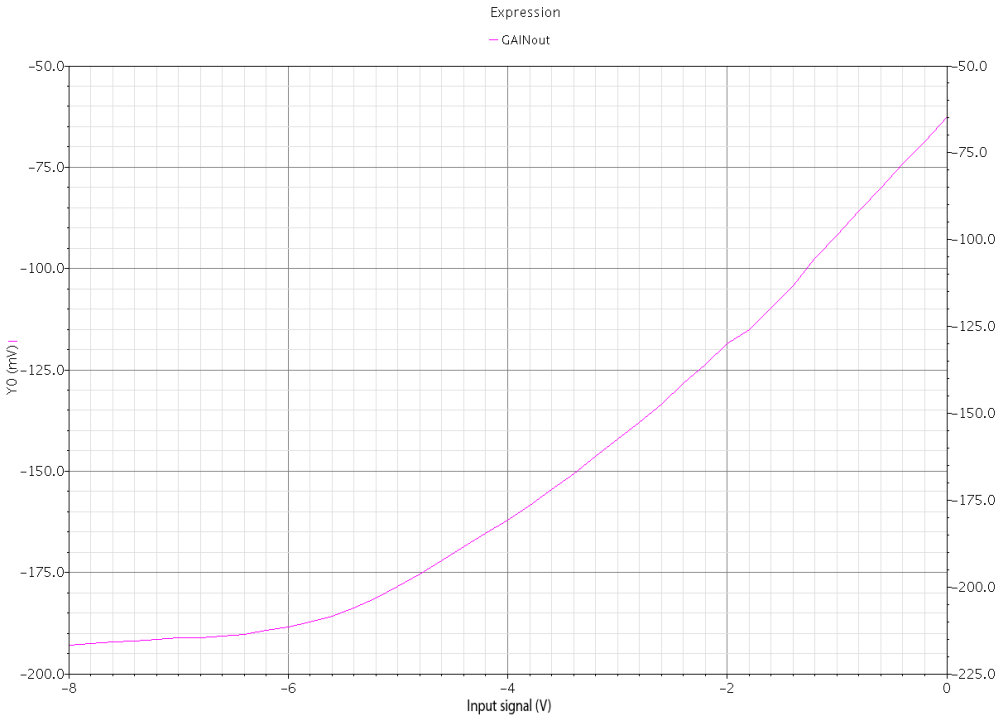


Figure 6:
The gain of the chip output as a function of the input signal's voltage.

Calibration (1 of 2)

- There are two tools implemented for calibration:
  - A test pixel
  - A calibration pulse
- The test pixel corresponds to the pixel output. (Readout in figure 7) The voltage applied to the I/O pad simulates the voltages over the Sample/Hold capacitor.
- It is an addition to the first pixel column.
- No bit in the row SR is needed for activation. Only a bit in the column SR && LA.
- Intended to calibrate effects of the pixel output and the periphery.

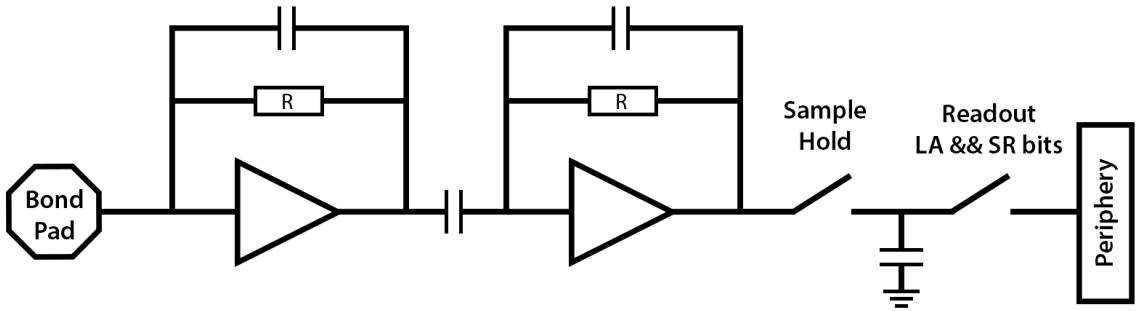


Figure 7:
Simplified schematic of a pixel cell.

Calibration (2 of 2)

- The calibration pulse simulates a signal pulse and goes through the whole pixel.
- To enable calibration pulses, the pixel must be enabled by SR bits, LA and an additional signal.
- The additional signal provides a layer of protection for the Sample/Hold capacitor.
- Without additional protection, activating a pixel for readout could cause an unintentional calibration pulse.

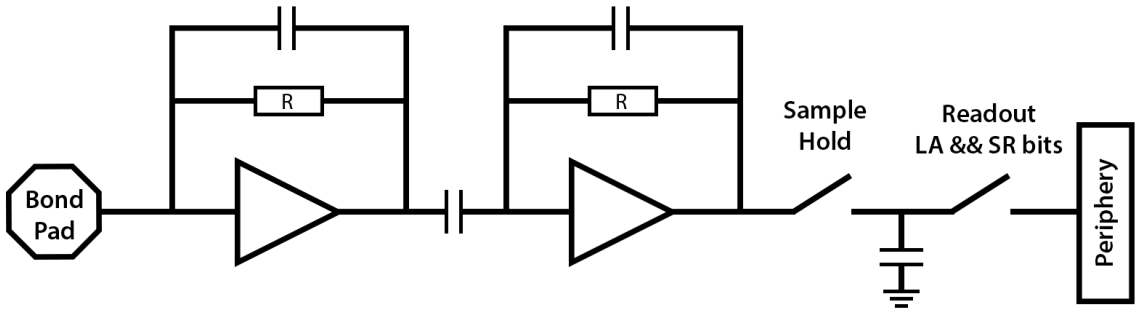


Figure 8:
Simplified schematic of a pixel cell.

List of Signals

- There are 40 wire bond pads in total:
  - Digital ground: 2 pads.
  - Digital power: 2 pads.
  - Analogue ground: 6 pads.
  - Analogue power: 4 pads.
  - Input bit to the SR (LVDS): 2 pads.
  - Output bit of the SR (LVDS): 2 pads.
  - Clock 1 (LVDS): 2 pads.
  - Clock 2 (LVDS): 2 pads.
  - Switch signal: 1 pad.
  - Hold signal (LVDS): 2 pads.
  - LA signal (LVDS): 2 pads.
  - Analogue output (LVDS): 2 pads.
  - Vcal pulse height (reference voltage): 1 pad.
  - Shaper feedback transistor gate voltage (reference voltage): 1 pad.
  - Preamp. feedback transistor gate voltage (reference voltage): 1 pad.
  - Reference voltage (multi purpose reference voltage): 1 pad.
  - Vcal enable signal: 1 pad.
  - Vcal pulse shape signal: 1 pad.
  - 2 pads related to the test pixel (reference voltages).
  - 3 pads related to the column amplifier (reference voltages).

Measurement: Lorentz Angle (1 of 2)

- Measuring the charge collection efficiency of particles penetrating the sensor at small angles wr.t. the sensor surface.
- Measurement performed by A.Dorokhov et al. using the PSI30 chip.

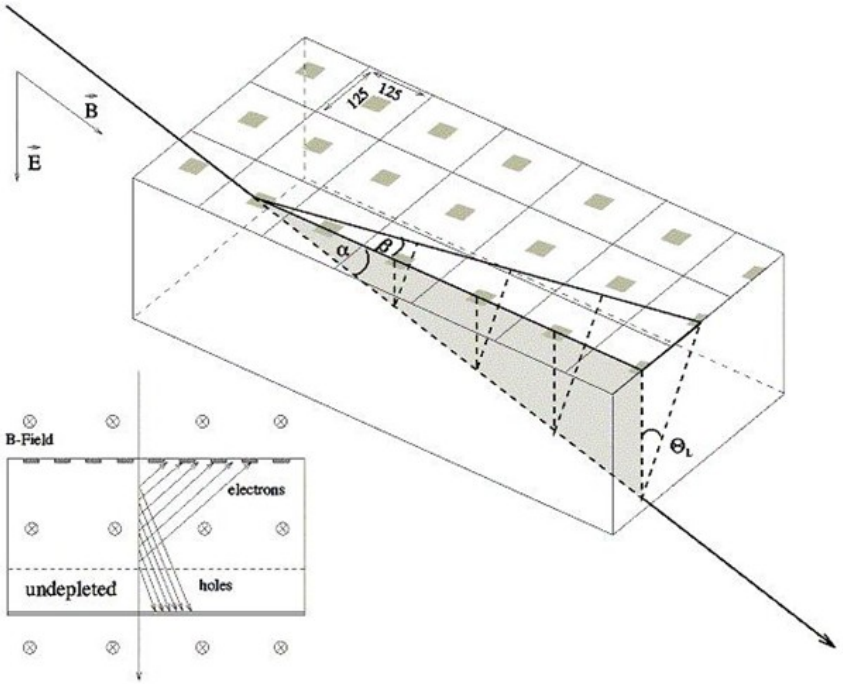
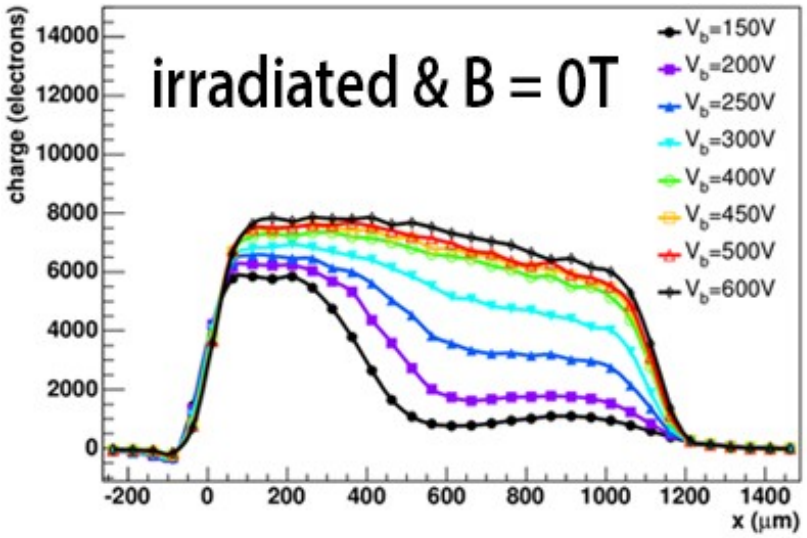
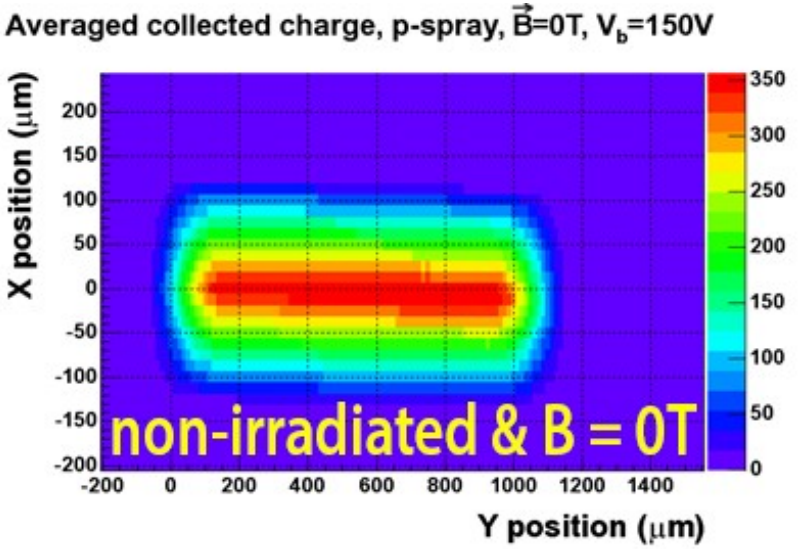
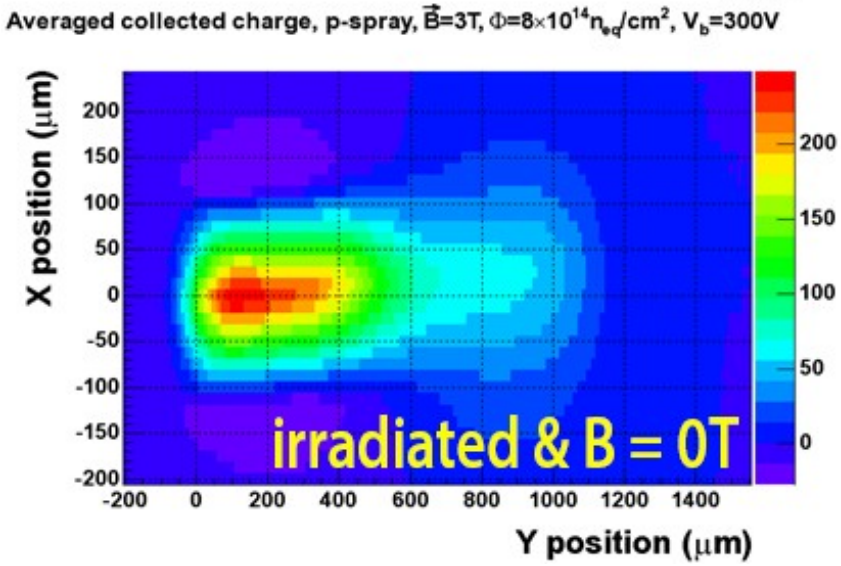


Figure 9:
Description of the Lorentz angle.
Figure placed at the disposal by Tilman Rohe, PSI.

Measurement: Lorentz Angle (2 of 2)







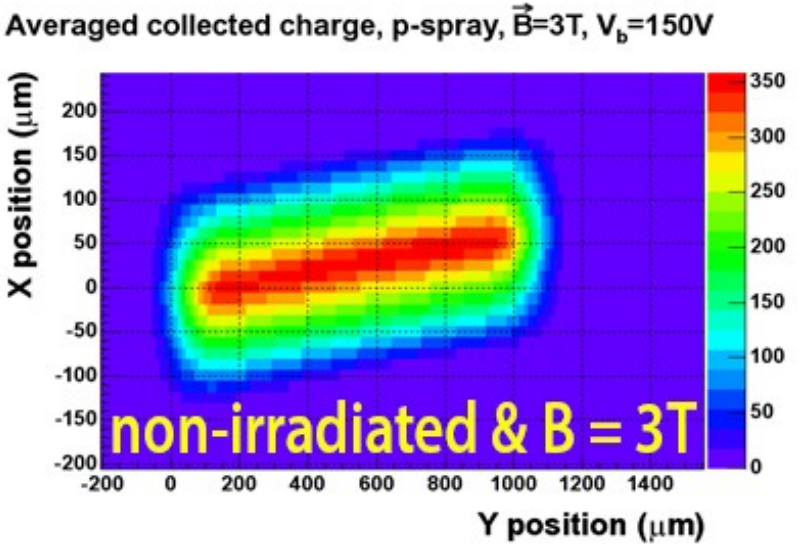


Figure 10: The charge collection as a function of position for different bias voltages and different magnetic field strengths. The figures were provided by A.Dorokhov et al.

Status & Prospect (1 of 2)

- The chip has been submitted on 23rd of October.
- The production is still in an initial phase.
- Expected return: March 2016.
- The functionality and radiation hardness will be tested by PSI.
- The testing and potential resubmission depends on the CMS phase 1 PROC600.
- Available not before summer 2016.

Status & Prospect (2 of 2)

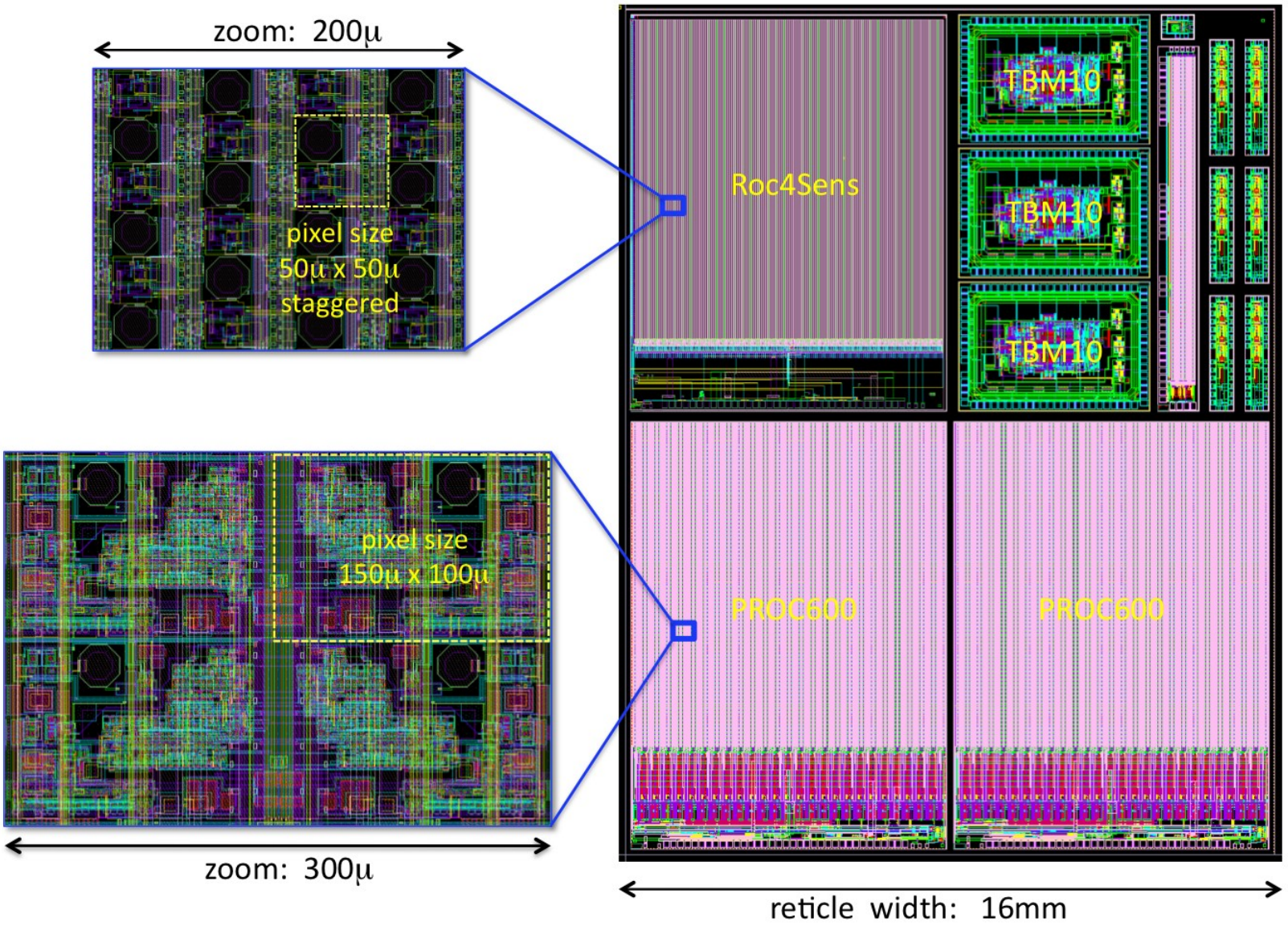


Figure 11: Submission including the ROC4SENS.

Summary

- General purpose readout chip without threshold and designed for sensor tests.
- The readout and calibration is controlled via two shift registers and provides an analogue output signal.
- Includes two calibration features.