Ongoing Activities at CiS

CiS Forschungsinstitut für Mikrosensorik GmbH

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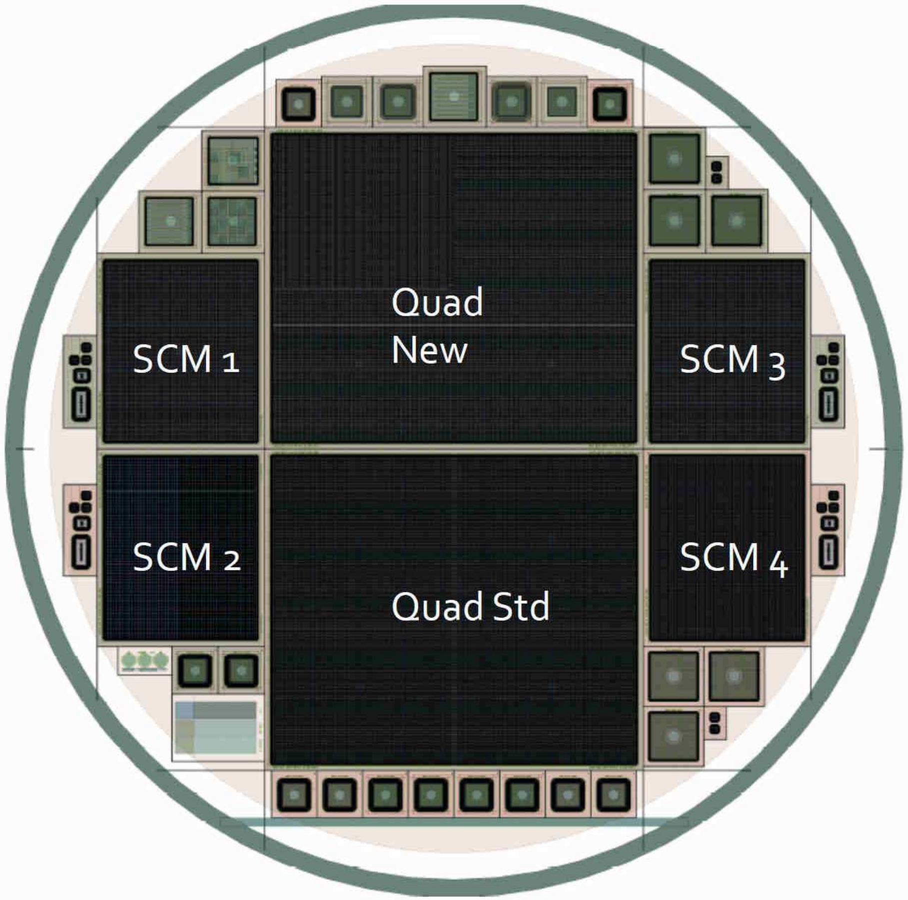
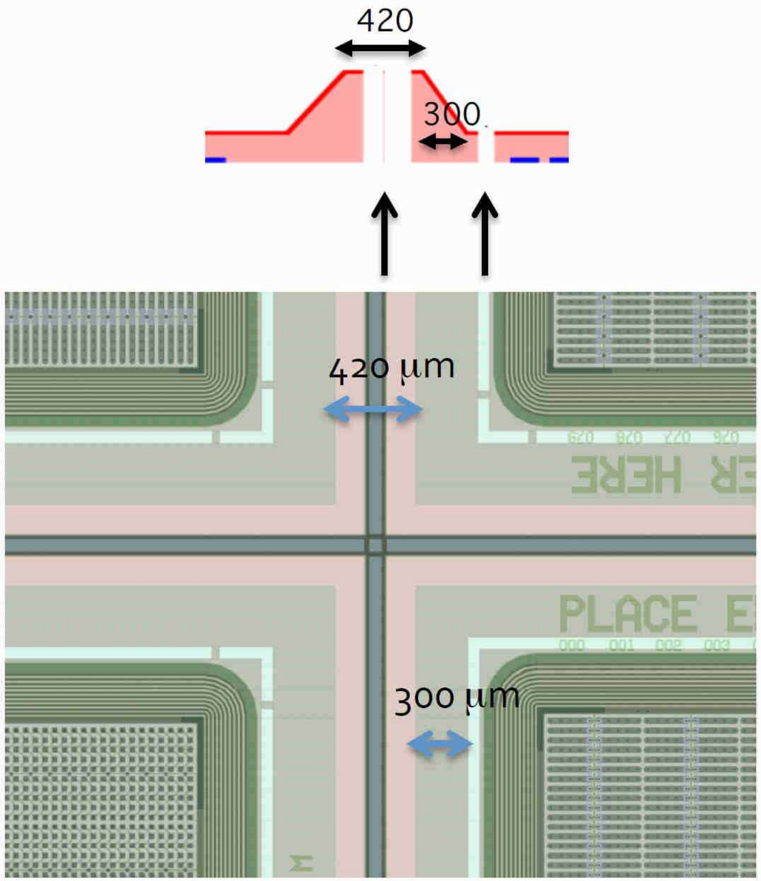
New thin production at CIS – Wafer Design

- Two sets of dicing lines:
  - On the 420 μm wide frame between the structures
  - Dicing along the sensor perimeter on the thinned substrate
  - Guard ring structure within the thinned area

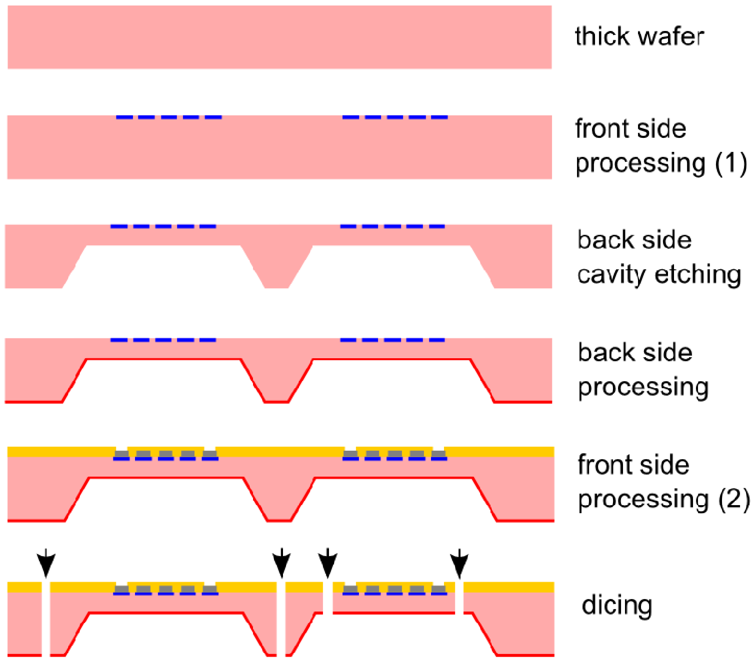
Design in collaboration between MPP and CIS

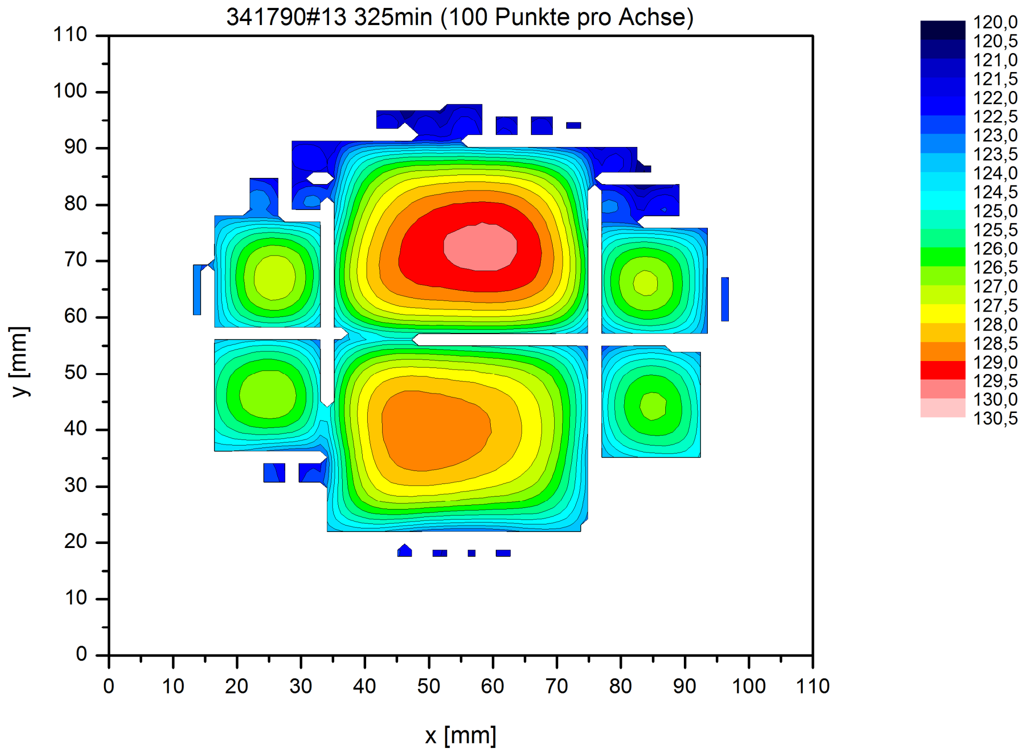


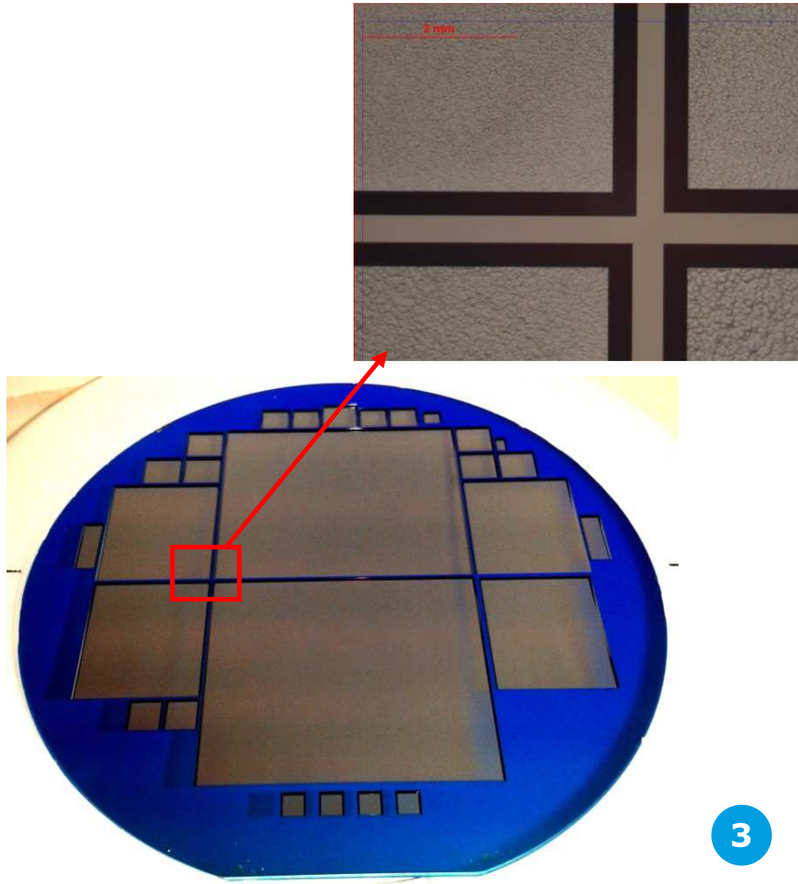


sensor thinning by KOH etching

- prototype run with MPP
- n-in-p ATLAS pixel sensors
  - FE-I4 Quad-Sensors (~4x4cm²)
  - FE-I4 SCS
- starting thickness 525µm, target thicknesses 150/100µm
- dummy wafer trials showed proof of principle for large area cavity etching
  - thickness fluctuations in the order of ~10µm could be reached



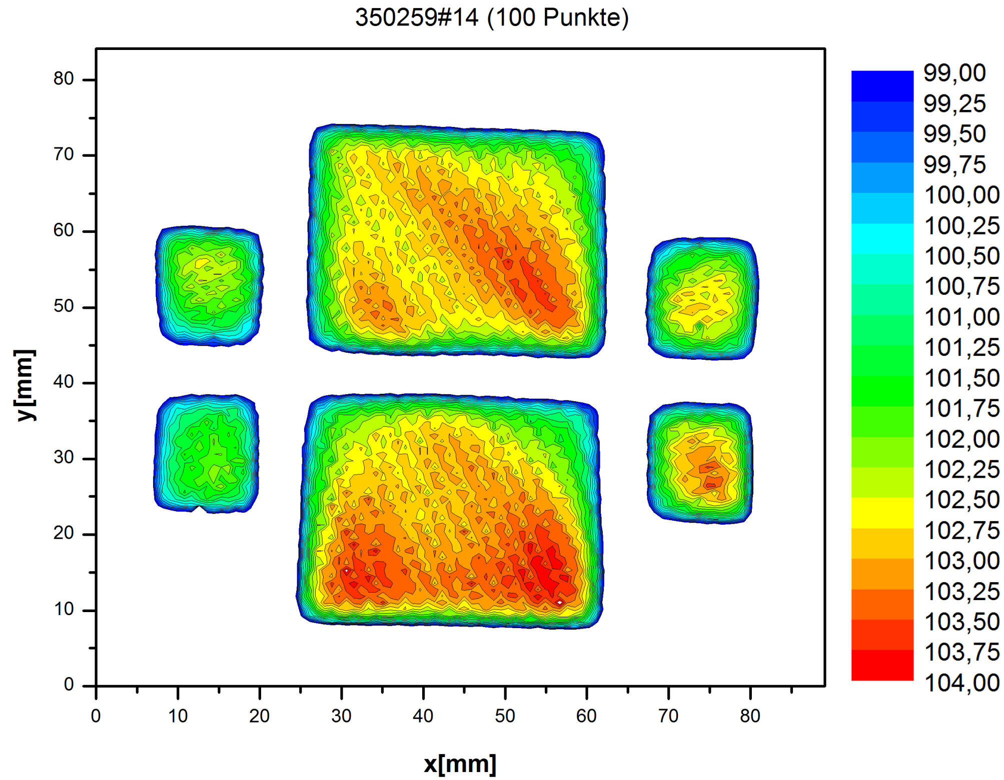


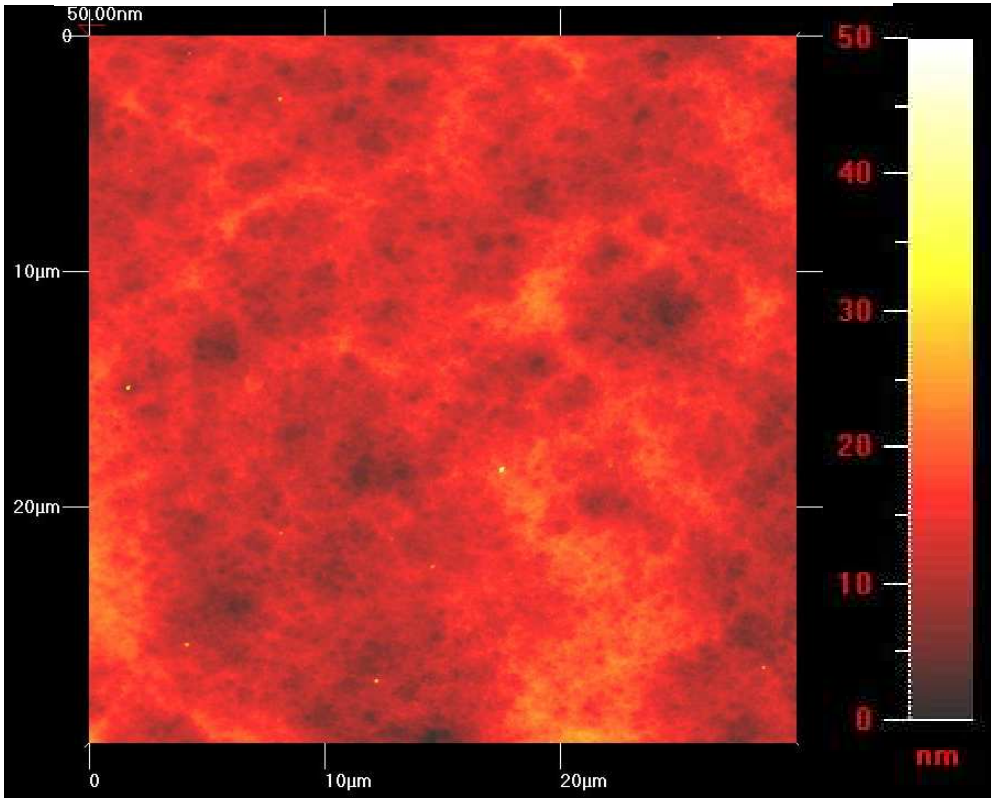


sensor thinning by KOH etching – sensor run

- one batch of 25 wafers processed
- no mechanical breakage

- checked again homogenity of the membranes:
  - large scale (thickness measurements)
    - same homogenity as seen for the dummy wafers
    - thickness fluctuations in the order of 5…10µm could be maintained
  - small scale (AFM measurements)
    - looks more than satisfying
    - average fluctuations in the order of a few 10nm





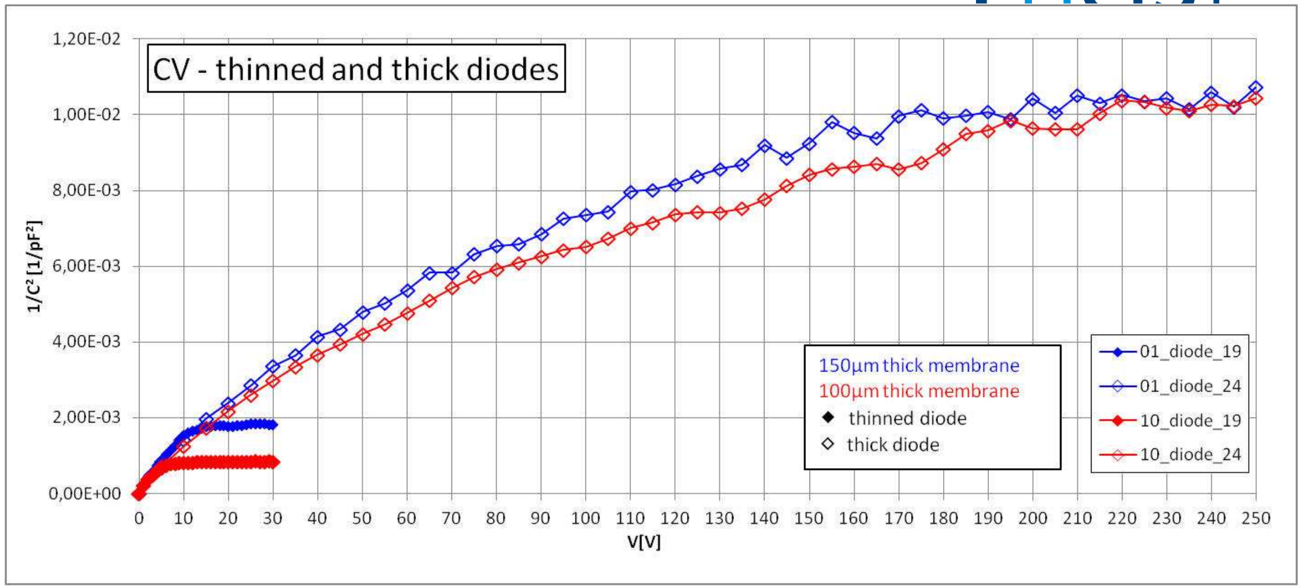
sensor thinning by KOH etching – sensor run

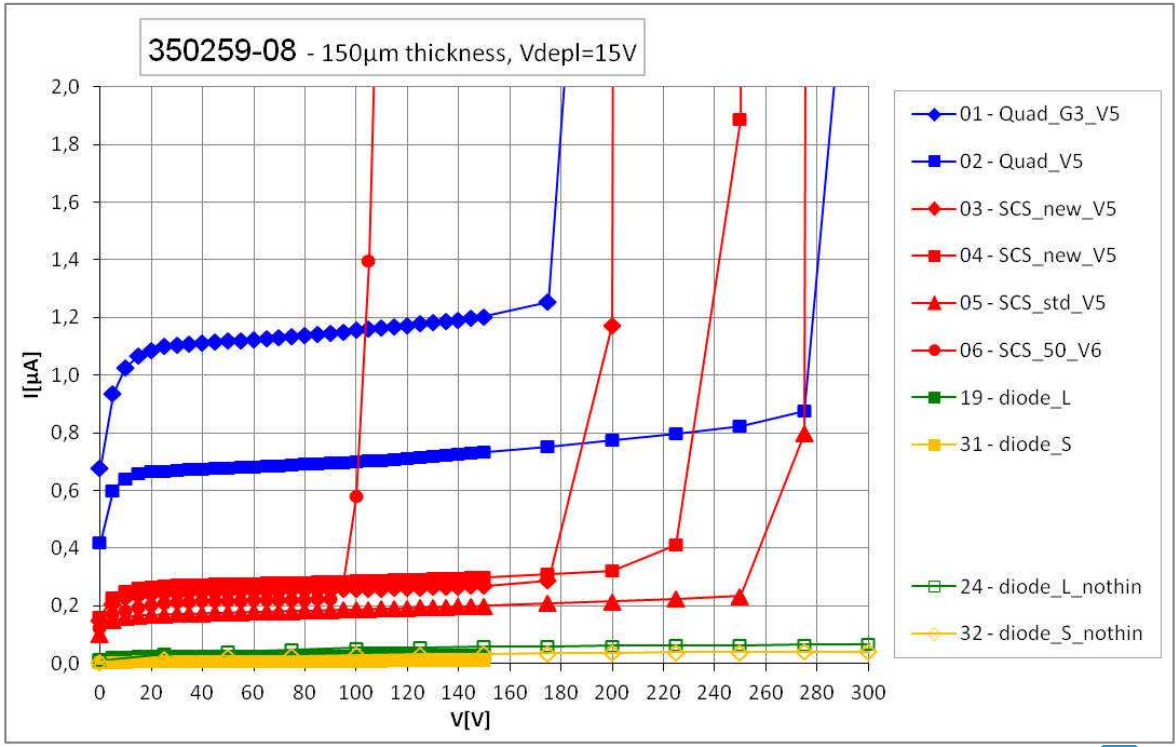
electrical characterization

- depletion voltages as expected
  - ~15V for 150µm membrane
  - ~7V for 100µm membrane
  - >200V unthinned
- IV-characteristic looks very well
  - breakdown voltages mostly >50V above V_{depl}
- electrical yield of pixel sensors:

	150µm	100µm	total
FE-I4 Quads	93,8%	71,4%	83,3%
FE-I4 SCS	96,9%	92,9%	95,0%

- next steps: UBM & Dicing
  - 3 different types of UBM
    - electroplating (IZM)
    - mask-based Ni/Au (as for CMS)
    - mask-based Pt/Au
  - dicing within the thin membranes



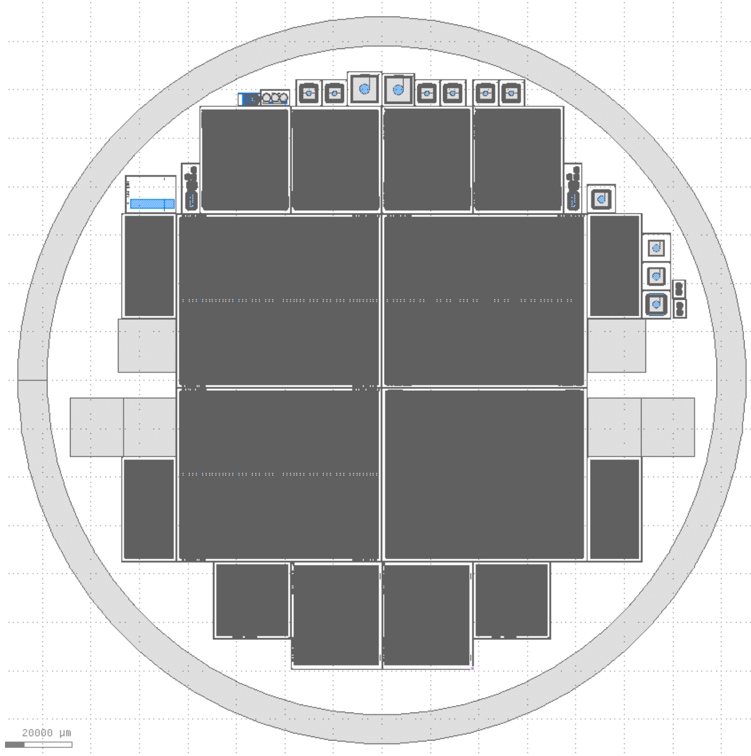


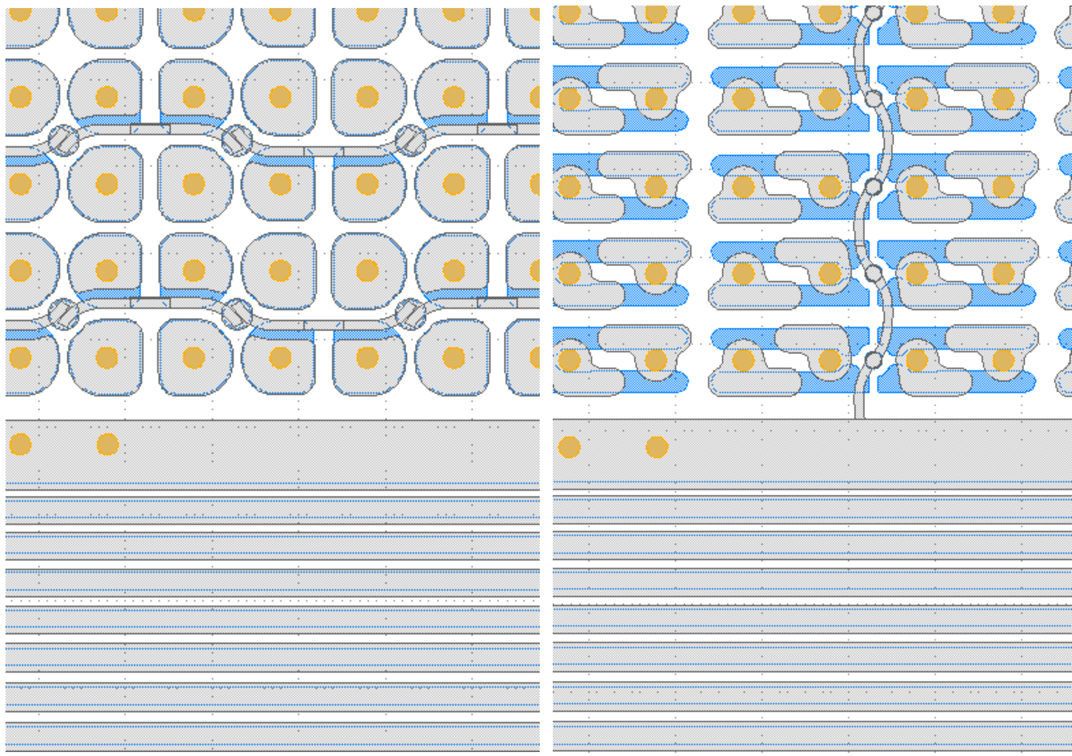
upcoming 6" prototype wafer run

- try to transfer the technology of cavity etching to 6" wafer size
- same kind of sensors for comparison
  - FE-I4 quads
  - FE-I4 SCS
- additionally several other new designs
  - RD53 test chip
  - CMS Roc4Sens
  - Omegapix
  - Medipix
  - test structures …

RD53 test chip and CMS Roc4Sens: 50x50 and 100x25µm² pixel size, w/ and w/o bias grid

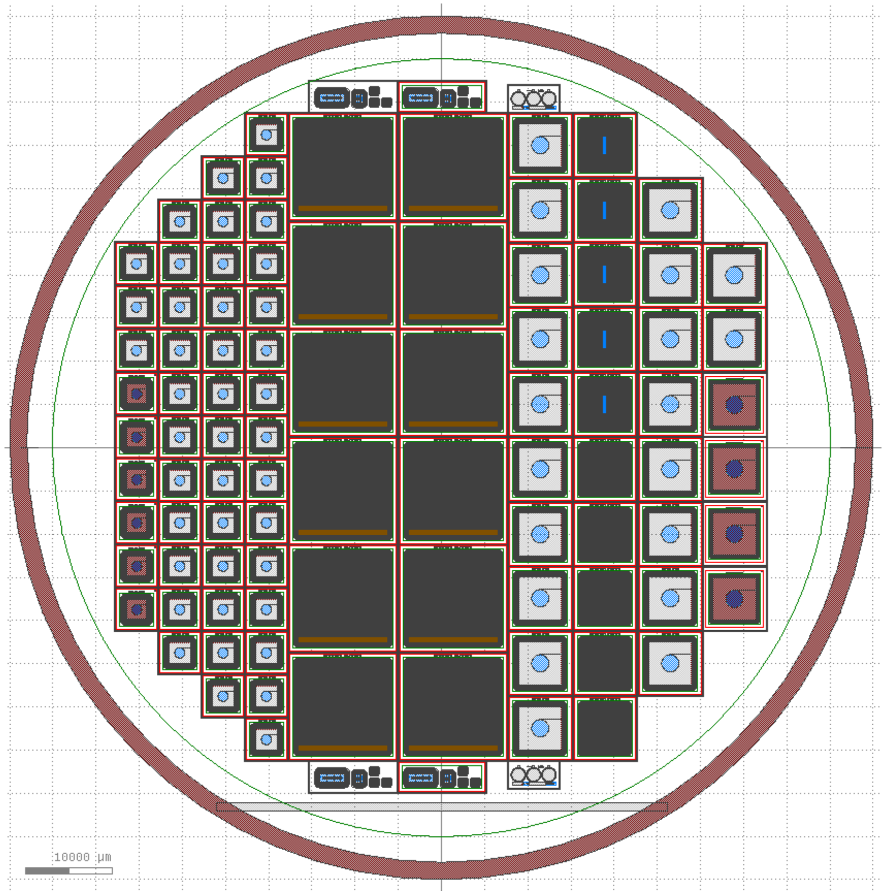
- wafer layout is currently finalized





SSD prototype wafer run

- analog technology as MPP run (+Poly-Si)
- n-in-p, backside cavity etching
- less ambitious as cavitiy areas are much smaller
- several different structures on wafer
  - micro strips (80µm pitch, Poly-Si-Res)
  - diodes (two sizes)
  - spaghetti diodes (two kinds)
- two kinds of wafer material with various resistivities
  - Epi (525µm substrate + 50µm Epi)
    - etching the complete substrate
  - FZ (285µm)
    - etching to 50, 100, 150, 200µm (+unetched)
- process should be finished next week

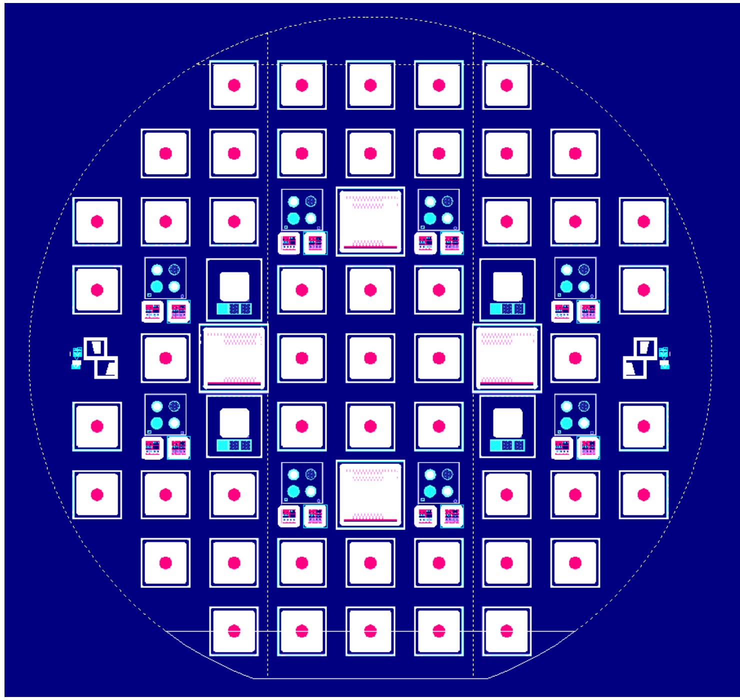


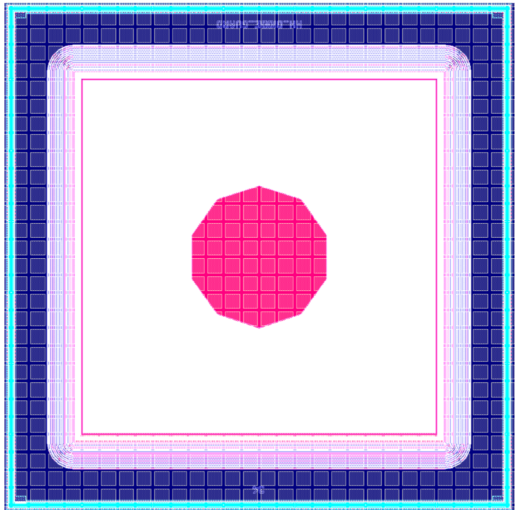
NitroSil prototype wafer run

- cooperation with ITME and Topsil
- comparison of N_2-enriched wafers to various other wafer materials
  - N_2-enriched
  - w/o enrichment
  - O_2-enriched
  - low-resistivity …
- MPW layout with pad diodes

- low temperature FTIR and charge carrier lifetime measurements are conducted in parallel on raw wafers

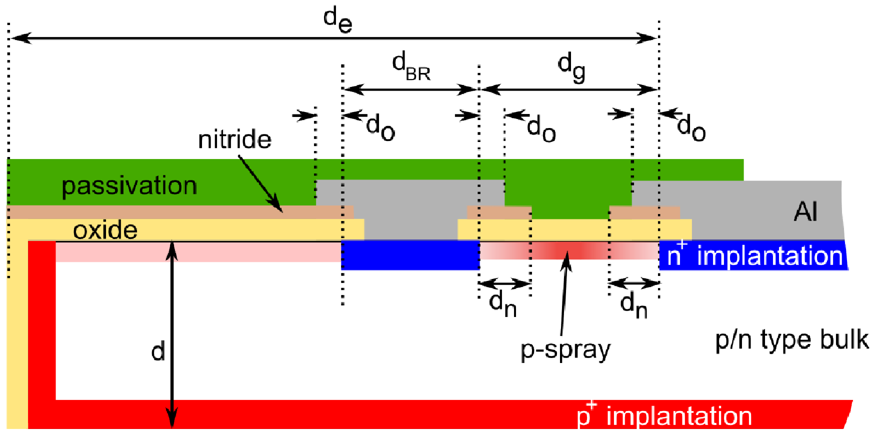
- wafer run just started

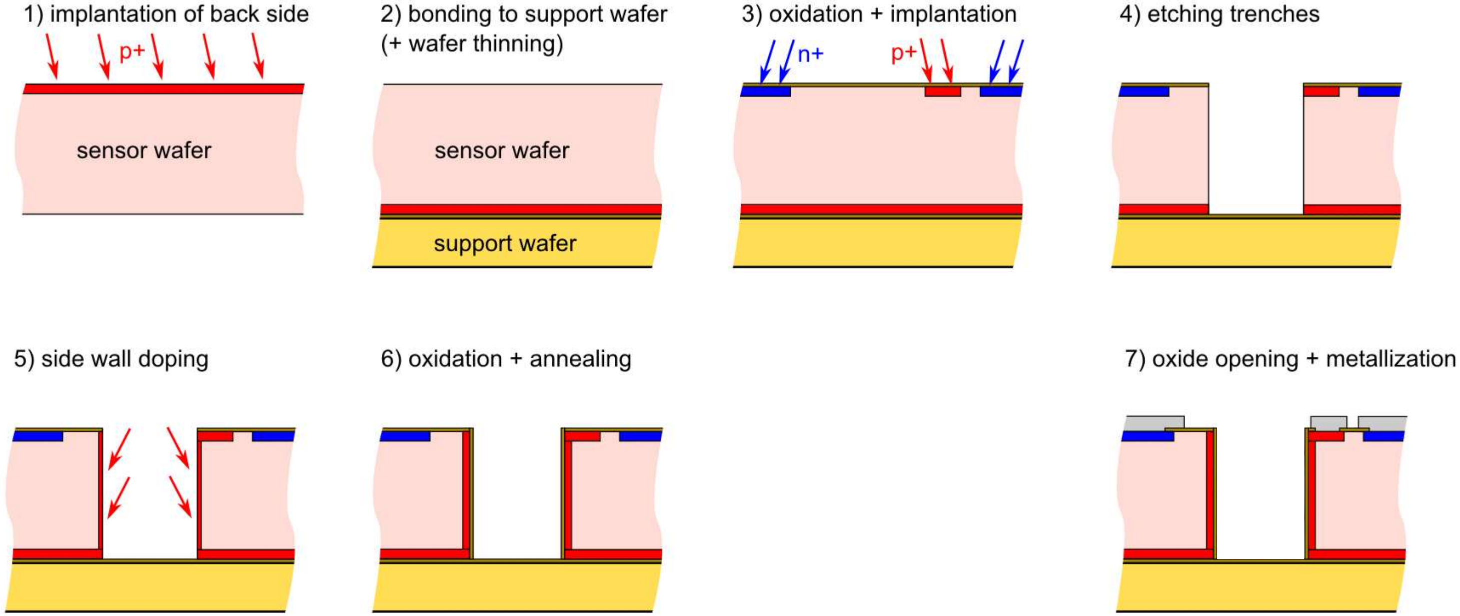




active edges wafer run

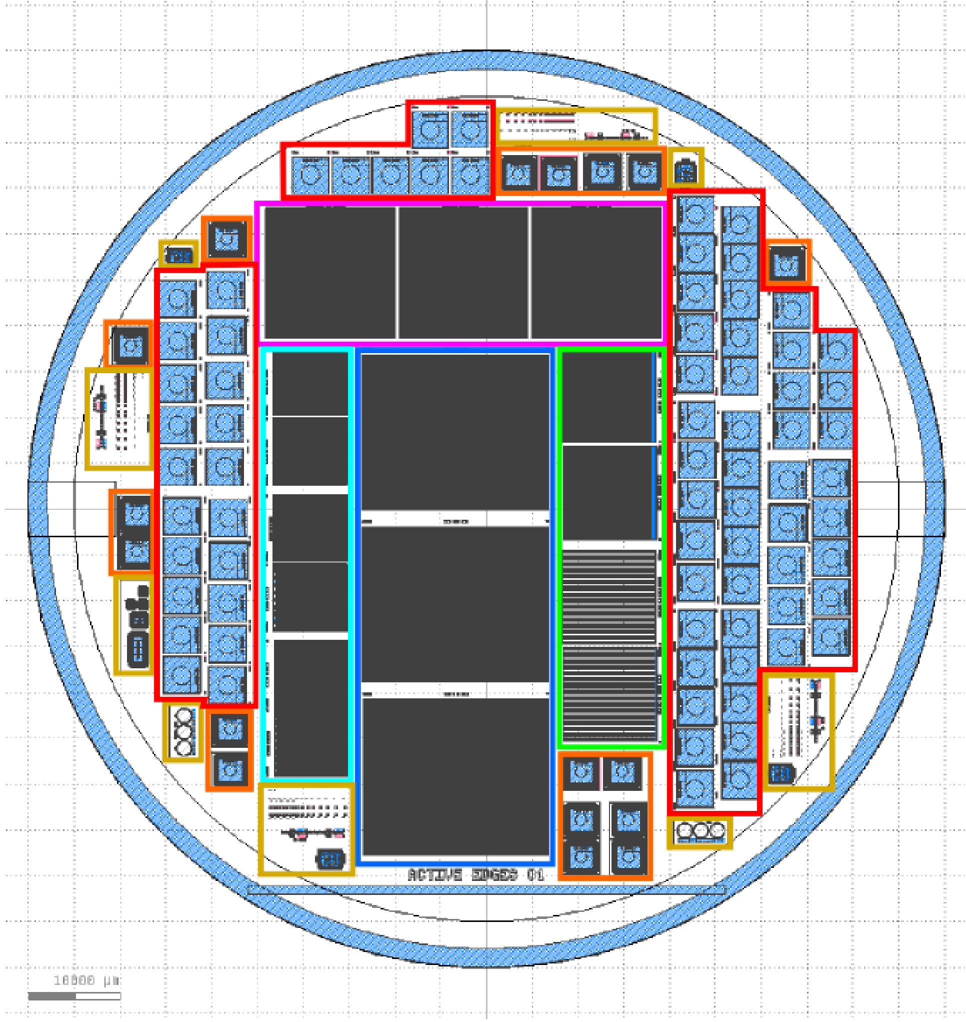
- reduction of inactive sensor edge by doping of side walls
- several parameters are varied which can be compared
  - p- and n-type bulk
  - sensor thickness (300 & 100µm)
  - three side wall doping methods
  - trench widths
- numerous edge designs had been simulated
  - most promising ones were implemented in the layout

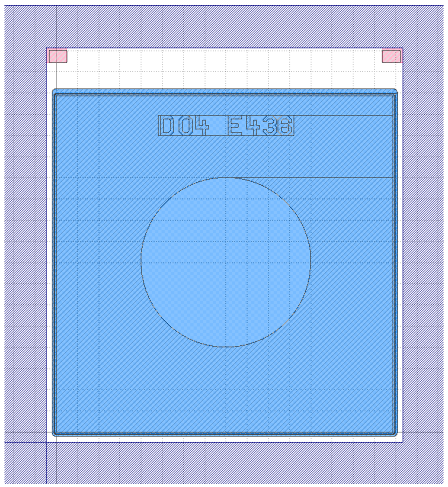




active edges – wafer layout

- numerous active edge diodes with systematic variations of edge design
- reference diodes
- FE-I4 & FE-I3 SCS
  - mod p-spray
  - nomod p-spray
- micro strip sensors (80µm pitch)
- MediPix/TimePix sensors
- test structures

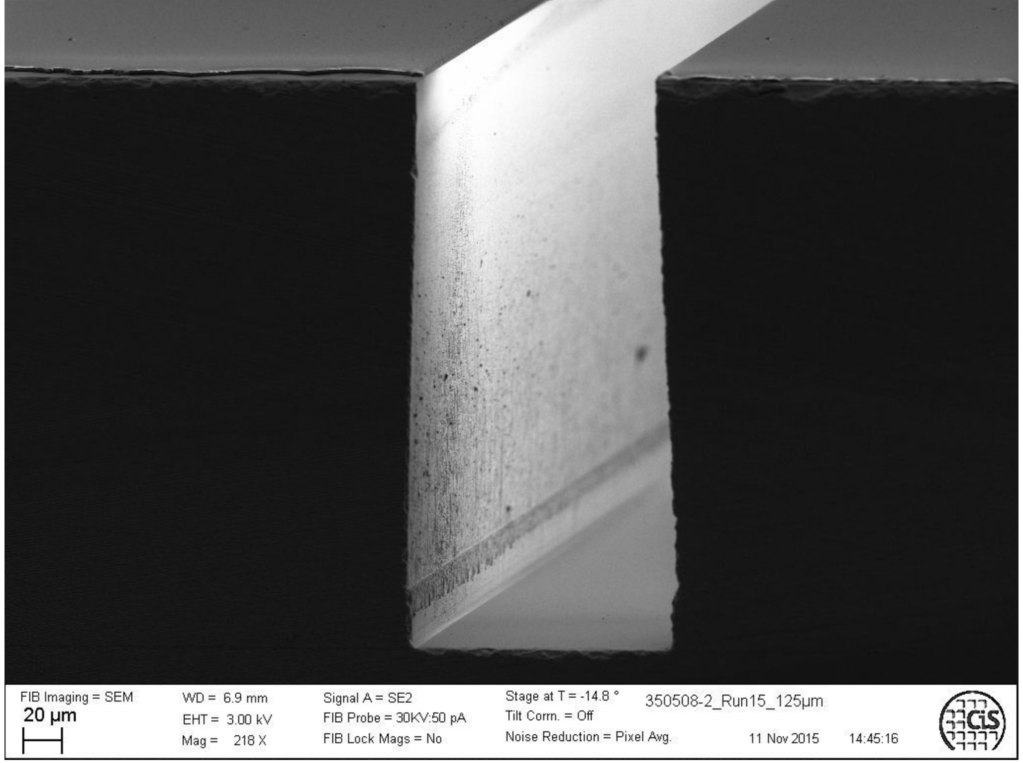


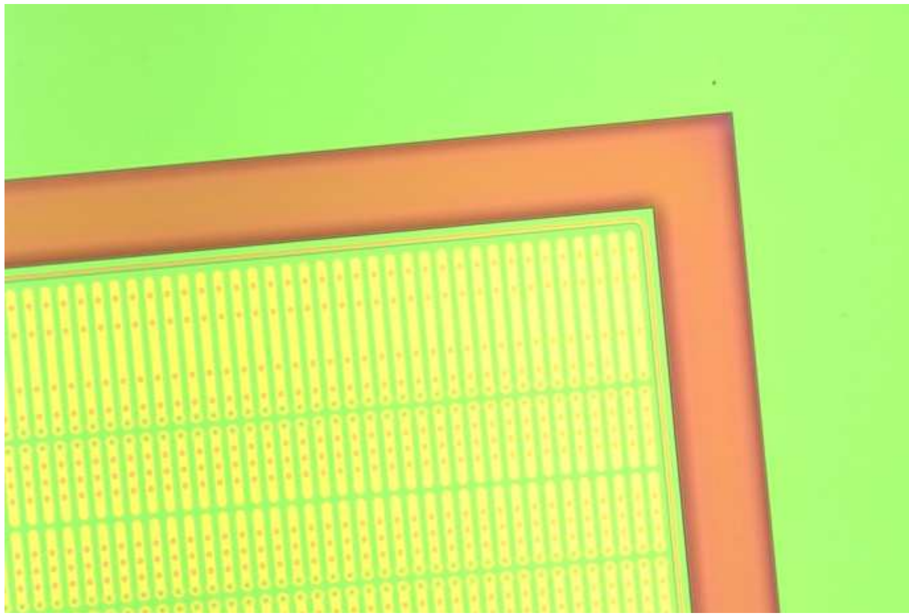


active edges wafer run
- status

- challenging step of the ICP trench etching has been performed for the thick wafers
- didn't have much experience up to now
- dummy trials to adjust etching parameters
- still have to optimize the etching homogenity at the wafer edge
- anyhow, most of the side walls look fine

- next step is the side wall doping
  - 4-quadrant ion implantation
  - plasma immersion ion implantation
  - BBr_3 doping from gaseous phase
- thin wafers are processed a bit later





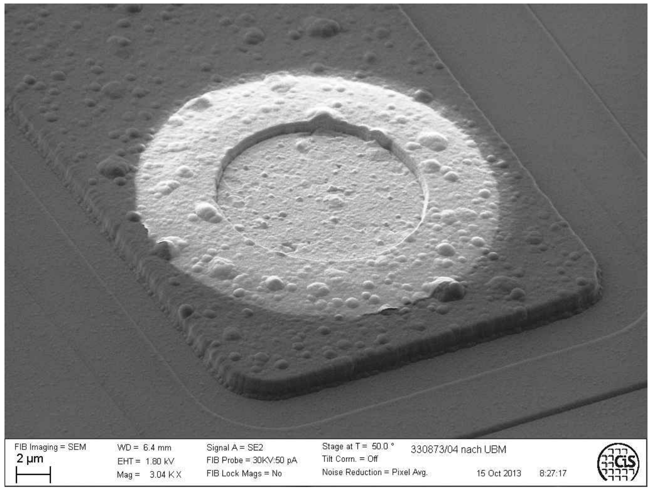
UBM @ CiS

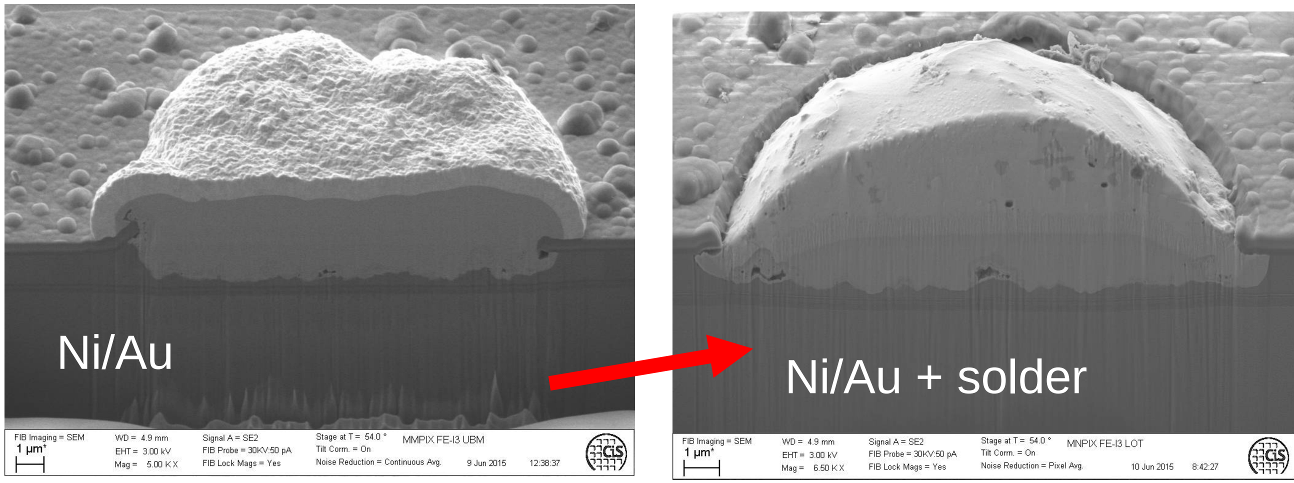
mask-based electroless Ni-UBM

- done for CMS-Pixel production, in combination with In-bumps
- process is partly outsourced
- relatively thin film on sensor surface
- already tested with (IZM) solder bumps

mask-less Ni-UBM

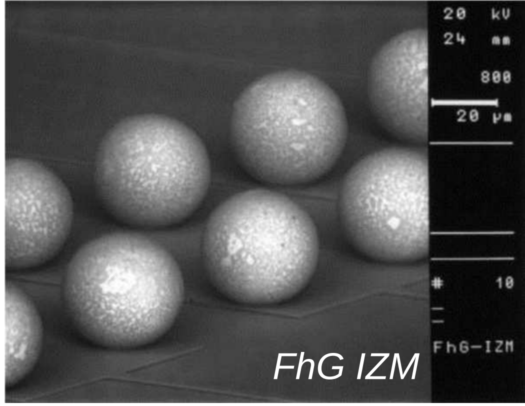
- Ni is growing on Alu surface on all passivation openings
- covered with Au layer
- can be done in-house
- already tested with immersion soldering to obtain solder caps

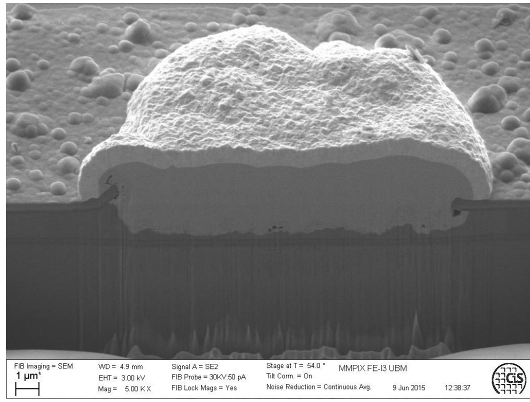


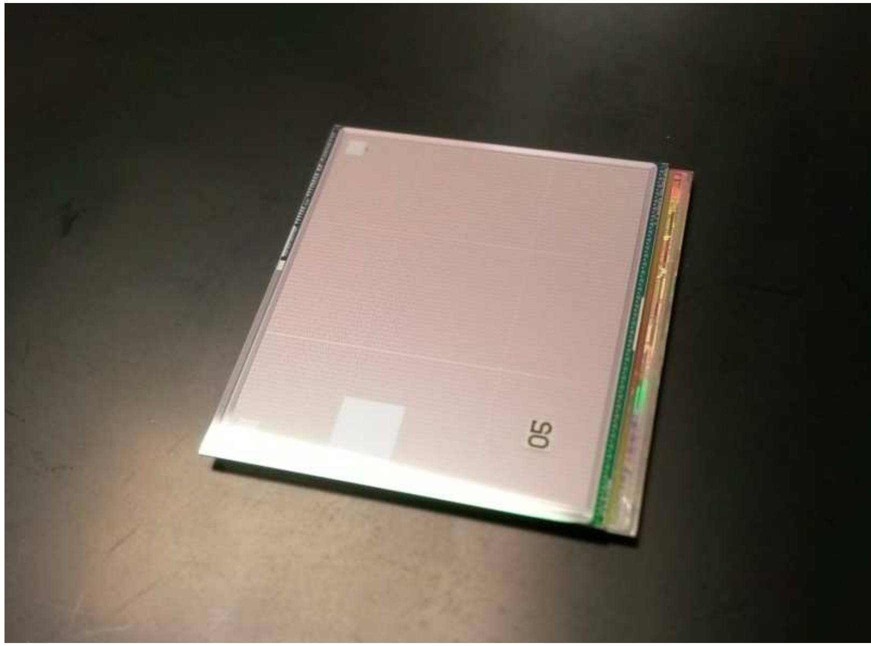


Flip Chipping

- first trials at CiS to flip chip FEs with IZM solder bumps with Ni-UBM
- large size of the FE-I4 is challenging for our fineplacer
- in principle the alignment works
  - not yet 100% reliably reproduceable
  - have to gain some more experience
- next steps:
  - read-out assembly to get some statistics of disconnected bumps
  - try out our Die-Bonder for flip chipping
  - investigation of solder paste print technology is in preparation
    - could be a low cost alternative for solder bumps







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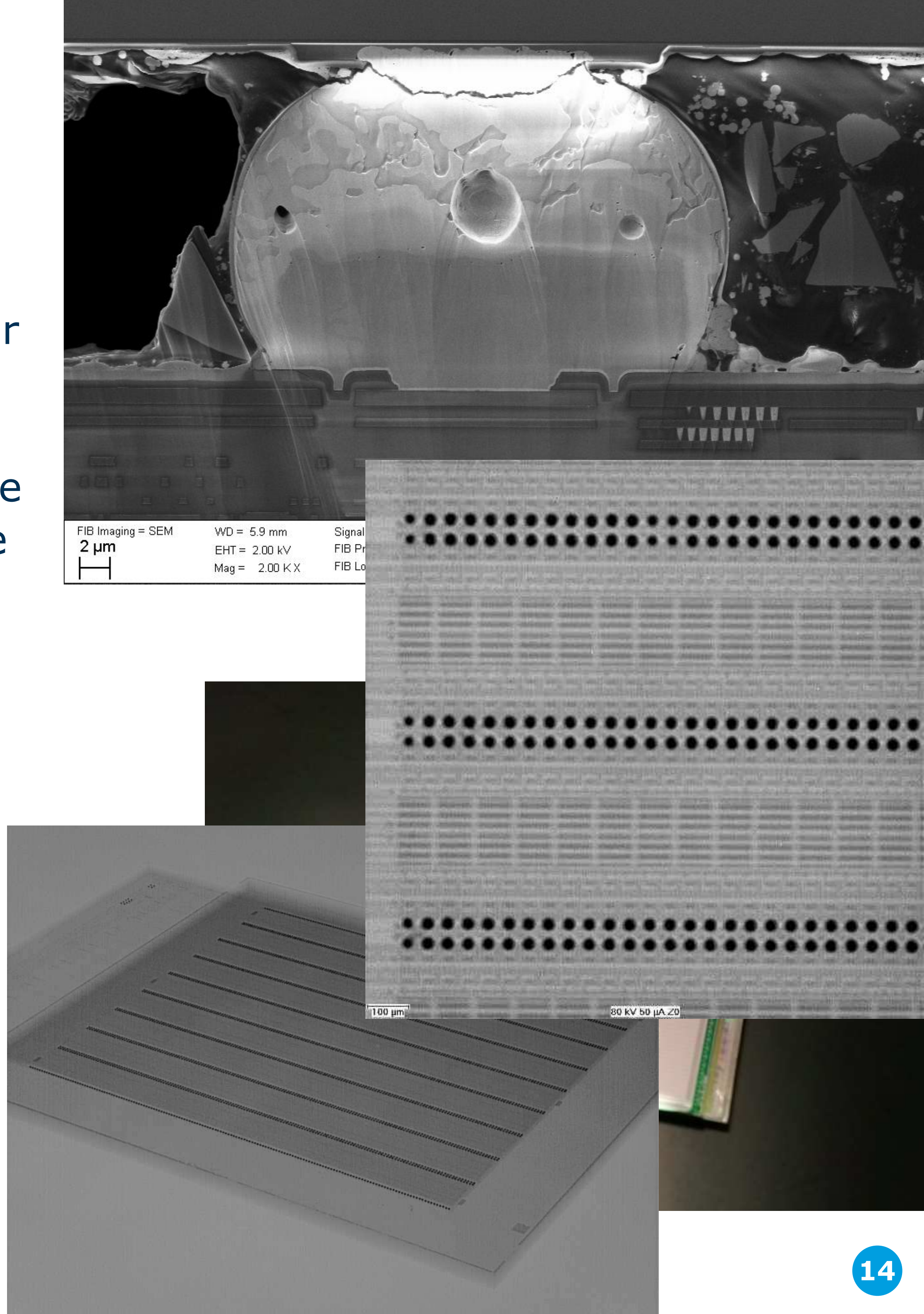

Conclusion & Outlook

- the implementation of the cavity etching technology to produce thin planar sensors without large additional expenses has been demonstrated
  - 4‟ production shows proof of principle
  - next step is the transfer to 6‟ wafer size
  - 4‟ test wafer for SSD-lab is near completion
- active edge wafer run is progressing
- NitroSil wafer run to study N_2-enrichment has started
- UBM & flip chip technologies are followed up
  - first assemblies have been produced
  - process optimizations are ongoing

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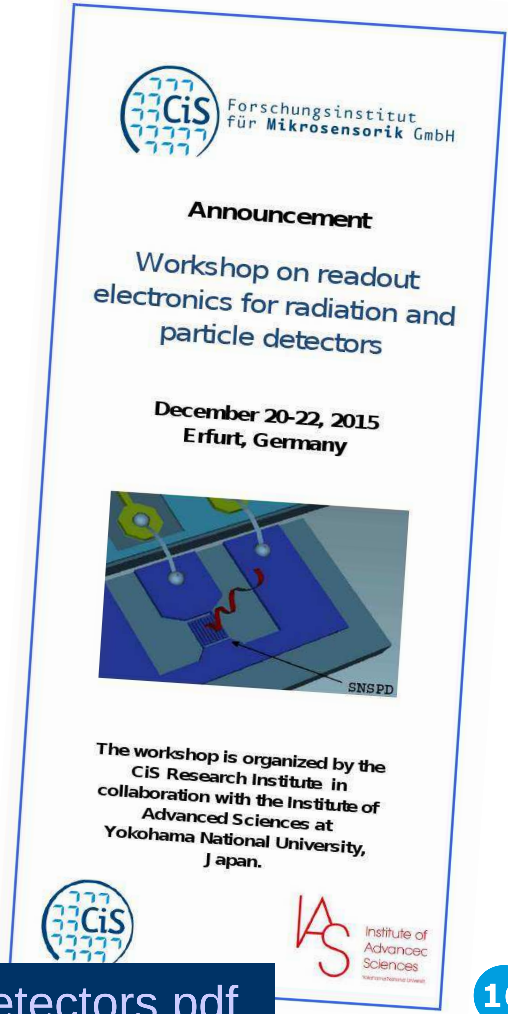


http://www.cismst.org/fileadmin/user_upload/news/flyer-detectors.pdf

Backup

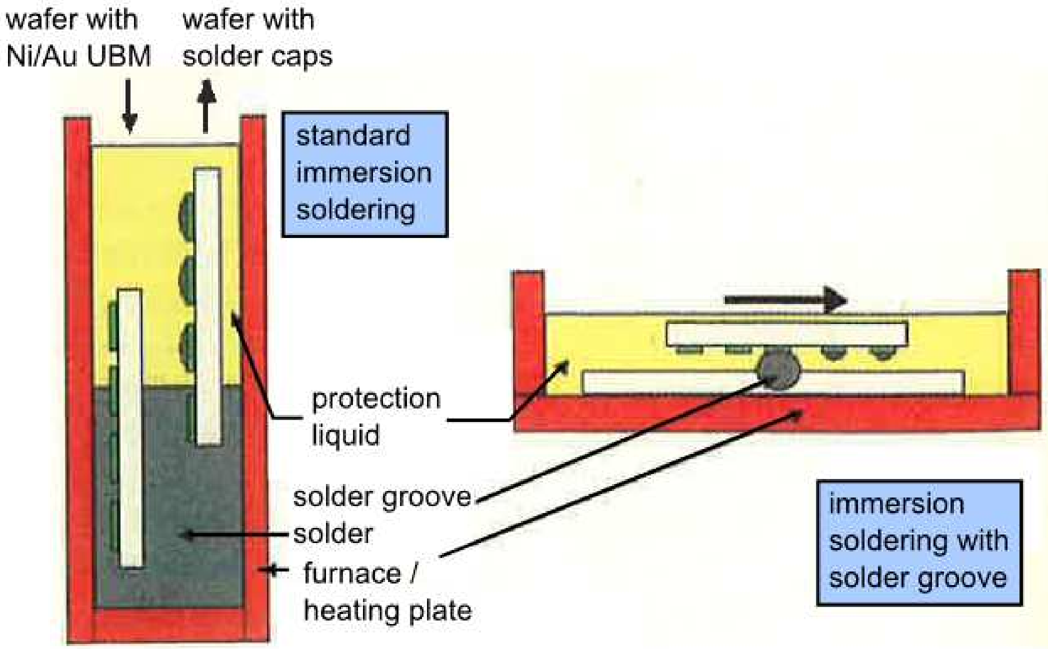
Flip-chipping at CiS

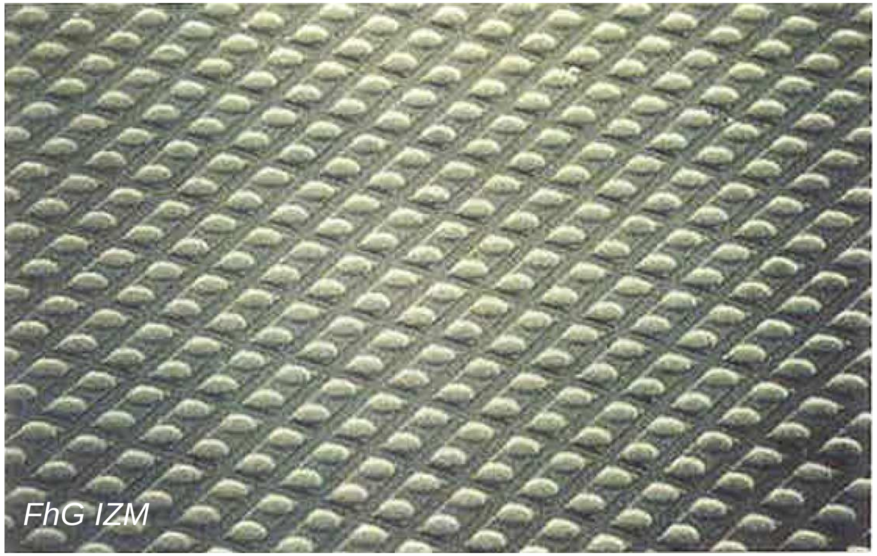
Fineplacer

Die-Bonder

Immersion Soldering

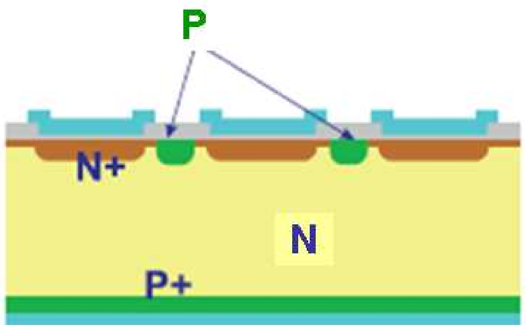
- wafer or diced sensor
  - is immersed into solder bath
  - moves along a solder filled groove
- solder adheres to Ni/Au-UBM, forms caps

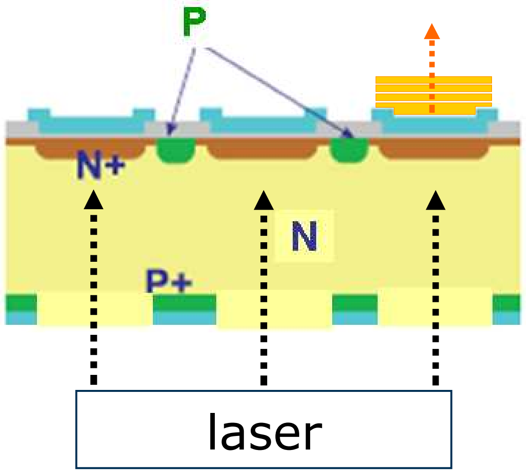




LIP – Light Induced Plating

- epitaxial growth of the UBM is stimulated by laser light
- UBM is only growing on the passivation openings
- openings in the back side metal could be necessary
- no additional process steps necessary
  - no plating base / resist
  - no stripping / etching
- less cost & time consuming



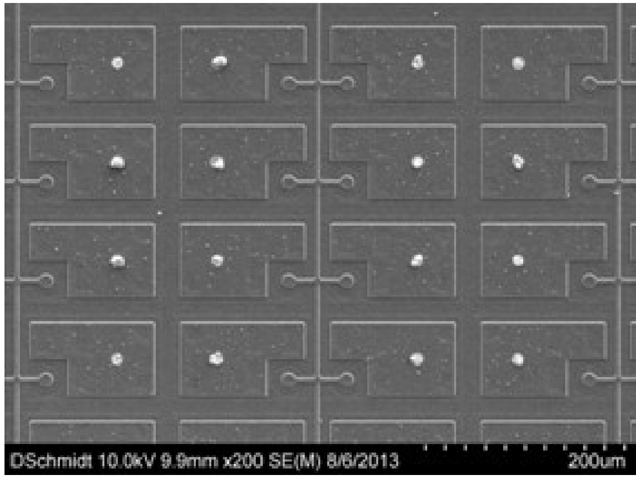


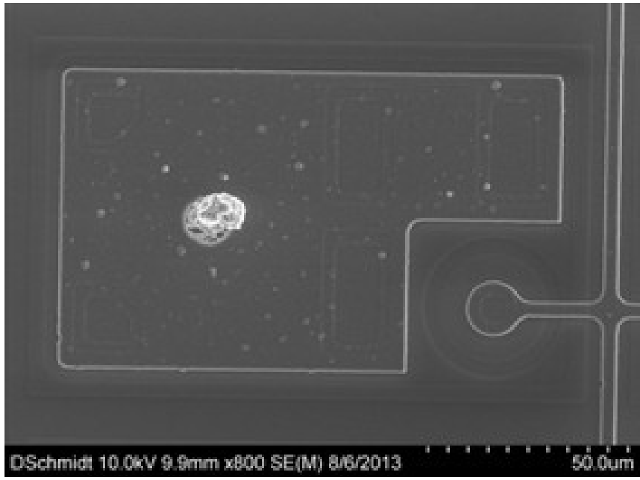
cooperation with TU Ilmenau

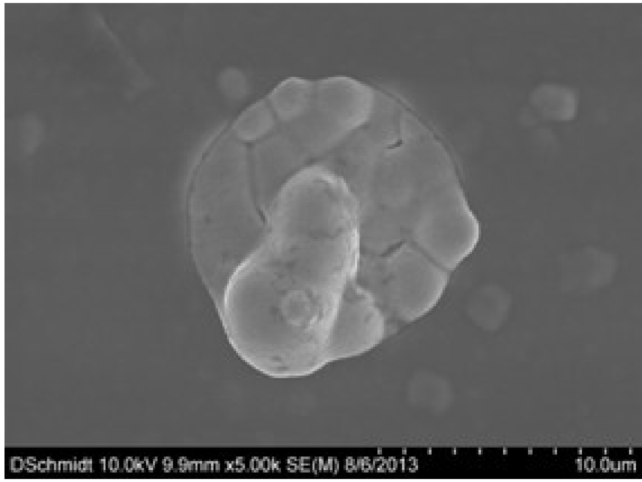
LIP – Light Induced Plating

- first trials done on CMS-pixel sensors (no difference to ATLAS pixel)
- works in principle
- homogenity of Ni is improvable
  - also old sensor with bad Alu surface used
  - expect better results with new sensors

- next steps
  - combine Ni-UBM (LIP or chemical) with LIP solder
  - alternative to immersion soldering
  - different electrolytes should be feasible
    - Sn, SnAg, In, In/Sn
    - possibly no UBM necessary
  - additional usage of lacquer mask to grow higher solder pillars



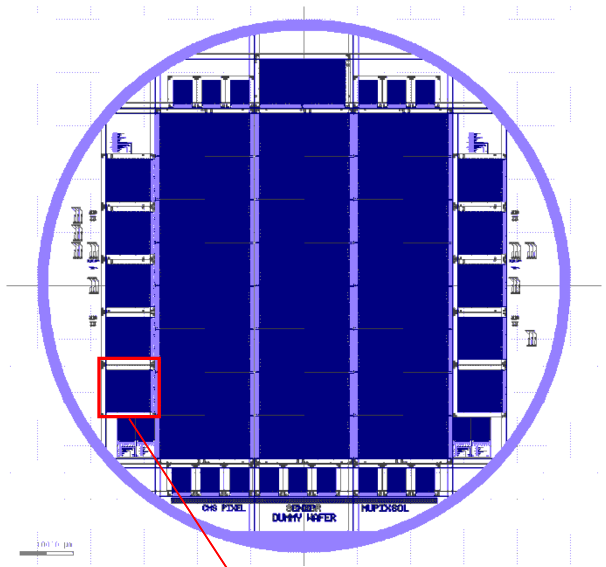


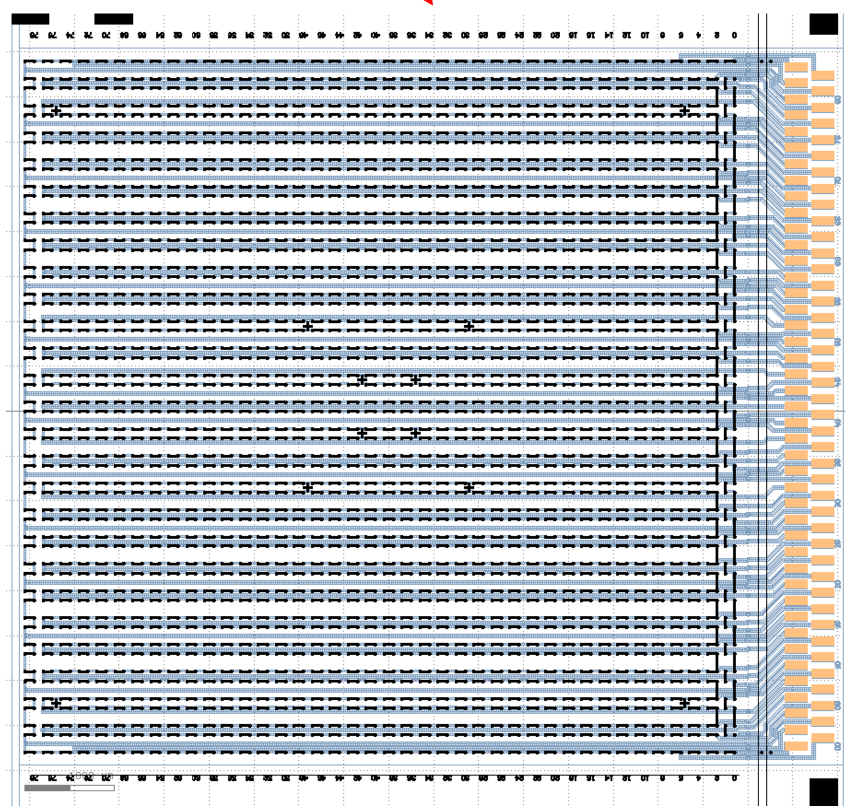


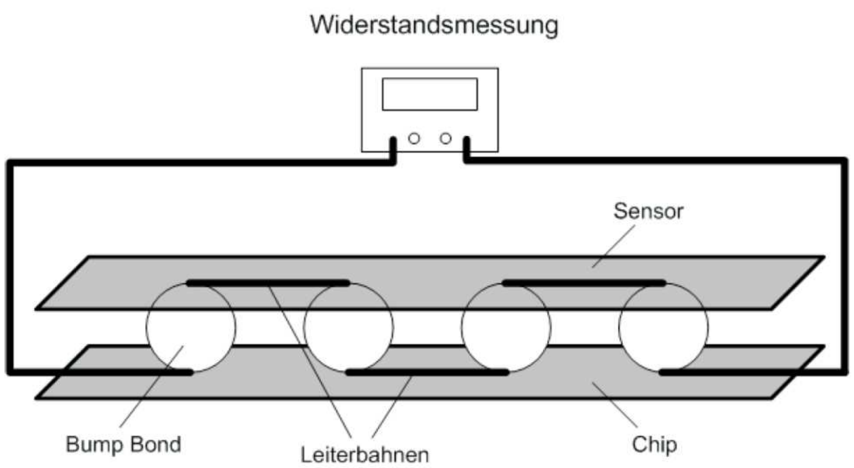
cooperation with TU Ilmenau

Daisy Chains

- daisy chain dummies in production
- geometry is based on CMS Pixel
- different bump pad diametres are tested
- possibility to try out
  - different UBM and solder variants
  - large quantity
  - different sensor/chip sizes







defect engineering

project in progress:

- improvement of the radiation hardness of silicon sensors by defect engineering

plans:

- analysis of defects in silicon during and after the processing, possibly also after irradiation
- investigation of the reason for increase of radiation hardness by oxygen
- optimize the defect configuration
  - investigate effect of other elements for bulk enrichment
  - adaption of essential process steps
    - influence of thermal budget to the oxygen defect configuration
    - influence of thermal donors
    - tempering
    - dielectrical layers
- tools:
  - simulation
  - charge carrier life time
  - low-temperature FTIR
  - DLTS