TCAD Simulations
HV-CMOS AMS 0.35 μm Reach-Through Diode

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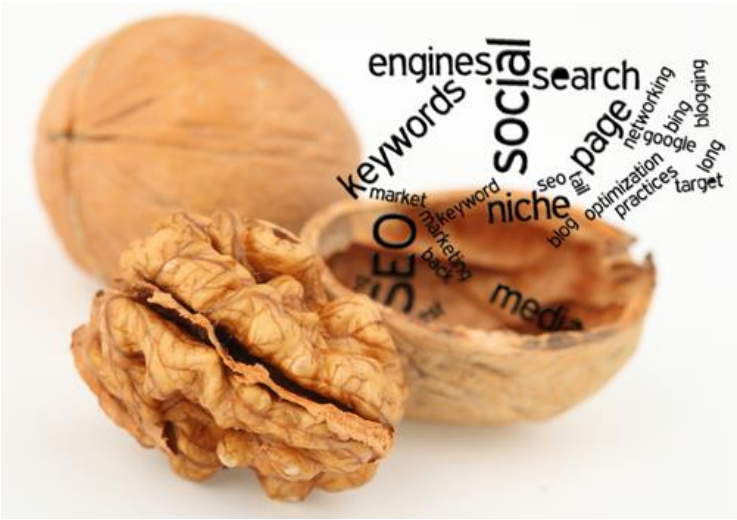
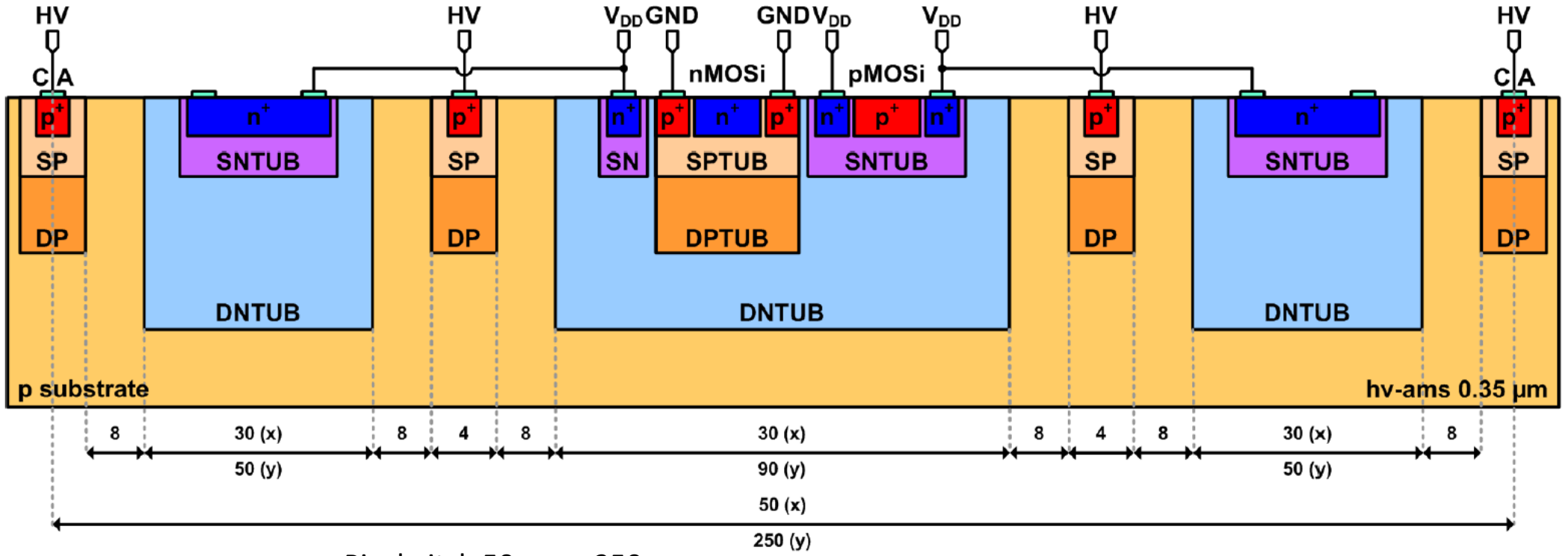
Outline

- HV-CMOS 0.35 mm Reach-Through Diode
- Gaussian Doping Model, I-V
- Gaussian Doping Model, edge TCT
- HV-CMOS + CSA/Shaper Front End
- HV-CMOS + CSA/Shaper Front End & SEE



Liverpool Univ. HV-CMOS sensor



- Pixel pitch 50 µm x 250 µm
- Discontinuous DNTUBs not to increase sensor capacitance
- DPTUB guard rings (HV) of 2 neighbouring pixels are overlapped
- Sensor with round shaped corners to avoid peak electric fields
- Separation between DPTUB and DNTUB is 8 µm everywhere
- P+ guard ring around the nMOSi transistor área is 1.8 µm everywhere

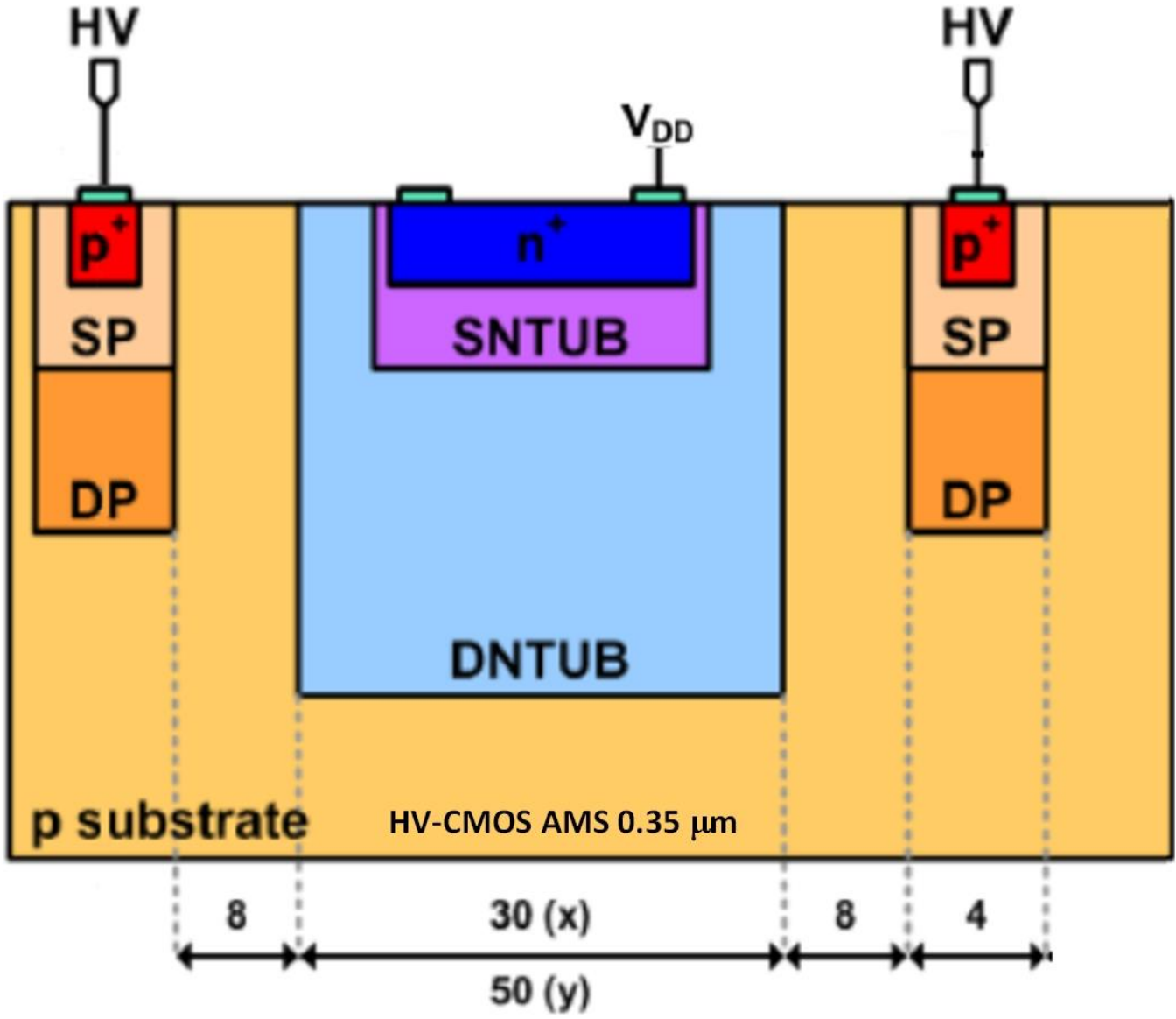
Eva Vilella, ITk Week CERN 23-27 Feb. 2015, https://indico.cern.ch/event/361445

HV-CMOS 0.35 μm AMS Technology kit

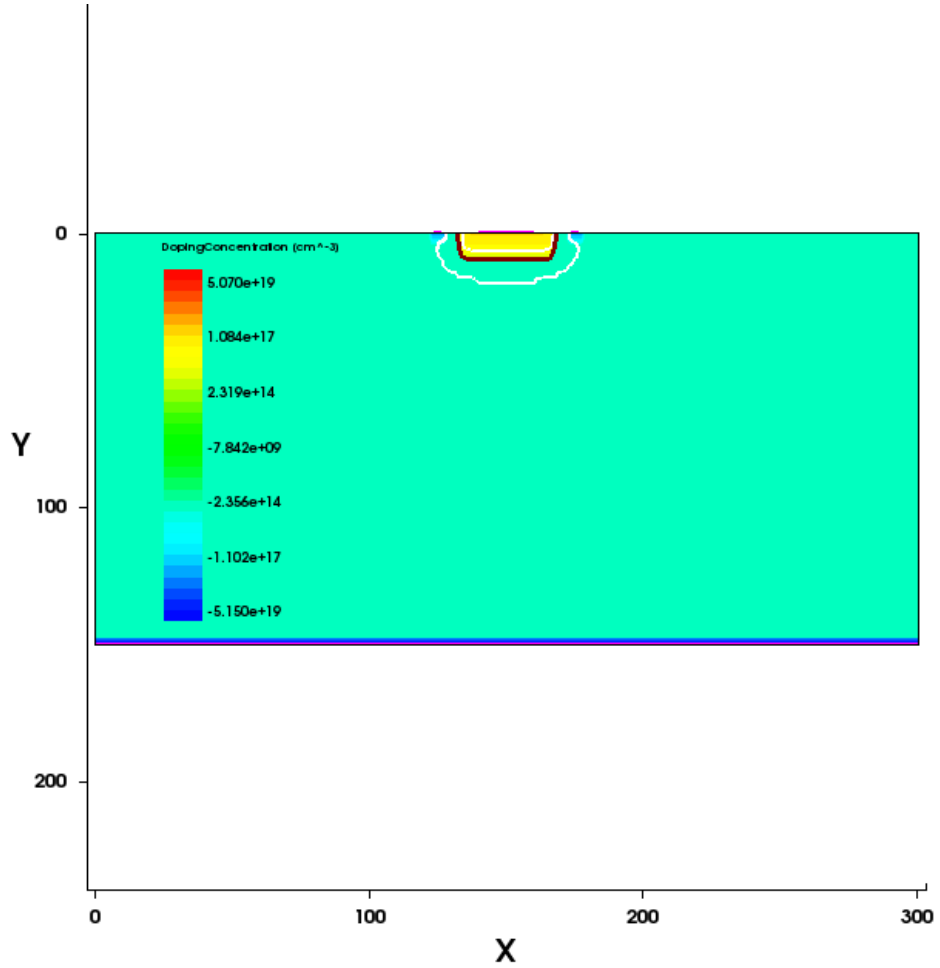
- Doping profiles? (*secret*), implant and well depths? (*confidential*)
- Reverse Engineering for a Reach-Through Diode biased by p-implants and/or backplane:
  - Reach-Through Diode equations
  - p-substrate doping to resistance equations (Resistance= 20 Ω-cm)
  - AMS public information
  - AMS kits confidential information
  - SIMS (Secondary Ion Mass Spectrometry) doping analysis public data on AMS HV-CMOS
- educated guesses

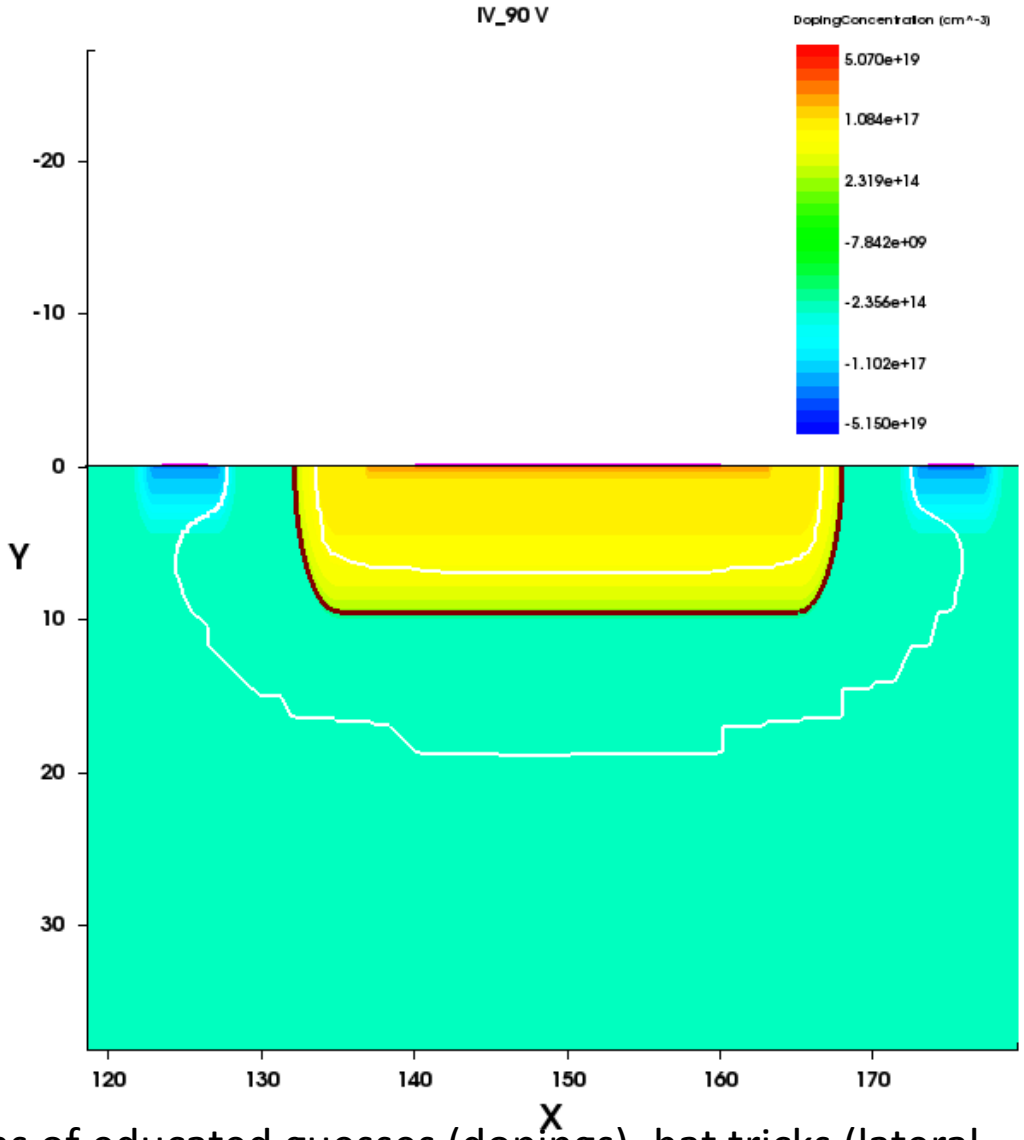
Reach-Through Diode Model

- First guess: after document (depths) and mathematical model analysis (doping) first try with constant doping profiles
- After several IV simulations and comparisons with conventional PiN diode models, the parametric search space is reduced
- I-V simulations for the constant doping profile, reach-through diode biased from p-implants and/or backplane.



Gaussian Doping Profiles

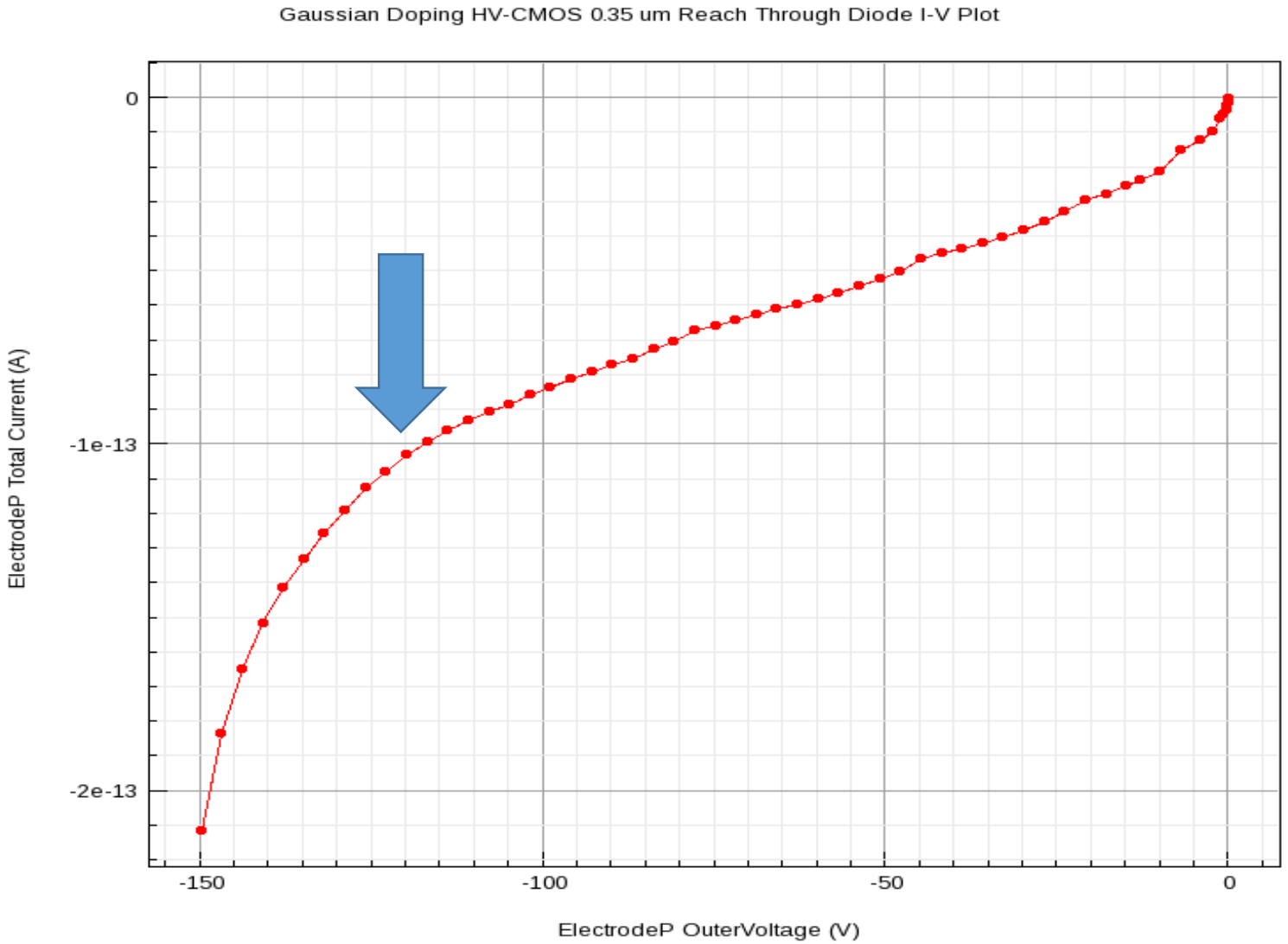




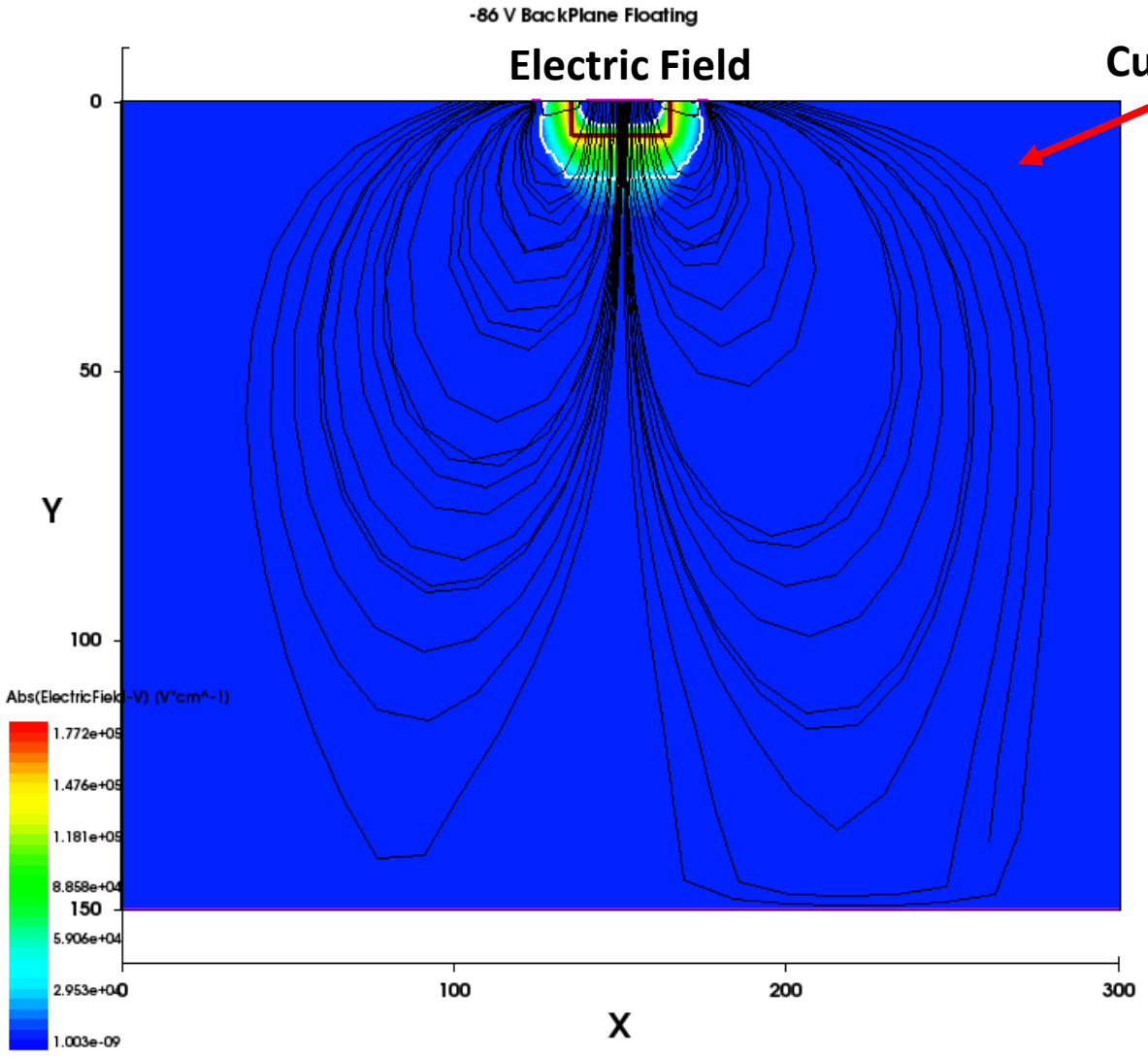
A simulation of the technological implantation process by means of educated guesses (dopings), hat tricks (lateral extension) and dozens of IV simulations

Gaussian doping I-V curve (n+ grounded, backplane and p-implant bias)

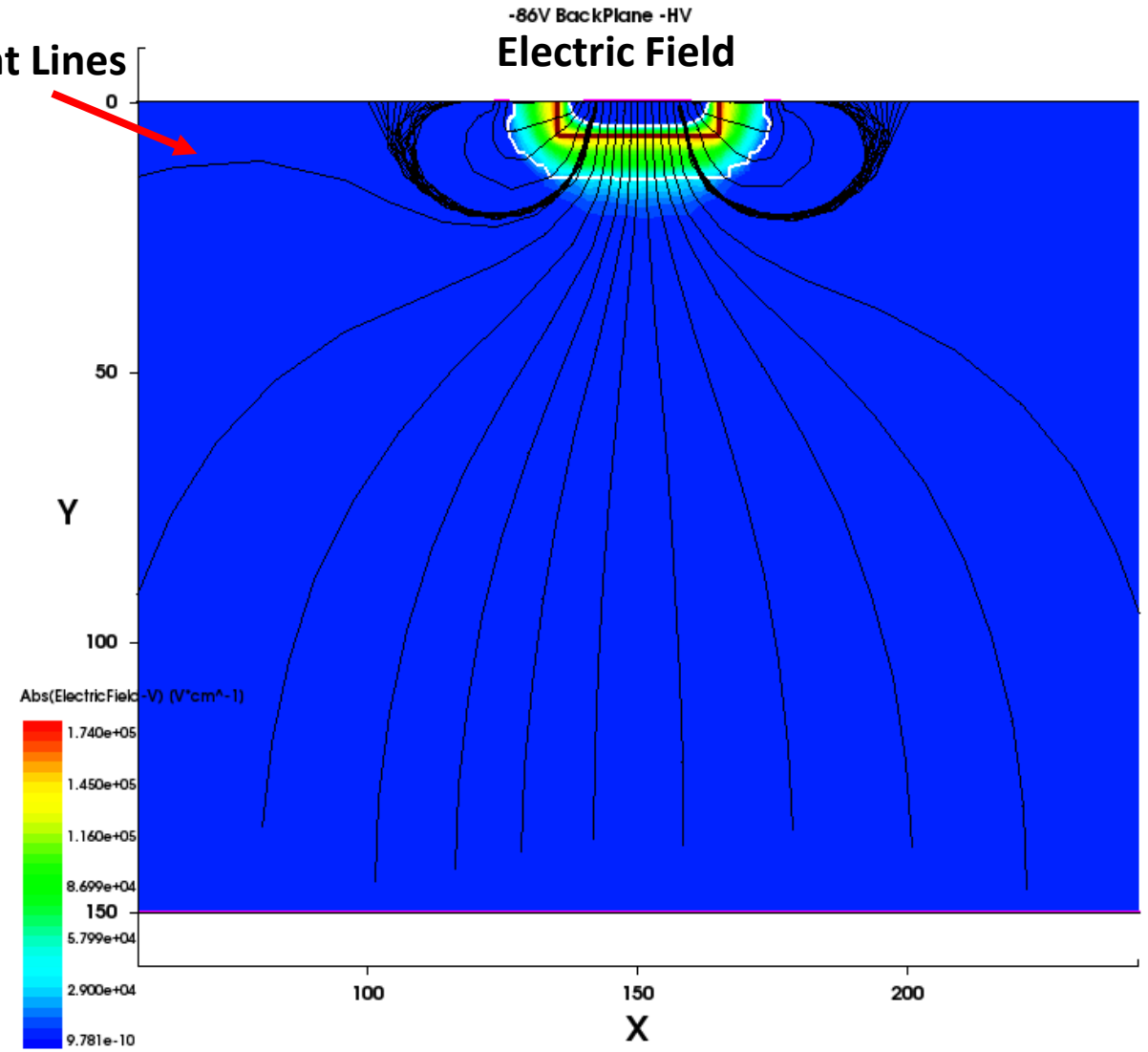
- Initial dopings from the previous results
- For a 20 Ω-cm substrate: Vbreak ~ -120 V
- After tweaking in the process parameters, the I-V curve starts breaking at ~120 V
- This is the final model (at the moment)
- Typical bias at the SSD experiments



Biasing HV-CMOS 0.35 μm AMS



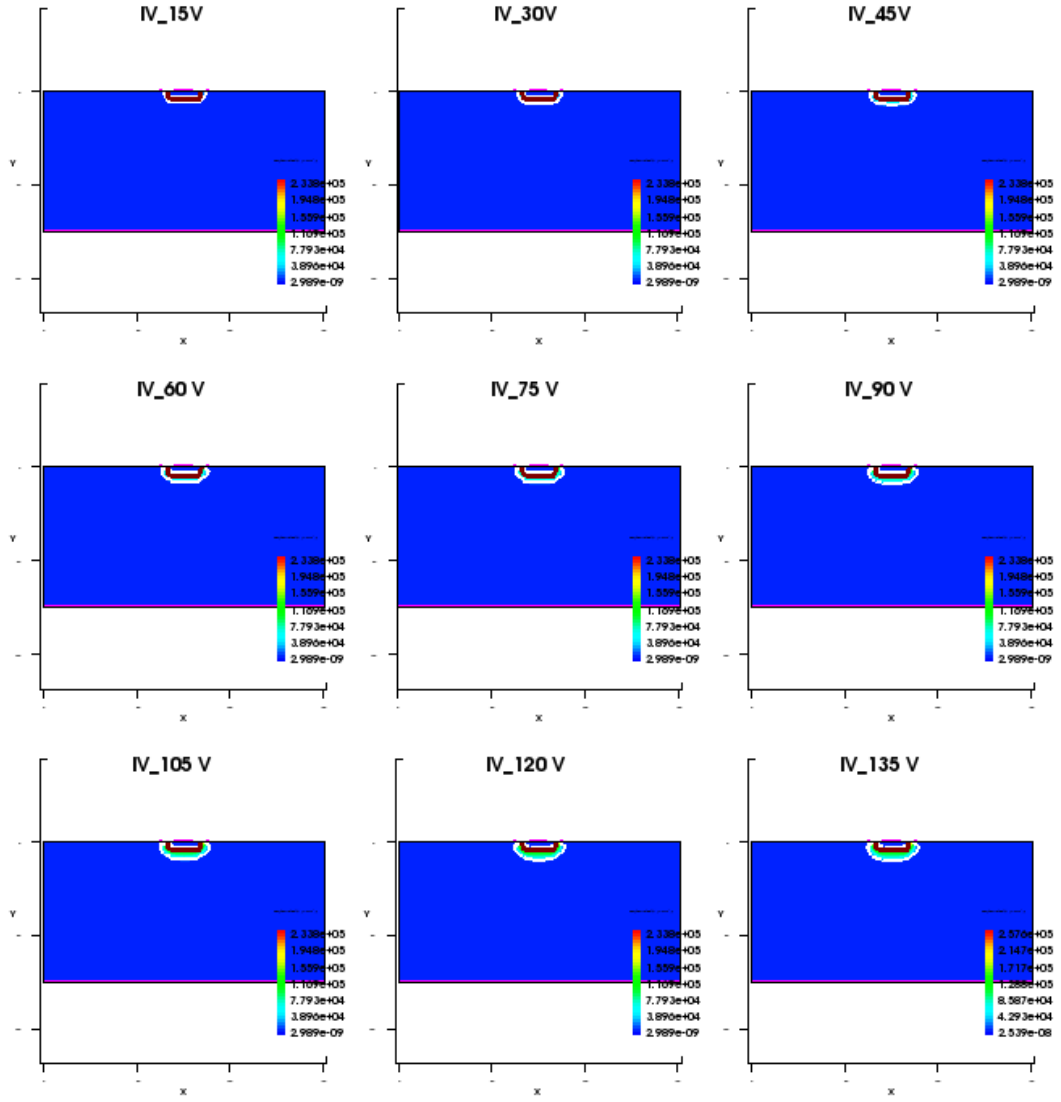
Current Lines

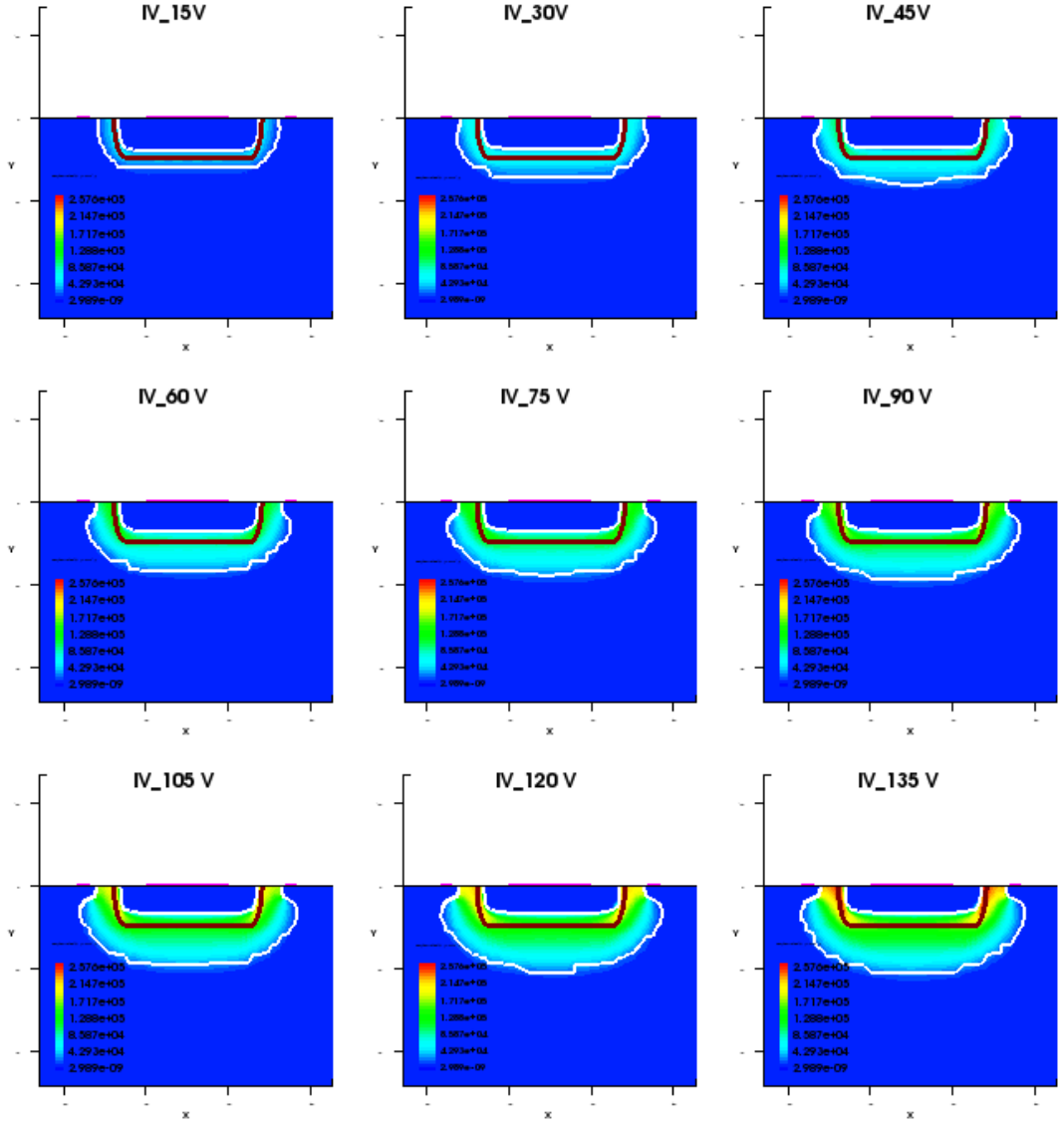


BackPlane Floating, p-implant bias (-86 V), 3.3 V at n+ contact

BackPlane bias, p-implant bias (-86 V), 3.3 V at n+ contact

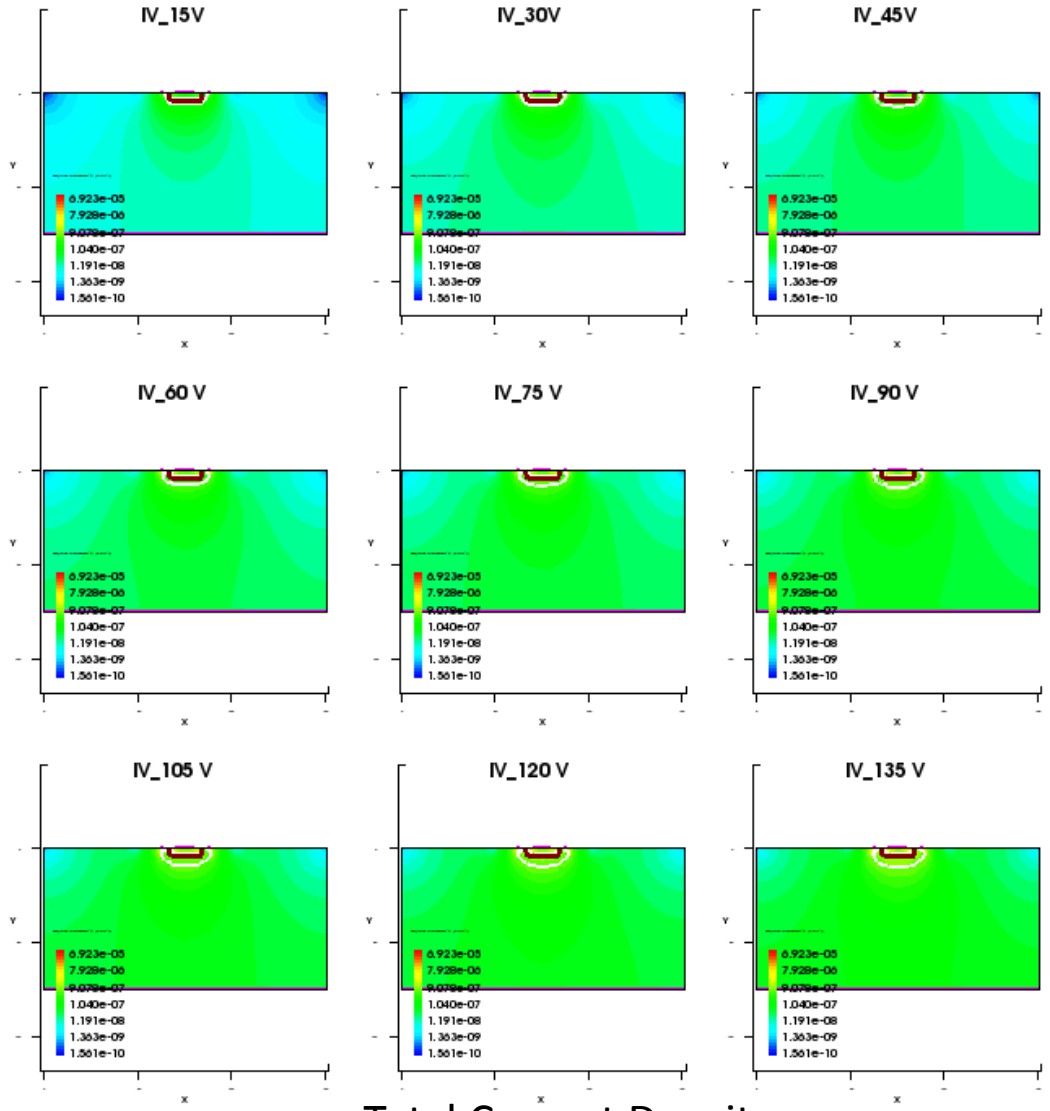
Gaussian Doping: Electric field



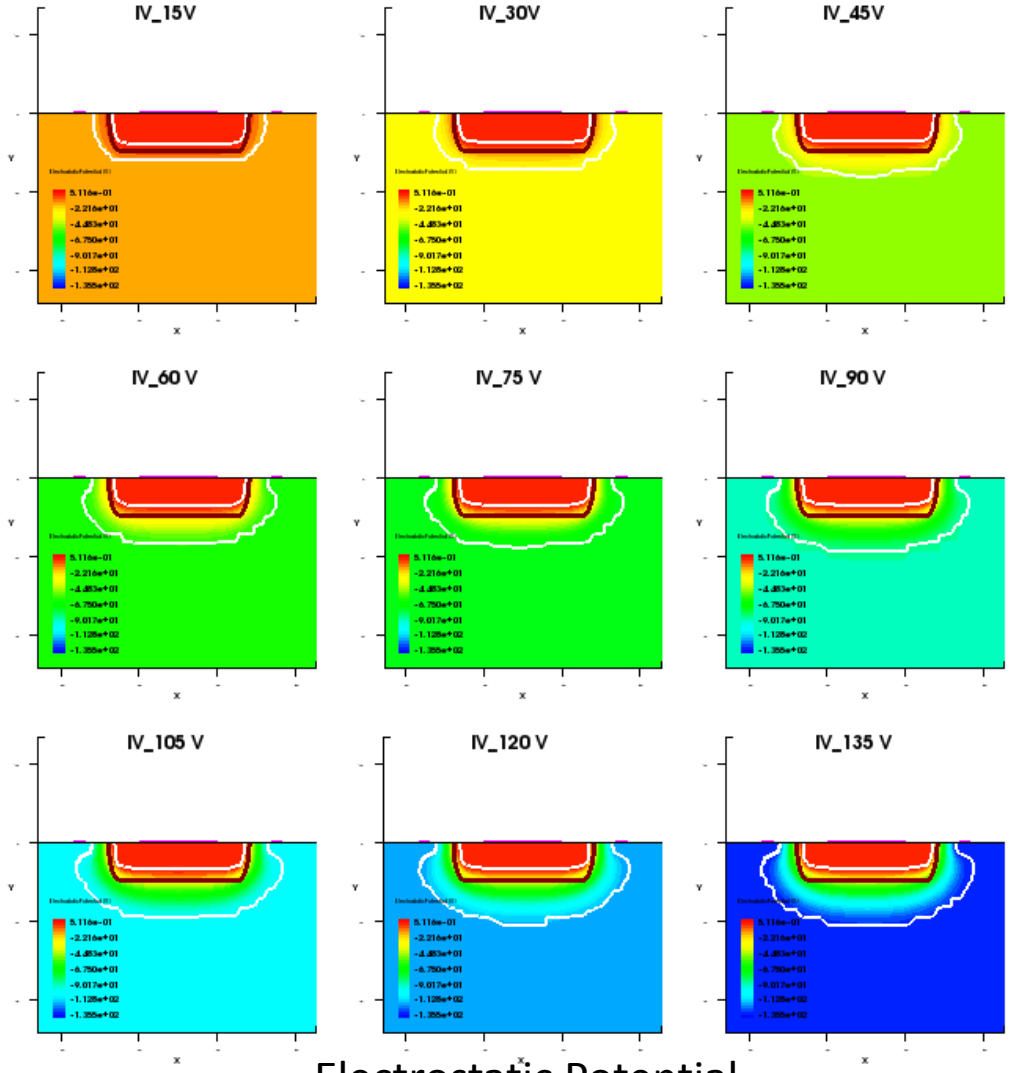


Bias: -15, -30, -45, -60, -75, -90, -105, -120, -135 V

Gaussian Doping: Total Current, Electrostatic potential



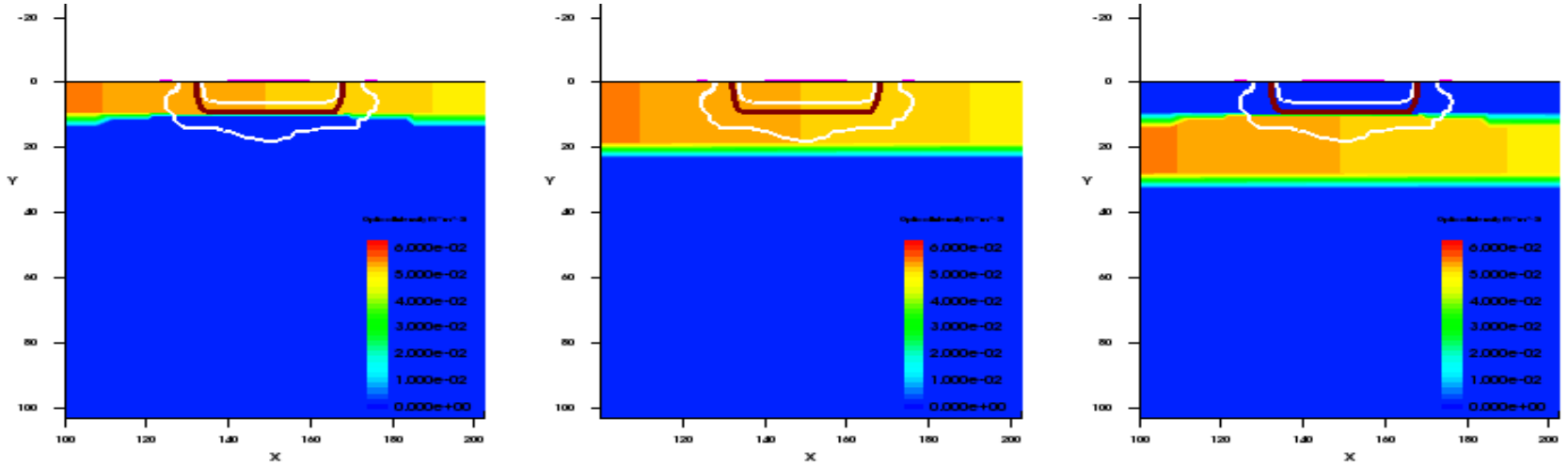
Total Current Density

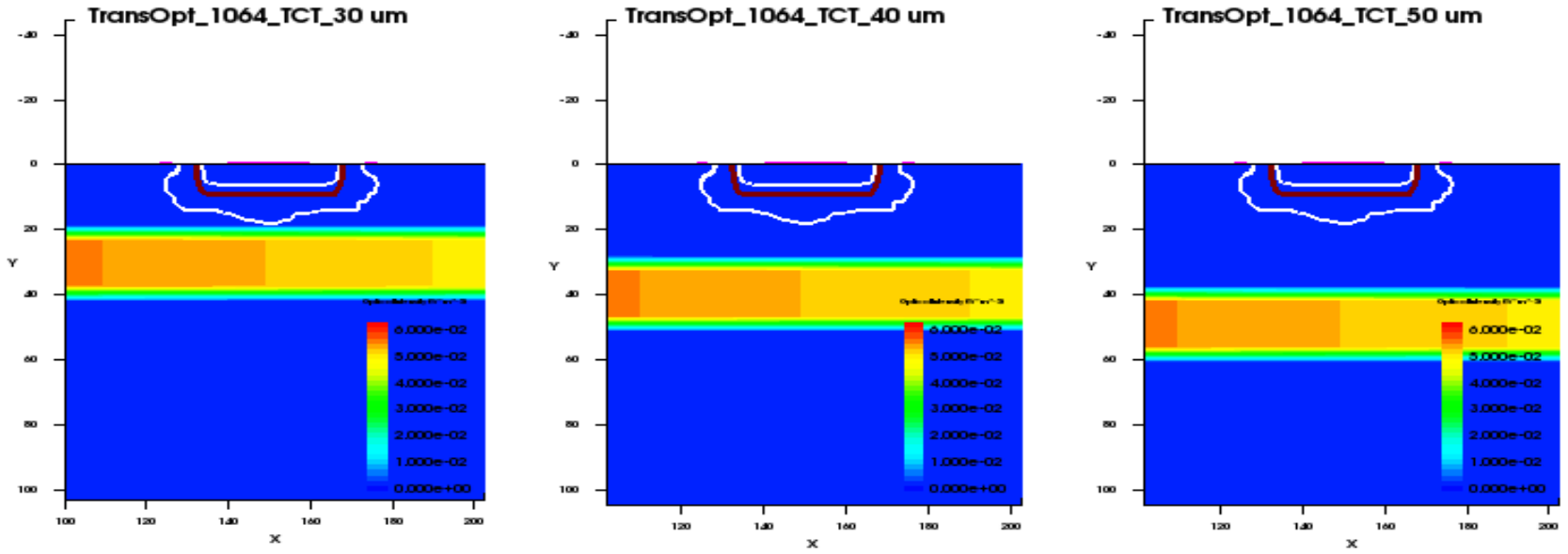


Electrostatic Potential

Bias: -15, -30, -45, -60, -75, -90, -105, -120, -135 V

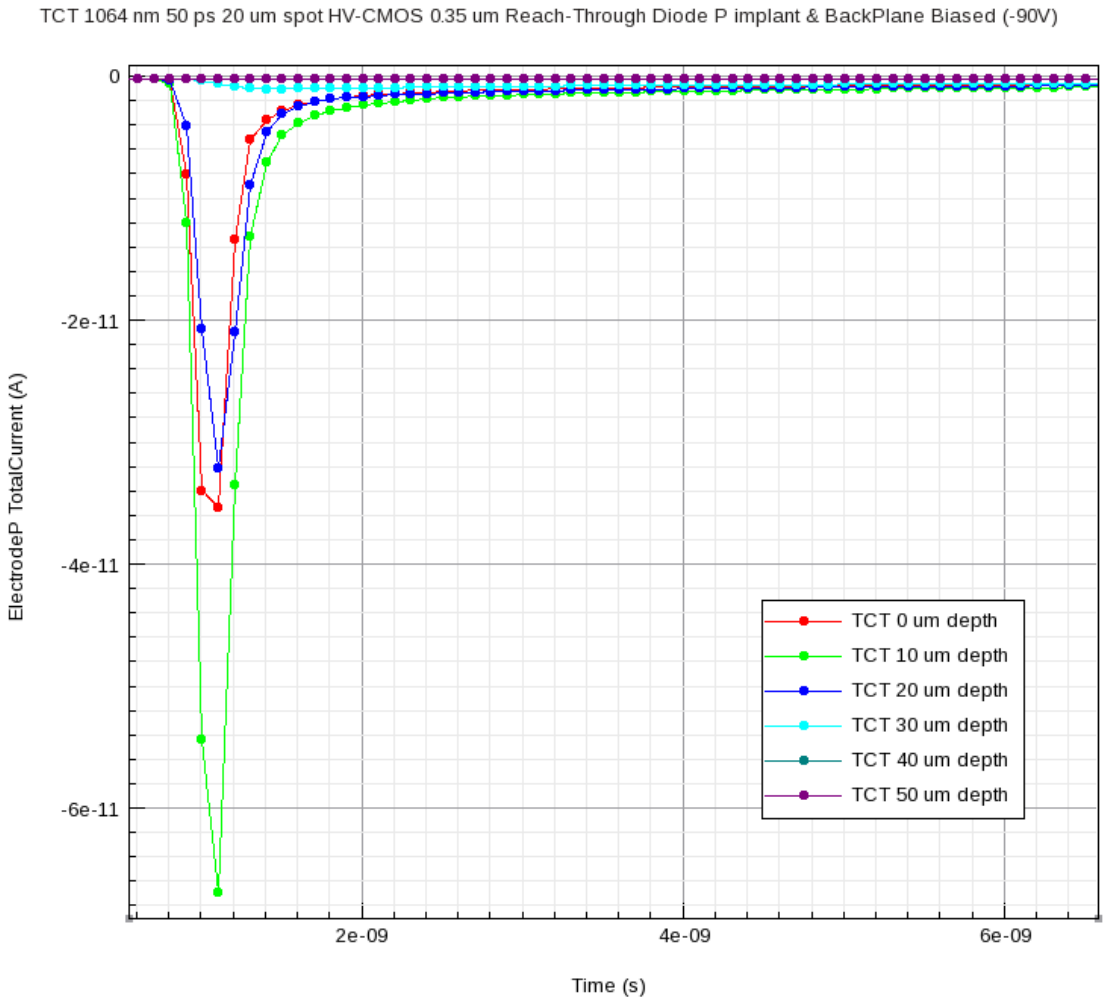
eTCT Gaussian Doping HV-CMOS AMS 0.35 μm Reach-Through Diode

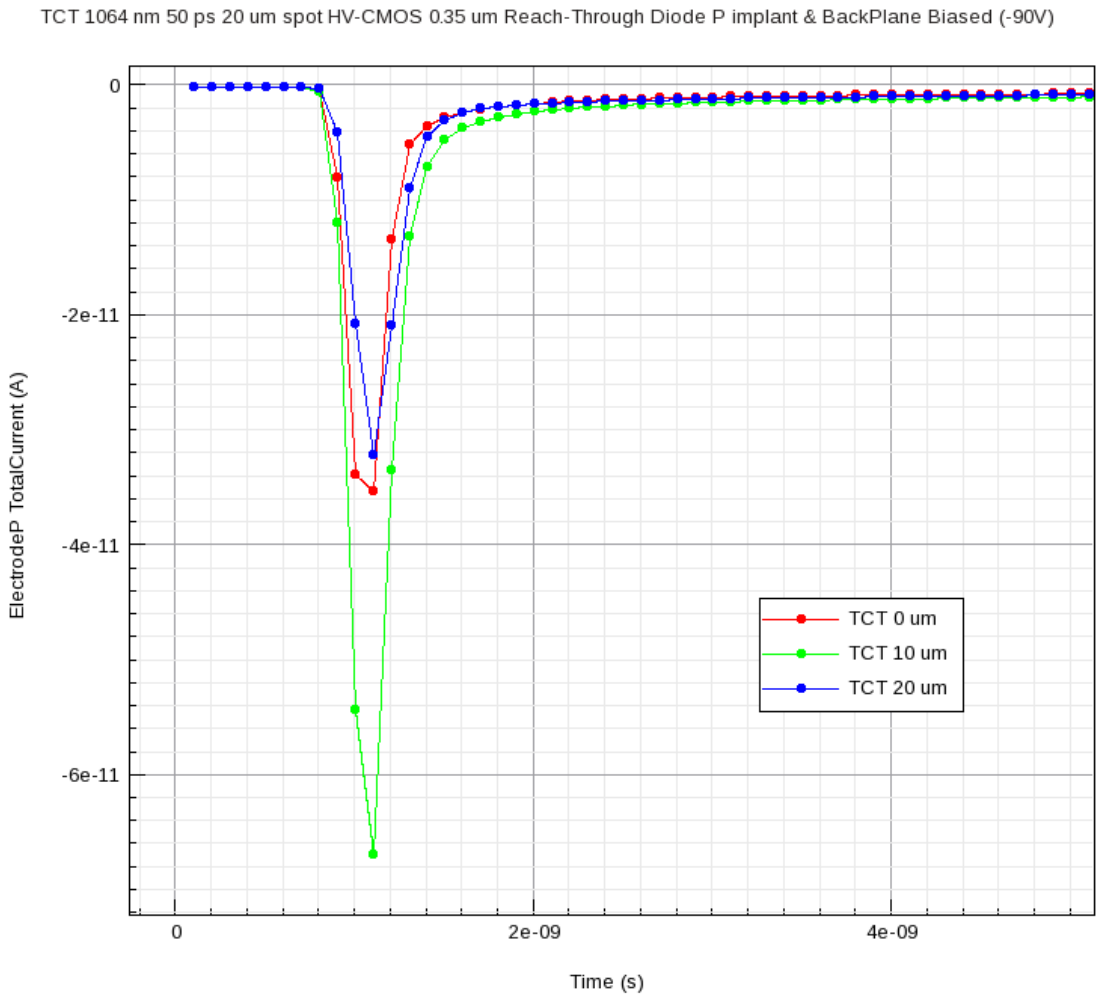




- 1064 nm, 100 ps, 20 μm spot diameter
- Illumination at 0, 10, 20, 30, 40 and 50 μm depth

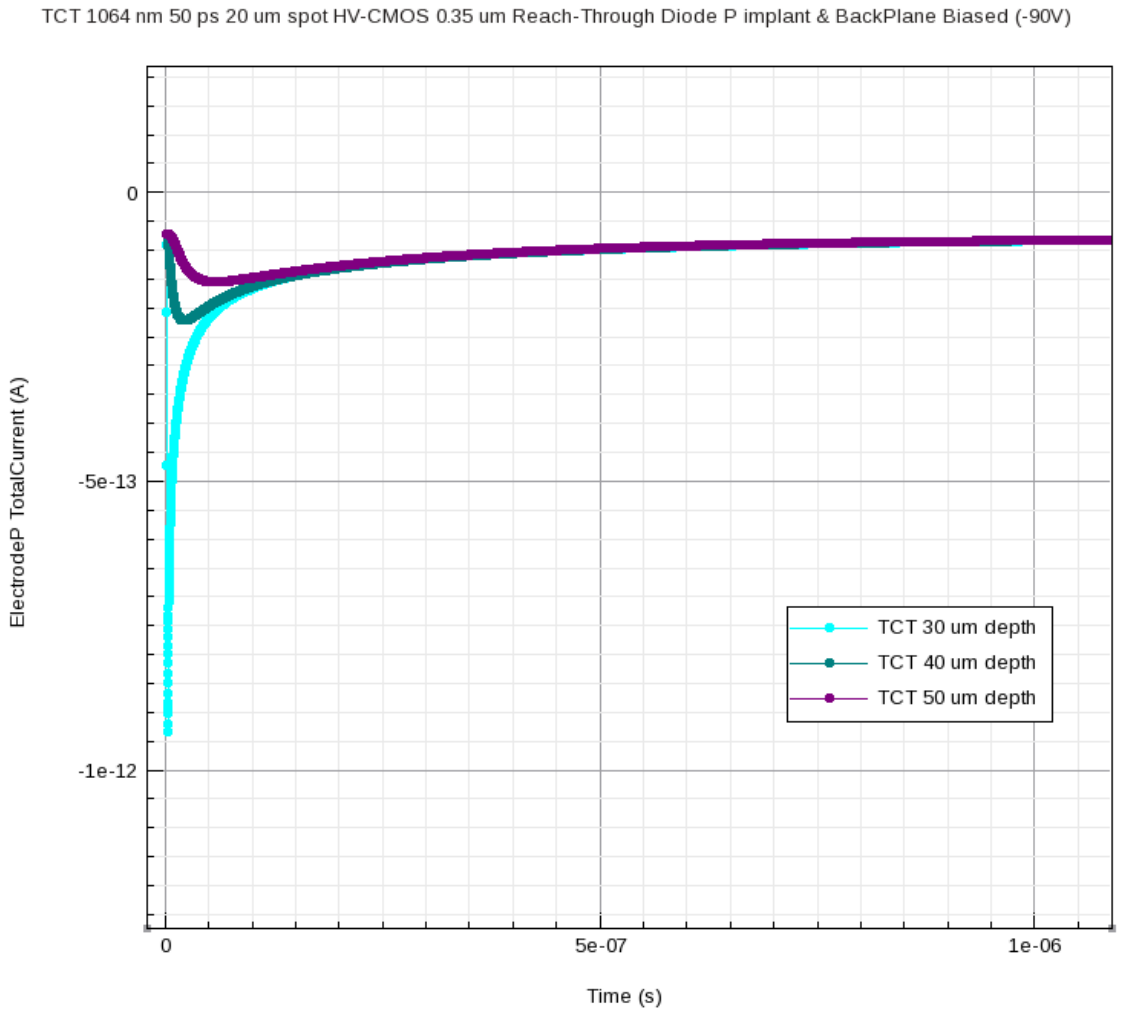
eTCT, Gaussian Doping, Backplane and p+ implant -90V, n+ GND

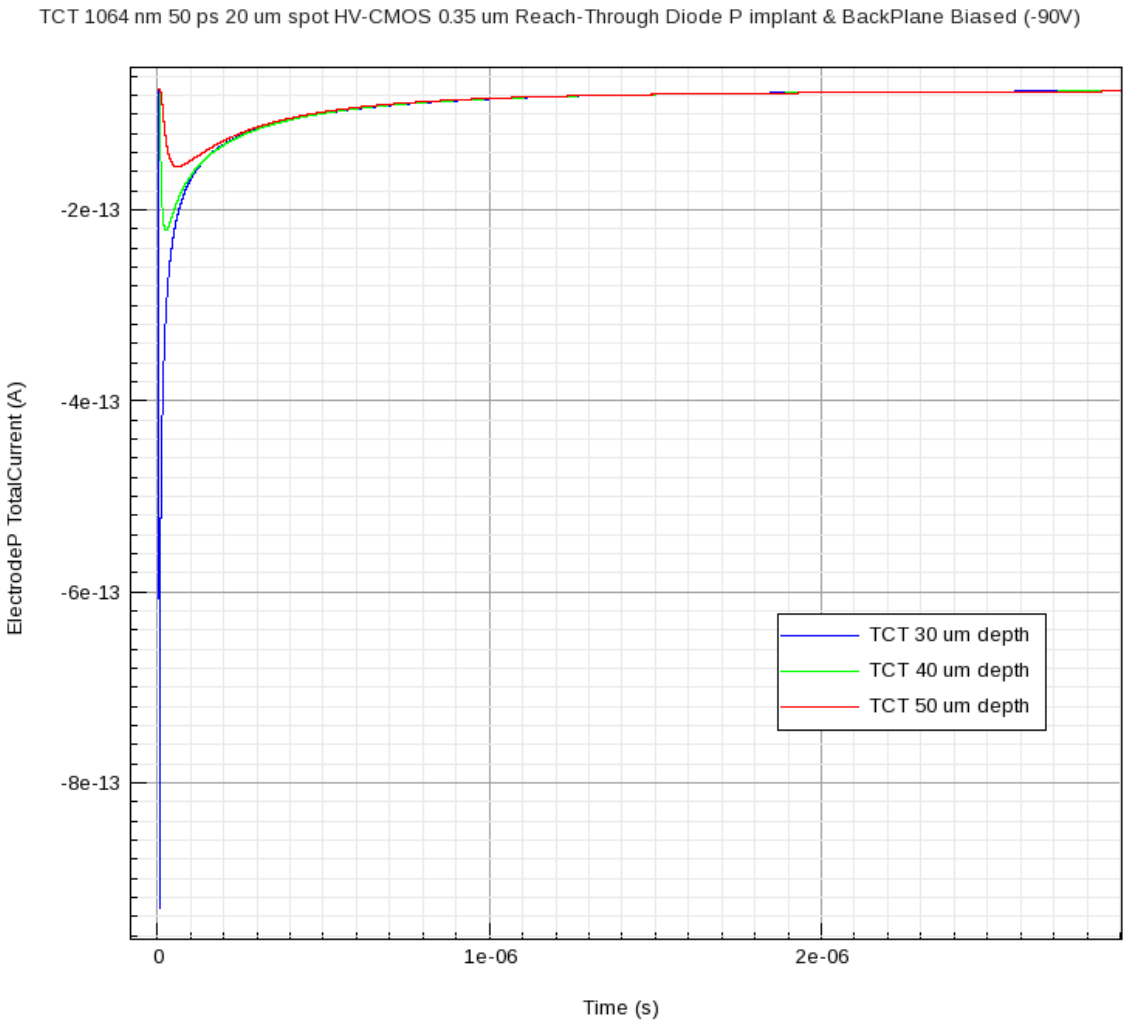




Left to right: response to the eTCT laser pulse, different depths, with a detail of short time response when laser is illuminating well in the DNTUB-p junction electric field

eTCT, Gaussian Doping, Backplane and p+ implant -90V, n+ GND

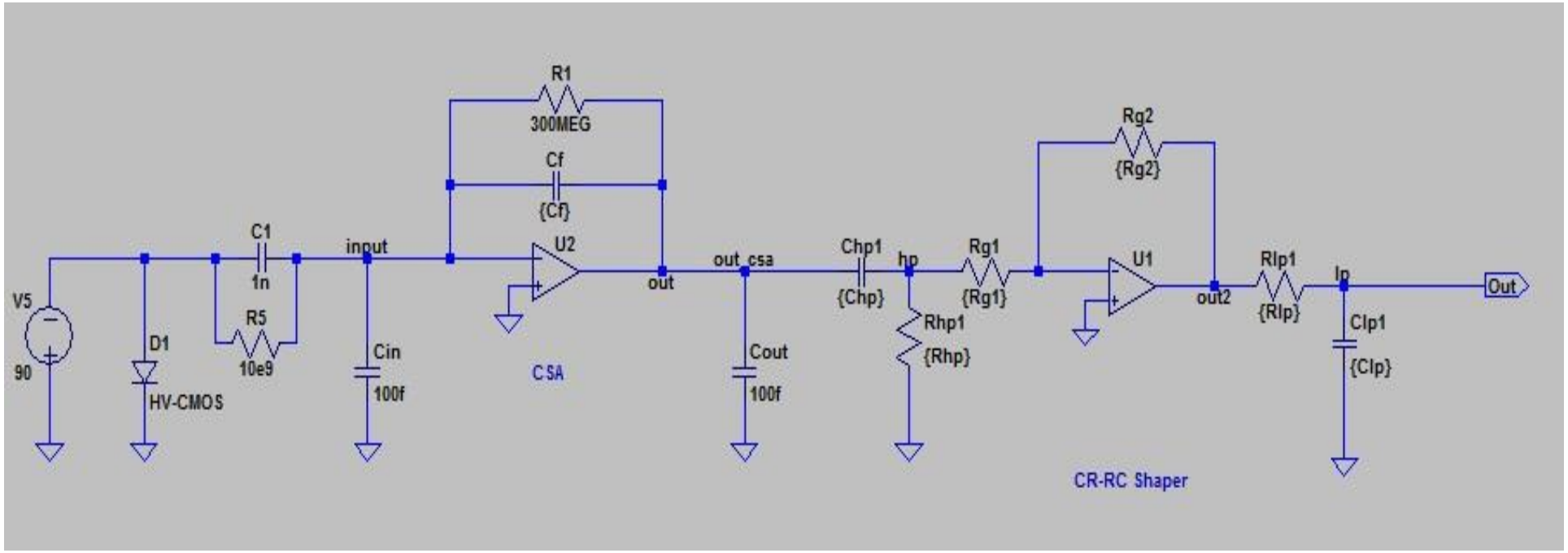




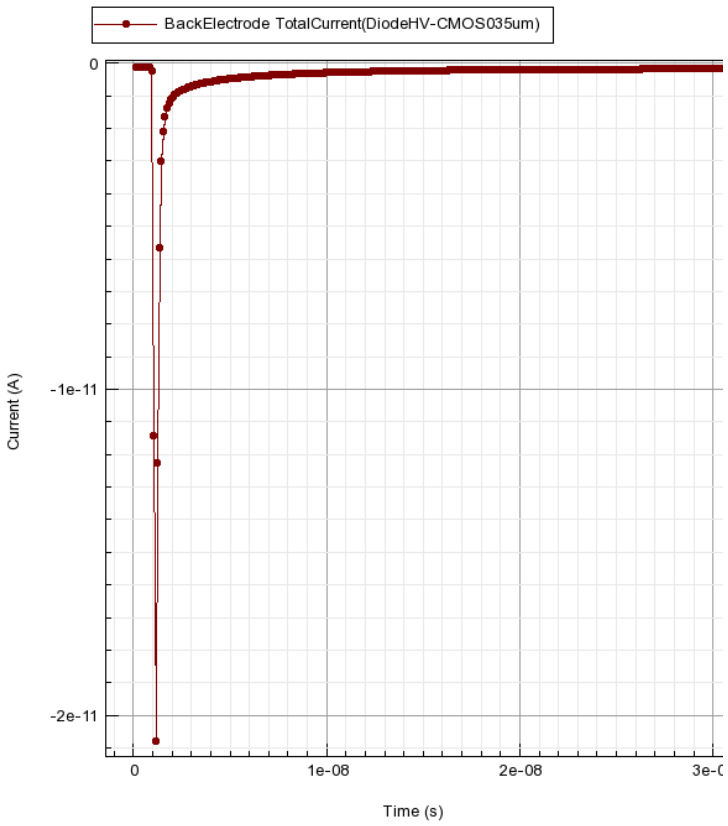
Left to right: response to the eTCT laser pulse, different depths, with a detail of long time response when laser is illuminating well off the DNTUB-p junction electric field

CSA+Shaper Front End

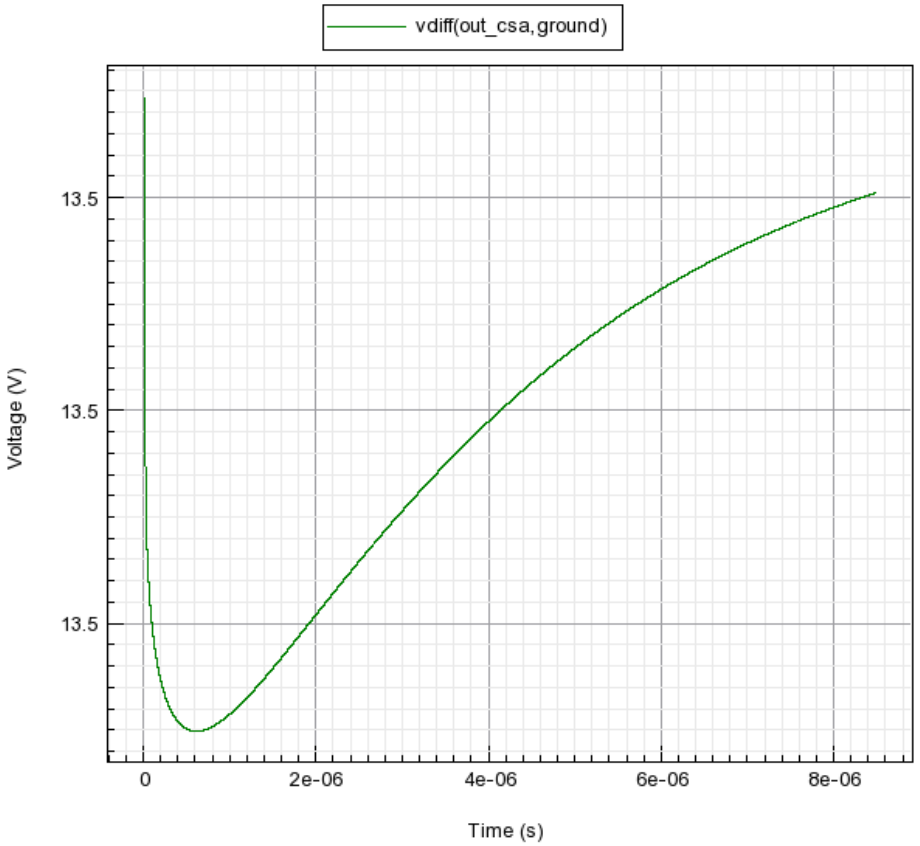
- **For experimental comparison, we simulate in TCAD a full front end connected to the HV-CMOS diode (Backplane and p+ implant -90V, n+ GND)**
- The front end simulates the bias T, Charge sensitive Amplifier and CR-RC Shaper
- The HV-CMOS, in this mixed simulation, receives a 1064 nm laser pulse hit



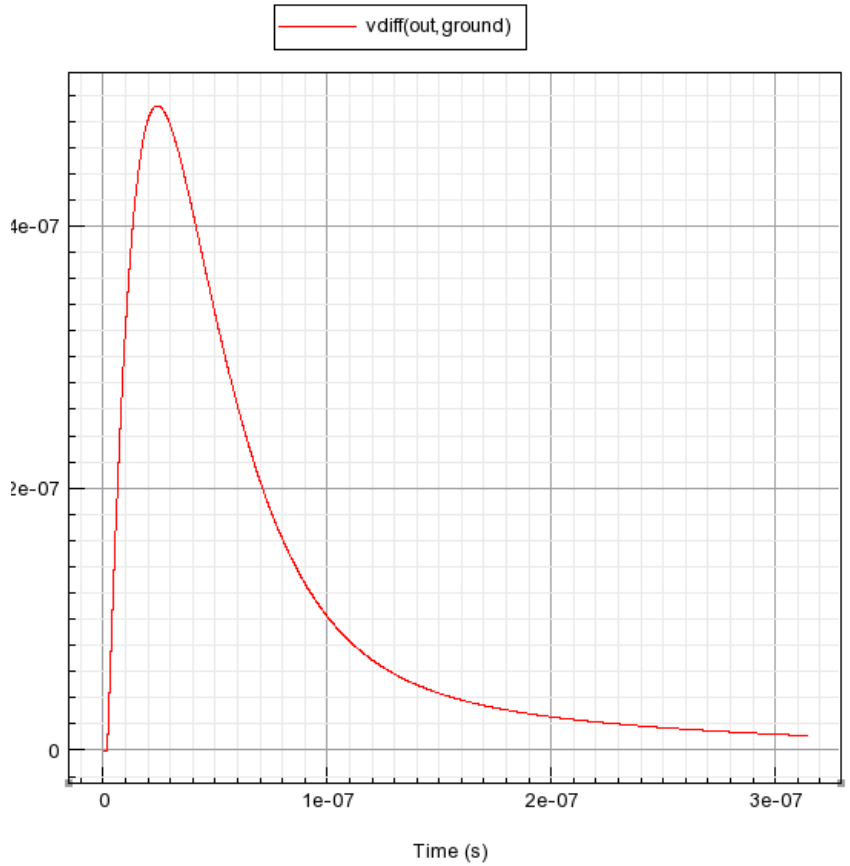
CSA + Shaper Front End Results



Detector Response
(1064 nm, 50 ps laser pulse)



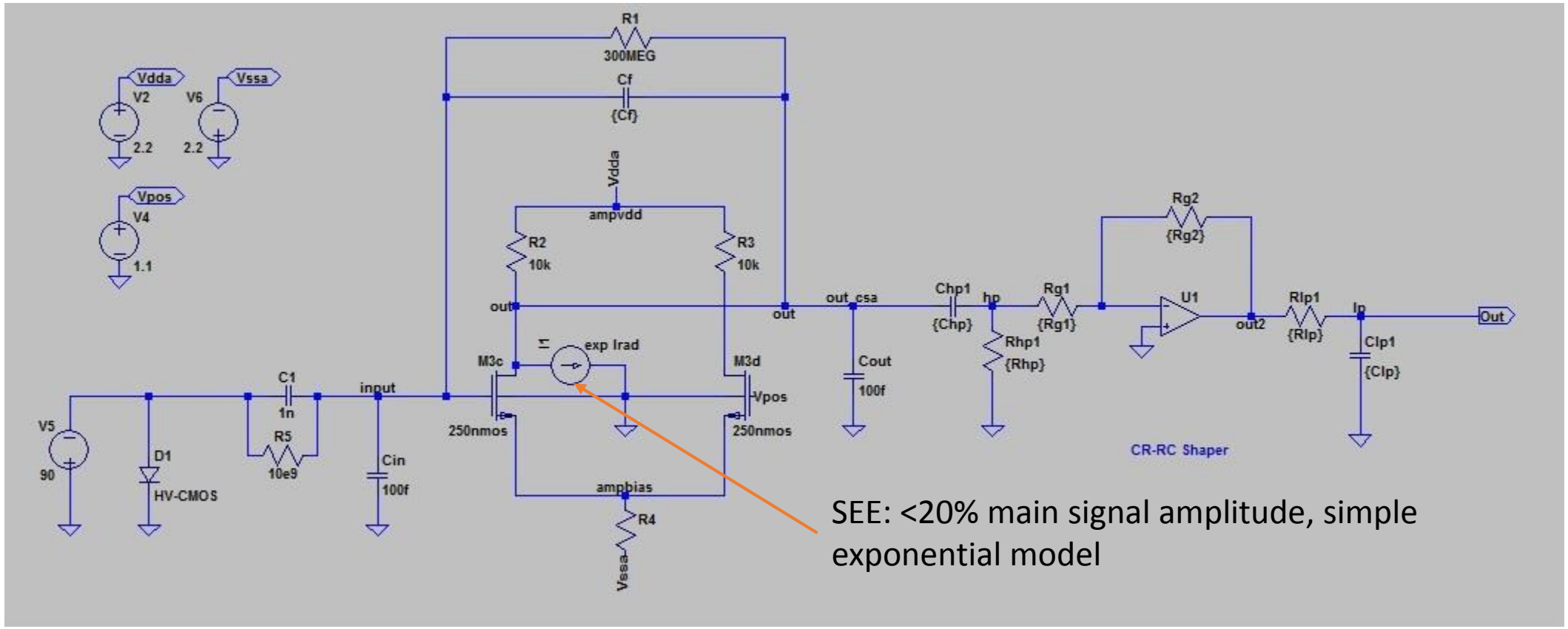
CSA Output



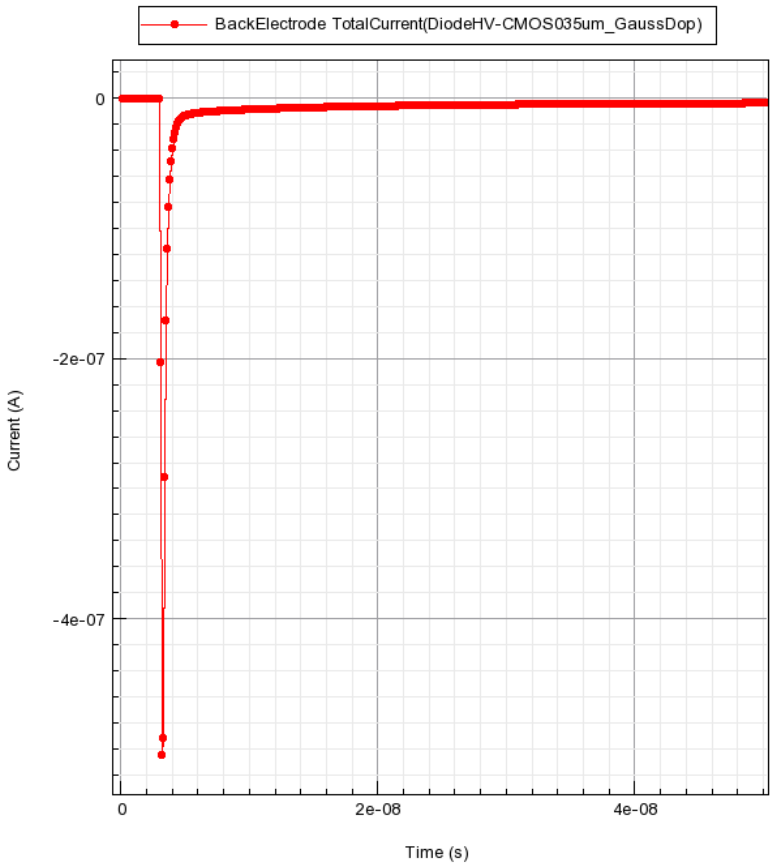
CR-RC Output

CSA + Shaper Front End + SEE

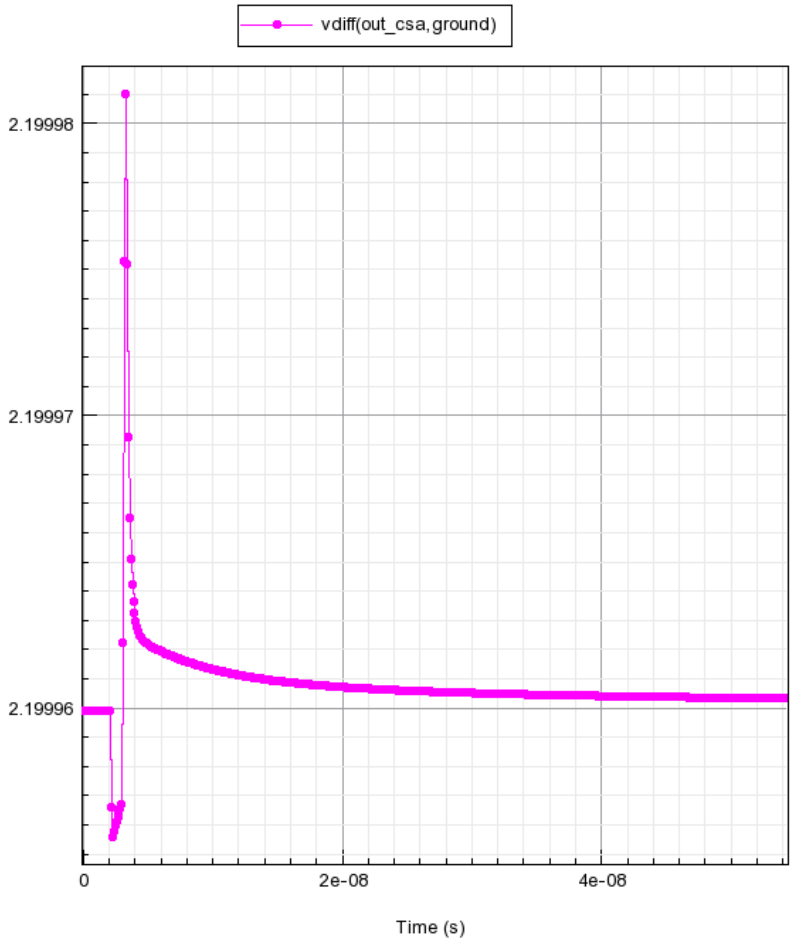
- **Any HV-CMOS is a monolithic detector so Single Event Effects could be an issue, mixed simulations could also be of help (Backplane and p+ implant -90V, n+ GND)**
- In this simulation, a MIP goes through the HV-CMOS (main signal) and also produces a SEE in one of the nmos transistors, simulated with the IBM 250 nm technology model and an impulse current source



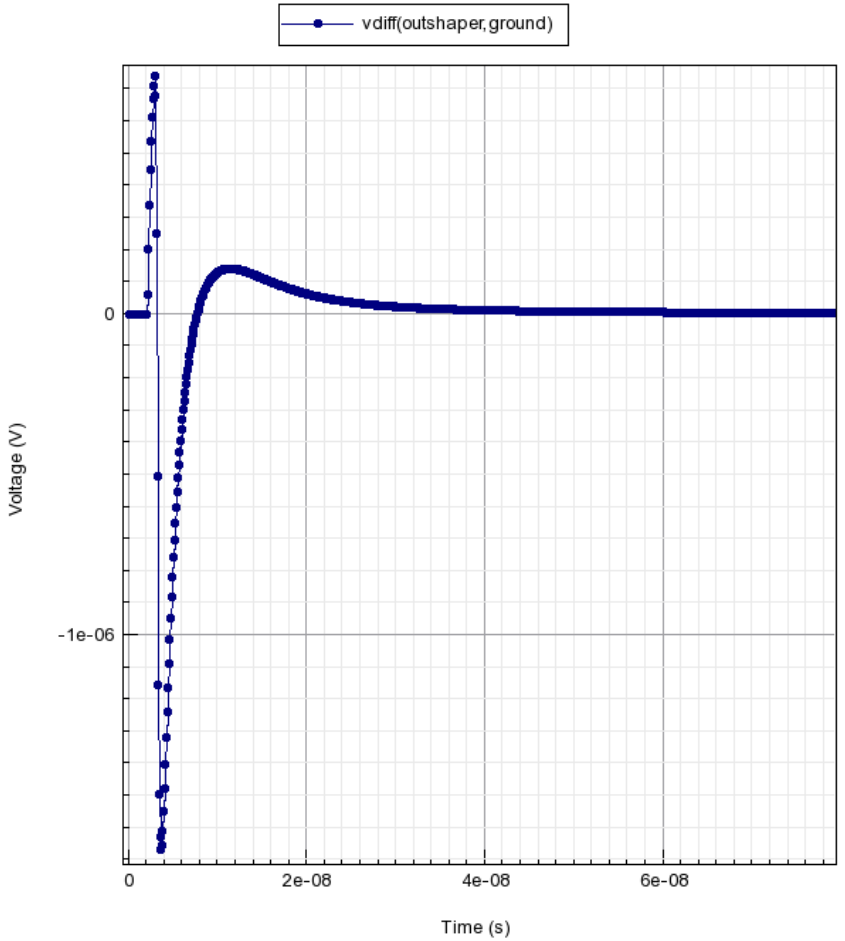
Diff amplifier +Shaper Front End+SEE Results



Detector Response (MIP)



CSA Output, a Single Event effect before the main hit is clearly visible



Shaper Output, the Single Event effect before the main hit is clearly visible

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