# *NEXT STEPS – detector group*

## *Needed info*

- ***mechanics***:
  - ✔ drawings of the flanges of the pots where the champignon has to be connected for *BOTH* the roman pots. In the document report_131108.pdf we have indicated how we intend to develop the champignon. We need the flanges design and clearly indicated what holes we should use for our cylinder. The minimum dimension for the top flange of the champignon to host the detectors is an ISO200; *the two roman pot responsibles should confirm this is ok and indicate the dimensions of the cylinder connecting the pot and the champignon flange. If an ISO200 does not fit a solution must be found together given the detector hybrid design allows a limited freedom*
  - ✔ *vacuum connection for the pump on the cylinder connecting the roman pot and the champignon top flange:* we need the model and the indication of who will procure it. We have to order also the cylinder, which means this info has to be given to the manufacturer as soon as possible to have an offer
  - ✔ ***For all the mechanical items we will place an order on the 1st of December***

- ***dose***:
  - ✔ we need the dose profile map in the regions where the detector will be placed both near the pipe and 30cm away
  - ✔ we need the dose due to protons, gammas and neutrons. This is fundamental to evaluate the SEU probability and to choose the correct kind of FPGAs
  - ✔ *we are going to perform dose tests from the beginning of december for a month. If no info is given on what to expect, we will set as a limit 20krad of gamma (that is if the components survive 20krad we will consider them fit)*

- ***DAQ***:
  - ✔ we need a written report on what signals (and what type) we need to sample from the SPS and where we would sample them. The design of the FATO board will end before Christmas.

## *Addendum on the readout electronics*

We had a fruitful meeting with the AB BI division for the DAB64 + mezzanine board for the data transfer between the tunnel and the VME crate on the surface.
Fig.1 shows a photo of the prototype of the ensemble. The tests on the board will start in the next weeks. The production of the ones needed by the experiment has already been ordered.
The tests on the final board should be done on the test bench at CERN.

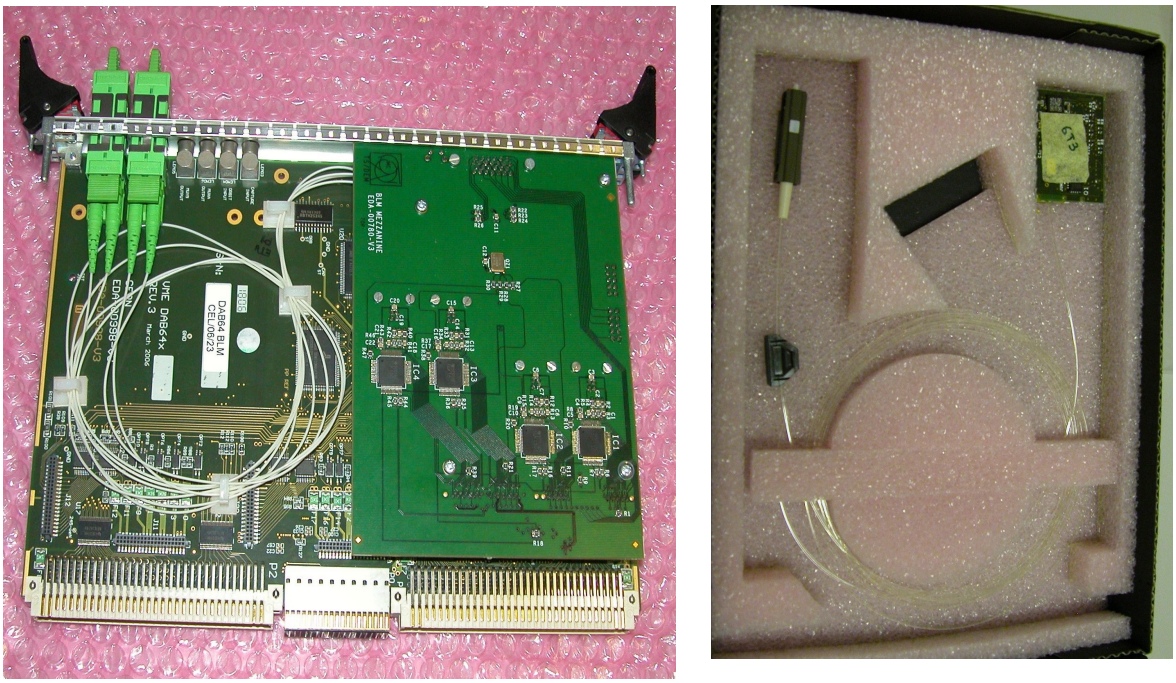

*Figure 1: DAB64 prototype + mezzanine (photo on the left) and GOH (photo on the right)*

The board is organized as follows:

- ✔ in the tunnel, the FATO board is in practice the ADC board: each ASIC will be read by an ADC with a 10MHz clock (which means each ASIC needs 12.8µs to be readout). The 3 ADC info of each view of the detector will be multiplexed by a FPGA to send the multiplexed signals to the transmission part of the board consisting of the GOH board. Each GOH board has a GOL (the ASIC controlling the transmission resisting up to 10kGy) and the diode (resisting up to 2kGy). The multiplexing is performed with a 40MHz clock (base clock of the board). The FPGA acts as a sequencer to generate the readout signals and to configure the ASICs themselves (the configuration signals are sent to the FATO through copper cables)
- ✔ on the ground, a DAB64 board equipped with a mezzanine is the real readout board. The mezzanine contains the photodiodes for the fibers. The DAB64 is the real intelligence of the board: it is equipped with a FPGA responsible of the pedestal and common mode subtraction, the zero suppression and the interface with the VME64 bus.
- ✔ At the moment the basic scheme is to equip each detector side with a FATO board and a DAB64 board for a total of 8 boards in the tunnel and 8 boards in the VME crate.

Fig.2 is a schematic representation of the readout system of one single detector.

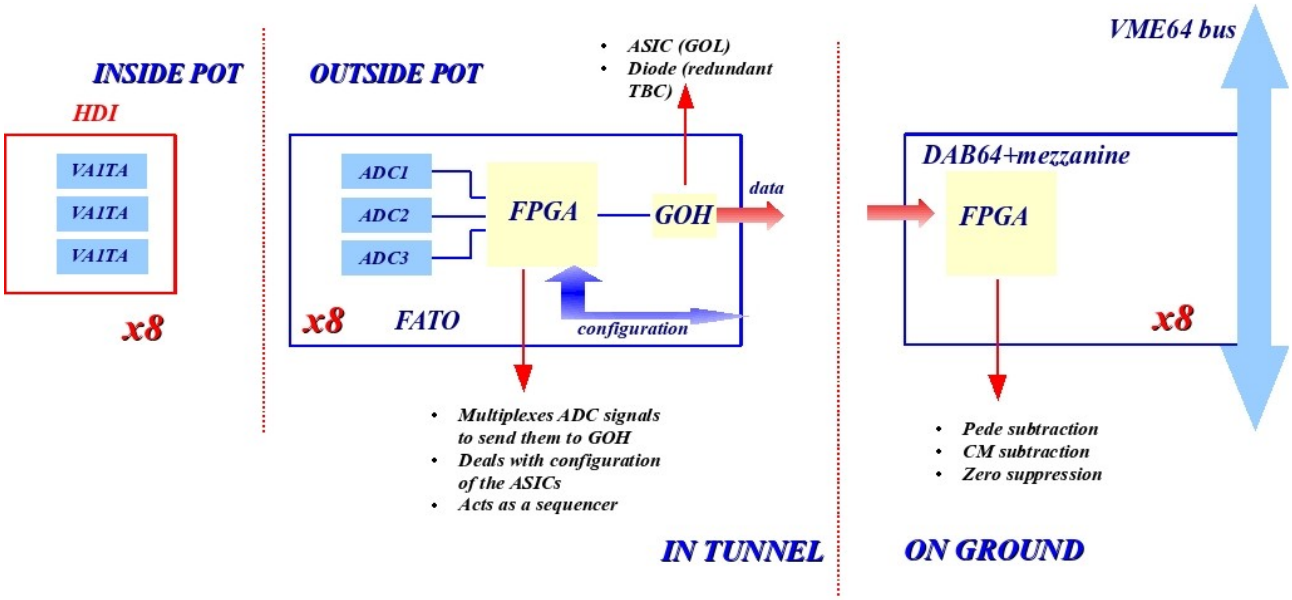


*Figure 2: Readout scheme*

As far as timing is concerned, this is the summary:

- ✔ the ASIC will be read with a 10MHz clock requiring 12.8μs to be readout
- ✔ considering the other operations for each event (hold, reset), each event will require 20μs to be readout meaning we can reach a final readout rate of 50kHz
- ✔ every channel info will consist of 64 bits: 16x3 for the ASICs (12 for the data, 1 for the Out of Range, 3 for the control) + 16 control bits (for the strip address); the time stamp is generated at the beginning of the event and sent as a first info to the DAB
- ✔ the throughput of each board is 40MHz x 16 bit for a real throughput of 640Mbit/s
- ✔ after the data reduction, we expect to have 10 strips per detector side over threshold (as confirmed by the number of the occupancy we have requested since the beginning, given we are performing a single track experiment). The info for each strip will need 24 bits (address, data and control)
- ✔ summing up all these numbers, we obtain a total throughput to the disk of: 24bit x 10 x 50000 ev/s x 8 detectors = 12 MBy/s

*This is much more complicated than whatever used on our beams up to now.*

***Final consideration:*** from when the INFN NTA Committee meets and decides the money assignments to the experiments, around 3 months are needed before the money becomes effectively available. **Given no meeting has been announced yet, we do not expect to receive money (if any) *BEFORE MARCH.*** *This will create incredible problems: no possibility to travel to CERN, no possibility to test the DAB and mezzanine boards (for which the test bench is present at CERN; preparing an alternative test bench in Italy would require at least 6 months and several tens of thousands of euros), no possibility to test with a mechanical mockup the detector in the roman pots. Just to make a few examples.*