Electronics R&D in J-PARC E16

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RD51 Mini-Week, Dec. 2015 @ CERN

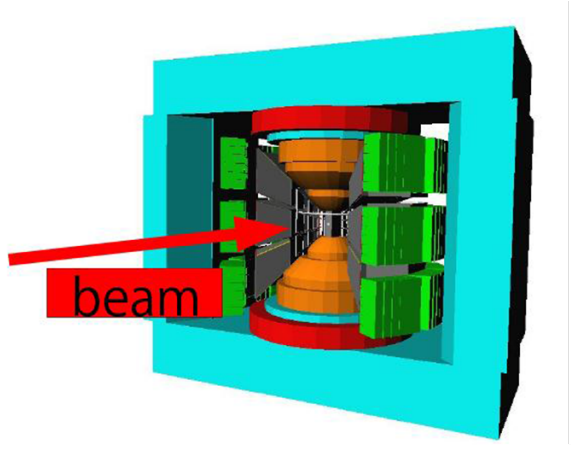
J-PARC E16 experiment

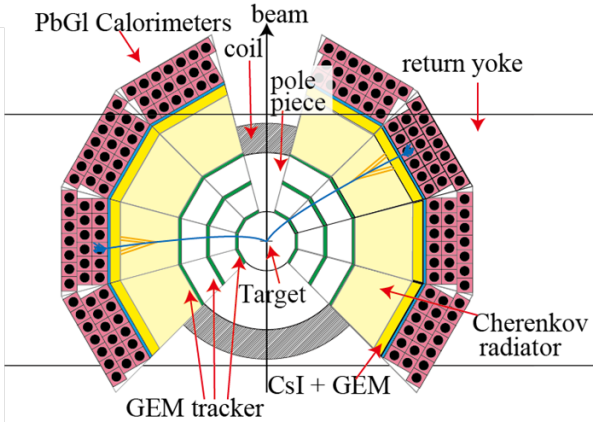
Chiral symmetry restoration in dense matter

- Mass modification of vector mesons in nuclei.
- $p + A \to \rho/\omega/\phi X$ and $\rho/\omega/\phi \to e^+e^-$

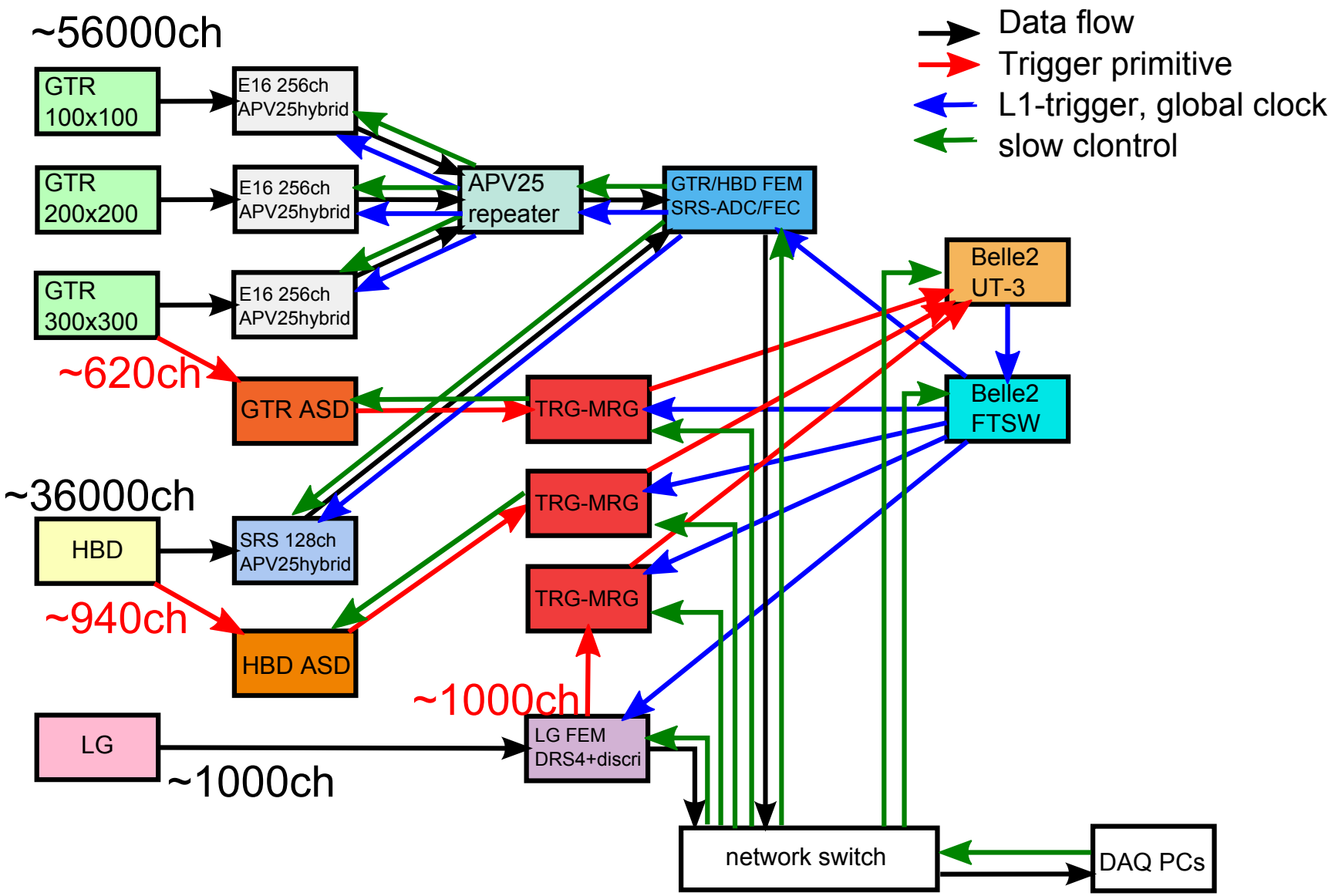
- High intensity 30 GeV proton beam 10^9–10^{10} Hz
- Large acceptance di-electron spectrometer
  - GTR (GEM tracker) ~56,000 ch
    - 100×100, 200×200, 300×300 mm^2
    - 5 kHz/mm^2, σ ~100 μm up to 30°
  - HBD (Hadron Blind Detector) ~36,000 ch
    - pure CF_4 Gas Čerenkov
  - LG (Leadglass EMCAL) ~1,000 ch

We will use SRS for readout of GTR and HBD.





J-PARC E16 elctronics overview

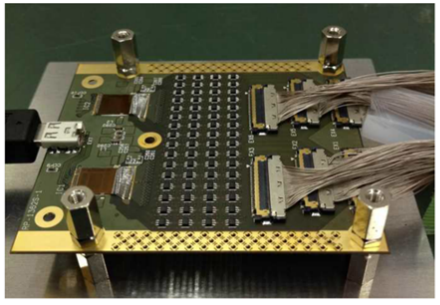


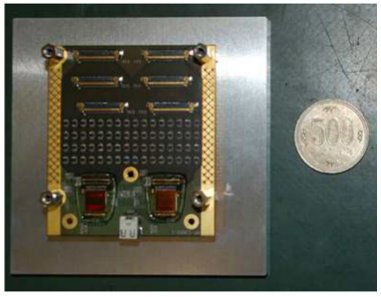
- FEM: Front End Module
- DAQ-Middlewaree developed by KEK e-sys group
- L1 trigger rate: 1–2 kHz

APV hybrid for E16 GTR

TRK-APV (U. Tokyo, RIKEN, KEK)

- A compact card with two APV25 chips
  - 8 layer FPC
- micro-miniature coaxial cable → flexibility in card installation
  - KEL-XSL cable, 48 ch ×6, ϕ =250μm, 250–500 mm length
    - http://www.kel.jp/english/product/FinePitch/xsl.html





Note

- No LDOs
- No PLL for phase tuning of clock/trigger

An external repeater module for power distribution of +1.25 V, +2.5 V and delay control is used.

Beam test @ J-PARC in 2012

K1.1BR beam line of J-PARC hadron facility

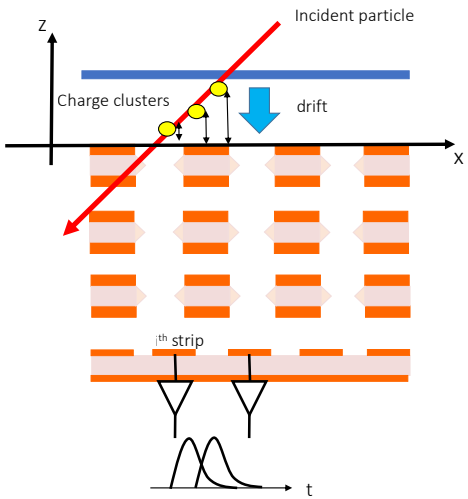
- Secondary beam ($e/\pi/K/p$)
- beam intensity : ~100 kHz in the test
- ~1 GeV/c

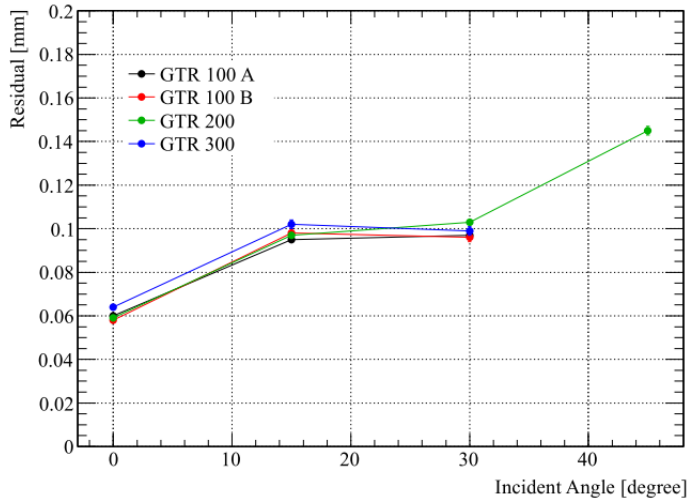
GTR under test

- size : 100×100, 200×200, 300×300 mm^2
- 3 mm drift gap
- Ar : CO_2 = 70 : 30
- slow drift velocity for timing method
- with TRK-APV and SRS ADC-FEC-V3 combo

Position resolution

Timing information





We achieved good position resolution for inclined tracks due to the timing method.

Beam test @ ELPH in 2015

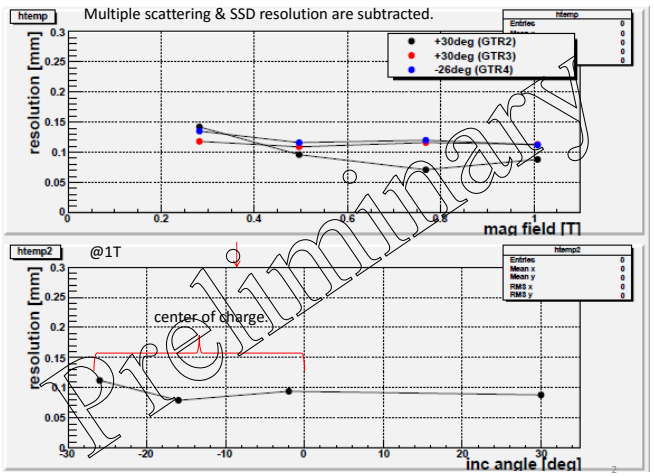
Research Center for ELectron PHoton Science, Tohoku U., Japan

- electron synchrotron facility @ Tohoku Univ., Japan
- e^-/e^+ beam line for a detector test

Position resolution in a magnetic field

- 100×100 mm^2 GEM
- magnetic field : 0.3 – 1 T
  - Lorentz angle $\sim 14°$ @ 1T (Magboltz)
- incident angle : $0°$ – $30°$
- $\sigma_x \sim 100$ μm (preliminary)

Analysis is in progress.



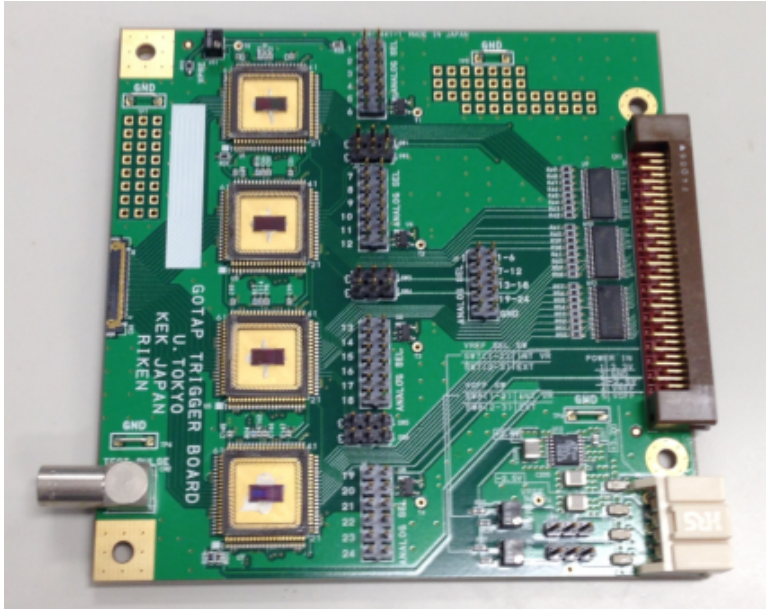
Foil trigger ASD (Amplifier-Shaper-Discriminator)

For an easy trigger application using a signal from a segmented cathode foil.

Specification

MXIC (Macronix International) 0.5 μm process

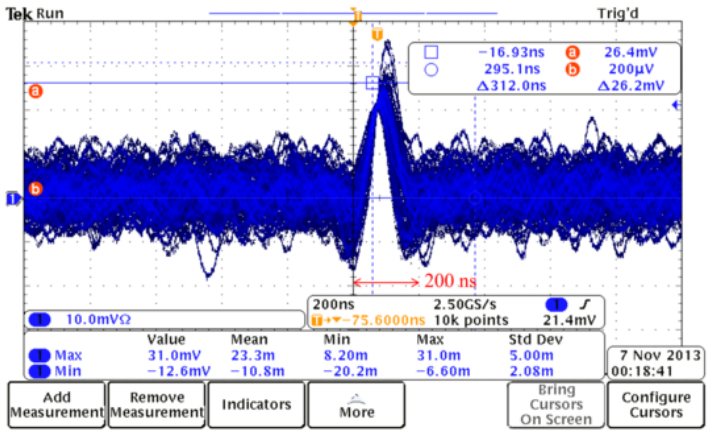
parameter	value
# of ch	6 ch/chip
Input range	10 fC – 1 pC (both pol.)
Shaper time constant	25 nsec
Pulse width	< 200 nsec
Conversion gain	3.2 mV/fC
Output	analog 6 ch
	comparator out 6 ch
ENC	20,000 (@ C_{det}= 2 nF)
Power	+2.5 V/0.1 A, -2.5 V/0.1 A



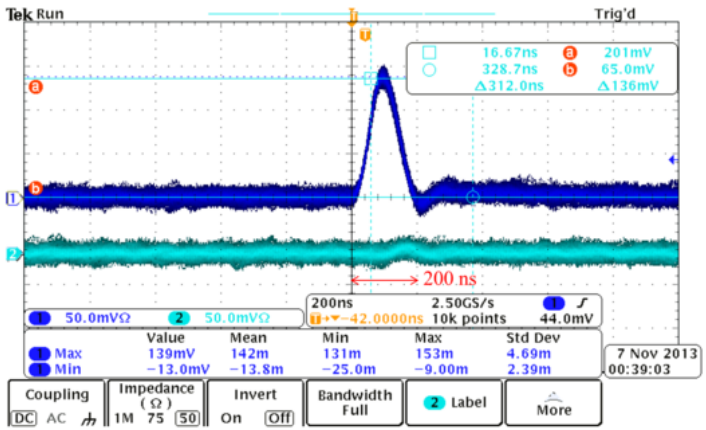
24 ch GTR-ASD card (prototype)

Foil trigger ASD (2)

Response to test pulse input

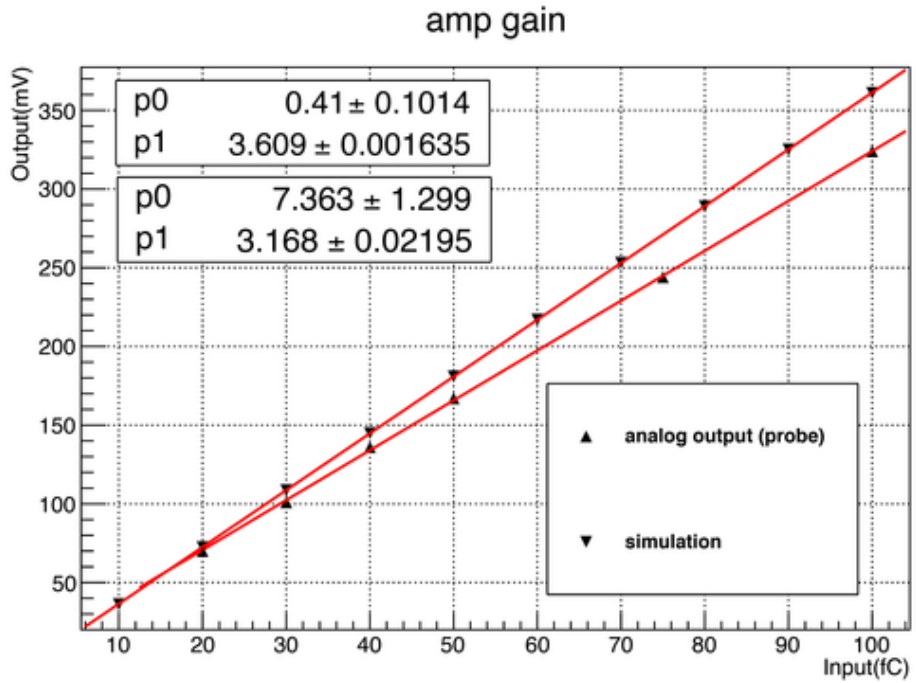


10 fC input



100 fC input

Conversion gain



Test with a GEM chamber is ongoing.

TRG-MRG (Trigger Merger)

Composed of a carrier card, 2 LVDS receiver mezzanine cards and 2 slow control sub cards.

Carrier card

- +12V, PCIe 6 pin
- Xilinx XC7K160T-2FFG676C
- 2 HPC FMC
- up to 256 ch TDC (LSB < 4 nsec)
- 8×10 Gbps optical links
- RJ45 for trigger and clock I/F
- 2 NIM in, 2 NIM out

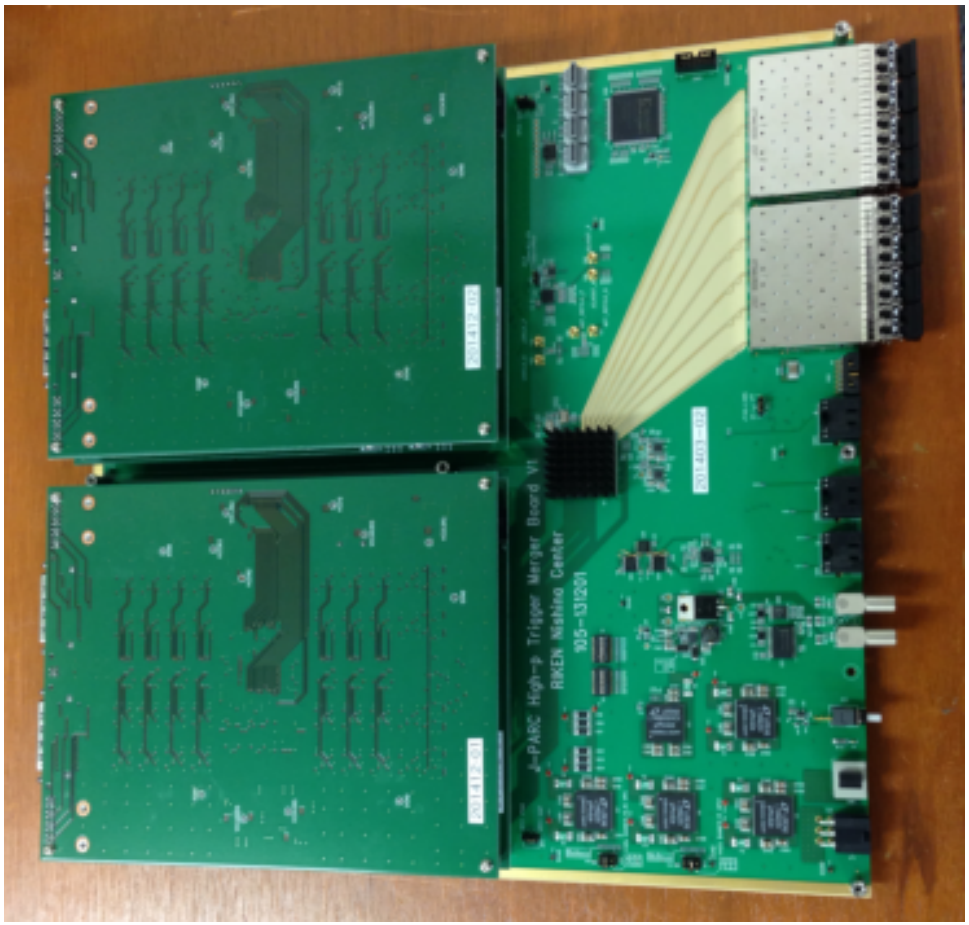
LVDS receiver mezzanine card

- 128 ch LVDS receivers per mezzanine with 4 VHDCI connectors

ASD slow control sub card

- Manages 4 GTR-ASD card

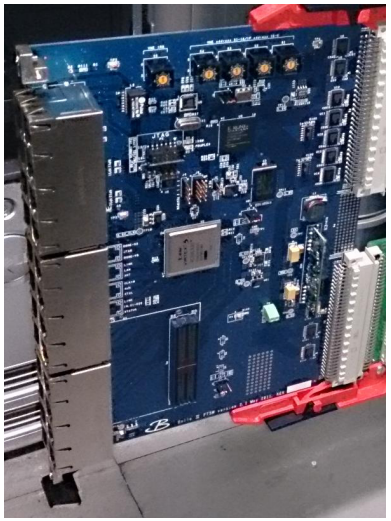
- Firmware development is ongoing.
- TRG-MRG test with an actual board.



Future works

Readout by SRS-ATCA

- We will use SRS-ATCA in the physics run.
- Two SRA-ATCA blades with mezzanines have been delivered in the summer for the test bench.
- Firmware development is necessary.
  - APV with zero suppress
  - Trigger I/F with our trigger/clock distributor module (Belle-II FTSW).
  - Communication with a custom-made protocol (not DTC protocol)
  - We would like to use the HDL source and schematics of SRS to develop the firmware by ourselves.



Belle-II FTSW

HBD trigger circuit

- ASD for cahode foil signal (~1,000 ch)?
- New hybrid cards with trigger output or self trigger for pad signal (~36,000 ch)?
  - Beetle, VMM, GEMROC, etc.

Summary and Future works

Summary

- J-PARC E16 will use SRS for readout of GEM detectors, GTR and HBD.
- TRK-APV hybrid card has been developed for GTR.
  - 256 ch/card, KEL-XSL micro-miniature coaxial cable
- Position resolution with timing method
  - σ ~100 μm for 30°
  - σ ~100 μm in a magnetic field (preliminary)
- We developed a foil trigger ASD chip for the trigger application.

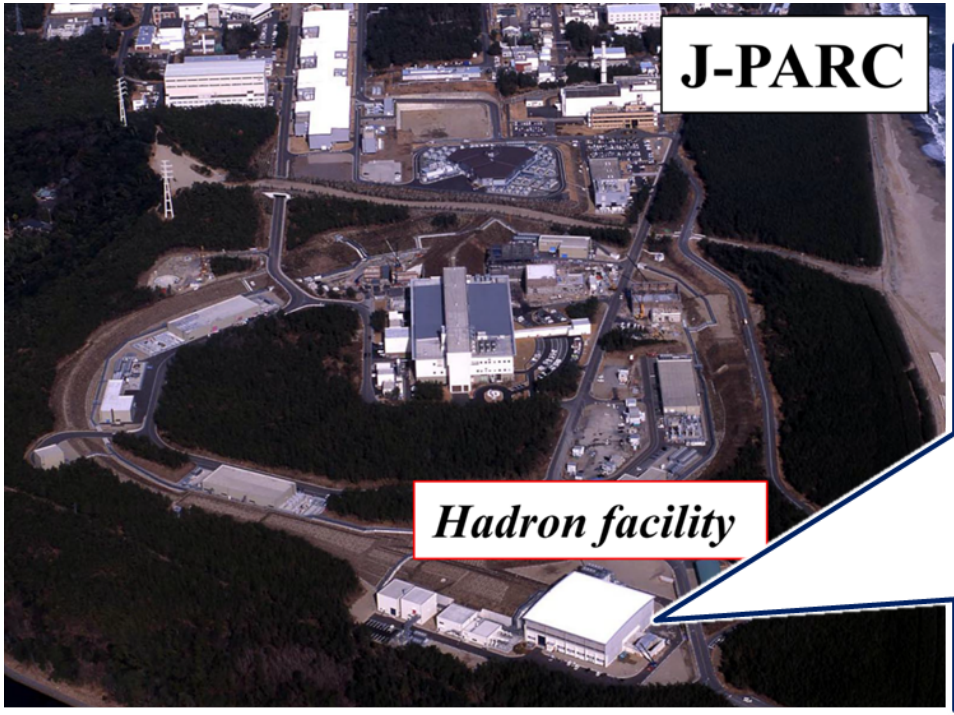
To do

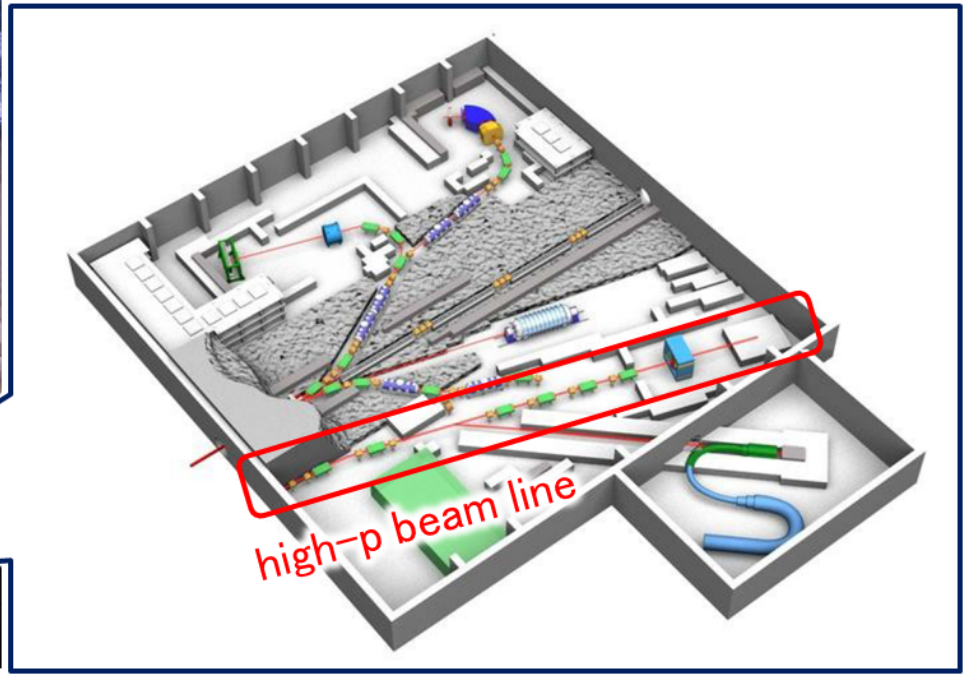
- SRS-ATCA firmware for the physics run
  - I/F with Belle-II FTSW, APV with zero-suppress
- HBD trigger FEE

BACKUP

J-PARC hadron facility and high momentum beam line

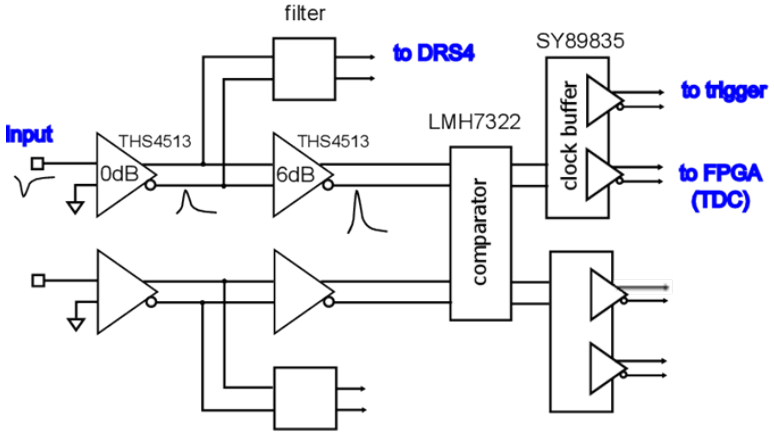
- $\sim 10^{10}$ protons per cycle (a fraction of primary beam)
  - 2 sec. beam-ON per 6 sec. $=$ slow extraction mode
- Construction is ongoing. Physics run starts in 2017.

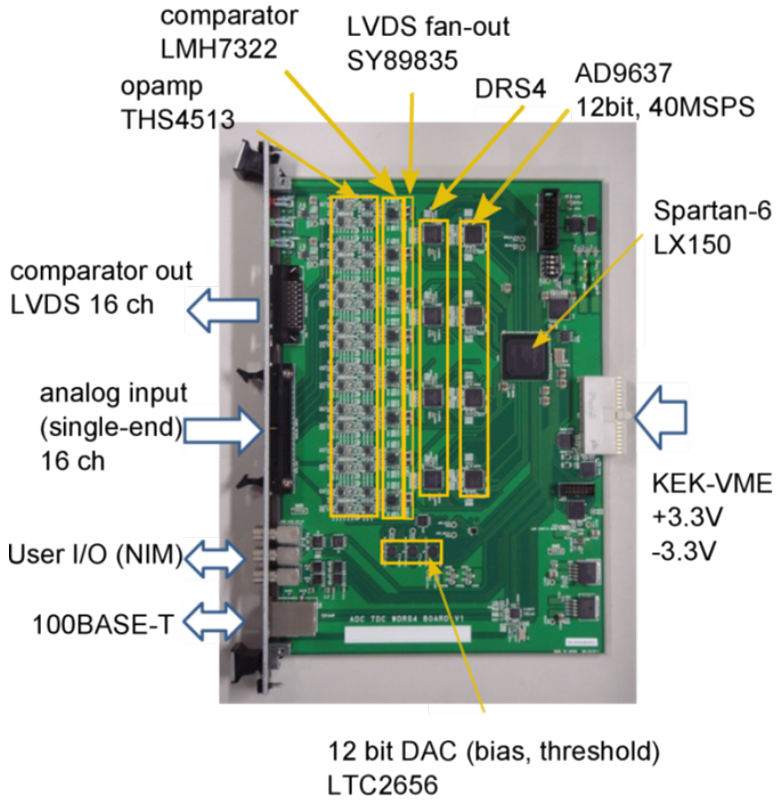




LG readout (prototype)

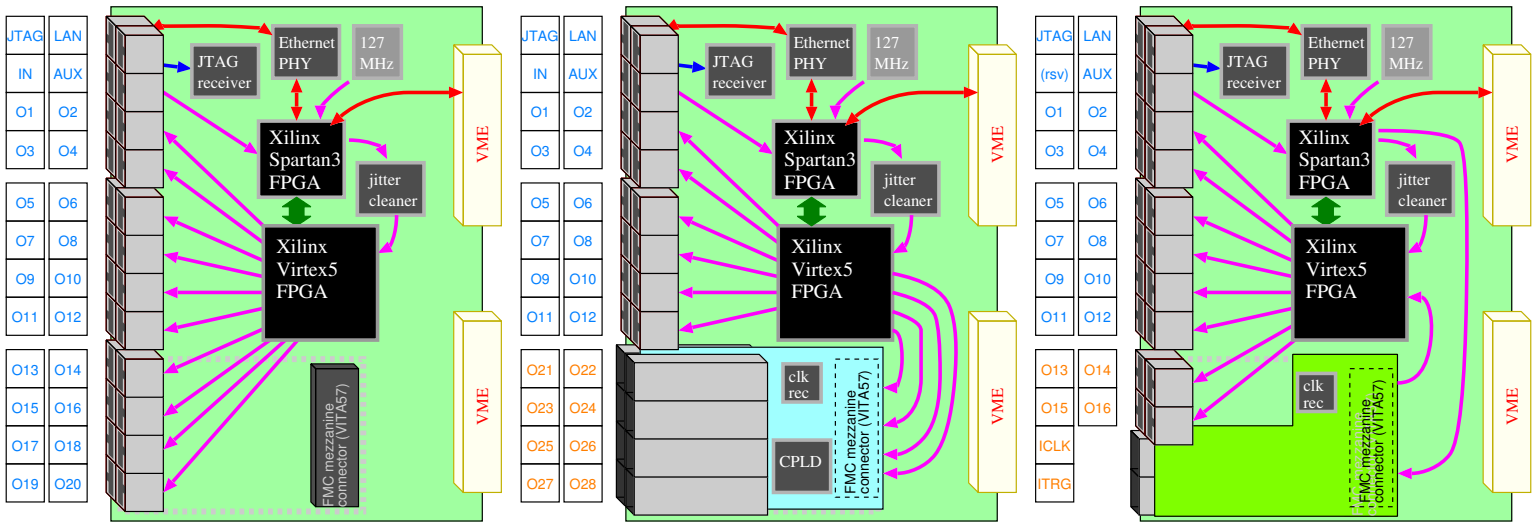
- KEK-VME 6U board (power and trigger tag from J0 bus)
- 16 ch analog inputs
- Waveform sampling at 1 GHz by DRS4 ASIC (max. 2 μsec buffer)
- Fast comparator output for trigger and TDC
- data readout and slow control by SiTCP (100 Mbps)
- FPGA-based high resolution TDC (goal: < 30 psec)





Belle-II FTSW (Fast Timing SWitch)

- Universal logic board for clock/trigger or JTAG deistribution over LVDS
- Developed by KEK Belle-II gruop
- Commecial RJ45 LAN cable for 254 Mbps data connection (Belle2Link)



Reference

- M. Nakao, JINST7, C01028, 2012.
- M. Nakao *et al.*, IEEE TNS 60, 3729, 2013.

Belle-II UT3 (Universal Trigger board 3γ)

- Developed by KEK Belle-II group

Main board

- FPGA: Virtex-6 HXT FF1923 package
- clock : 1 in, 1 out
- NIM : 2 in, 2 out
- 24 GTH (11 Gbps $\times$24)
- LVDS : 64(32$\times$2) in/out

GTX daughter board (optional)

- 40 GTX (6.25 Gbps $\times$40)

General IO board (optional)

- clock : 2 out
- NIM : 8 in, 8 out
- LVDS : 64(32$\times$2) in/out
- RJ45 for Belle2Link : 4