

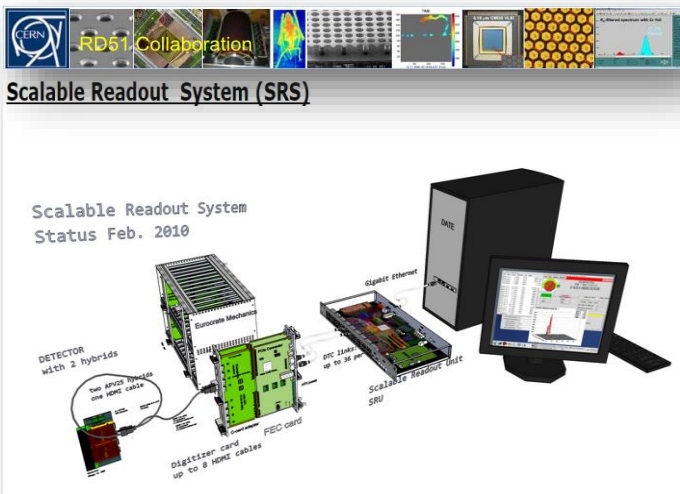
WP13

Innovative gas detectors

RD51 Mini Week, December 2015

Report on WP13 Sub Task 13.3.1 and 13.3.2
“Tools to facilitate detector development”

1. Interfacing FE-chips specific to gas detectors to the Scalable Read-out System (SRS)
2. Development of cheap, standard MPGD dedicated laboratory instruments



Support from **AIDA2020**

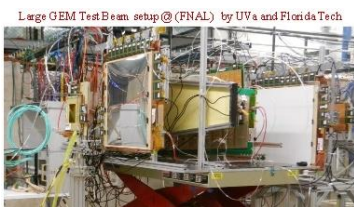
- Easy-to-use
- Portable
- Scalability from small to large system
- Common interface for replacing the chip frontend
- Integration of proven and commercial solutions
- Availability of robust Data Acquisition software package

- High impact in the community:
 - More than 2000 APV25 chips in use with SRS in the mpgd /rd51 community
 - SRS Components for R&D on detectors with APV25 FE chip available on the CERN store

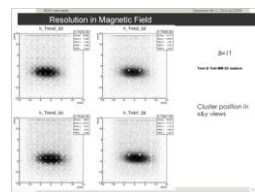


Common interface for replacing the chip frontend: Status (few examples)

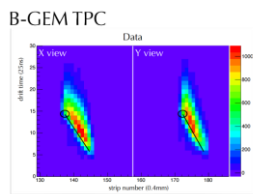
SRS & APV25 – Large MPGD/RD51 community



Uva & Florida Tech



ATLAS NSW mm test beam



ESS and CERN GDD



New FE ASIC with:

- Charge & time information
- Self triggering
- High readout rate

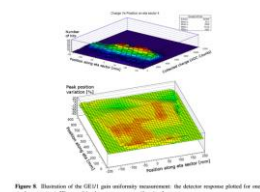


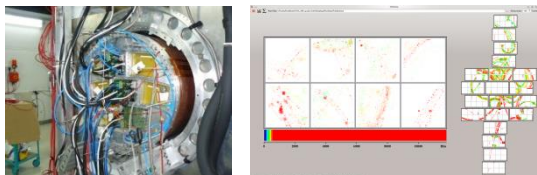
Figure 8. Illustration of the GEM1 gain uniformity measurement: the detector response plotted for one single active strip. 2D map of the detector response uniformity (bottom).

CMS-GEM

Selected Candidates:

- VMM (ATLAS NSW-BNL)
- GEMROC (AGH)

SRS & Timepix (LC-TPC) – Bonn/Desy



Interfacing TimePix3

SRS & SiPM (NEXT TPC)



Support from

AIDA2020

WP13 Task 13.3.1:
Interfacing FE-chips specific to gas detectors to the Scalable Read-out System (SRS)

	Task 13.3.1	AIDA 2020 <u>Key</u> /Partner Institutes
Milestone [M36]	VMM (ATLAS NSW, ESS, RD51)	<u>CERN</u> : H. Muller, E. Oliveri
Milestone [M36]	GEMROC	<u>AGH Krakow</u> : B. Mindur, eicSys: T. Jezynski <u>CERN</u> : E. Oliveri, H. Muller
Milestone [M36]	Timepix3 (LC-TPC)	<u>University of Bonn</u> : K. Desch, J. Kaminski

VMM

The ATLAS New Small Wheel(s) Upgrade (2019-20) 3

The ATLAS upgrade is motivated primarily by the pile-up rate expected at high luminosity which will lead to an increased trigger rate. There is a need of replacing the innermost muon station with an efficient trigger and precision system to eliminate fake triggers without loss on physics acceptance.

Existing Small Wheel (MDT, CSC, TGC) \rightarrow **NSW**

New Small Wheels (16 sensitive layers)

- sTGC (8x) (small strip Thin Gap Chambers)
- Resistive strip Micromegas (8x) (Micromesh Gaseous Structure)

Front-end Electronics Requirements (need of custom ASIC)

- Another challenge for this Project - More than 2.3 million channels total (2M for Micromegas and 300k for sTGC)
- Operate with both charge polarities
- Sensing element capacitance 10-200pF (sTGC Pad up to 2nF)
- Charge measurements up to 2pC @ < 1% RMS (6pC for sTGC pads)
- Time measurements ~ 100ns @ < 1ns RMS
- Trigger primitives, complex logic
- Low power, programmable
- Space requirements on the detector

Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System: [Link](#)

George Iakovidis - MPGD 2015 15/10/2015

VMM1 - Testing with Micromegas Detectors 7

- First prototypes (x16) tested in 2012 test beam successfully¹ with custom readout
- First time testing the Resistive Micromegas as trigger system.
- Low noise (~0.2FC) and good timing gives an excellent position resolution (close to 100 μ m demonstrated performance²) and accurate timing for the μ TPC studies.

Position Resolution for perpendicular tracks
Res: 65.98 μ m

Position Resolution for inclined tracks

Track segment resolution at the trigger level

¹T. Alexopoulos et al. - Performance of the First Version of VMM Front-End ASIC with Resistive Micromegas Detectors, ATLAS-UPGRADE-PUB-2014-001, [arXiv:1403.3330](#)

²G. Iakovidis - The Micromegas project for the ATLAS upgrade, JINST, C12087(03), [arXiv:1208.4001](#)

- Charge & time information
- Self triggering
- High readout rate

VMM1 Architecture and Specifications (analog) 5

64 channels

CA, shaper, peak, time, logic, ART (ToT, TlP), amplitude, timing, address, reset

pulsers, bias, DAC, temp

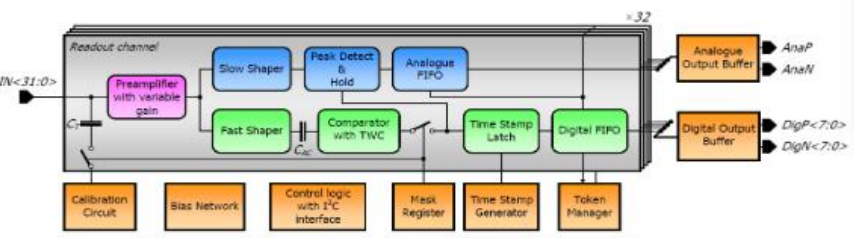
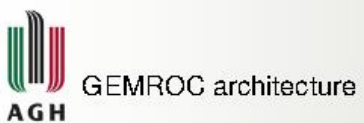
TAC stop, TAC stop (opt), analog thr, neigh. enable, peak detector, time detector (TAC), flag, fflag (ART flag), fa0.5 (ART addr.)

- **Charge amplifier:** input MOSFET: 10mm, 1.65mA, 18pF with adjustable positive or negative polarity, input capacitance: optimised for 200pF, can operate in a range from sub-pF to 400pF gain: adjustable 0.5, 1, 3, 9 mV/fC (maximum charge 2, 1, 0.33, 0.11 pC)
- **Shaper:** 3rd order with complex conjugate poles in Delayed Dissipative Feedback (DDF), adjustable peaking time: 25, 50, 100, 200ns
- **Discriminator:** adjustable with 10-bit global DAC, adjustable threshold, channel discrimination adjustment up to 15mV (1mV step), capable of processing sub-hysteresis signals with effective discrimination of ~2mV. This provides neighbour logic for channels but also chip interconnection
- **Peak detector:** measurement of the peak amplitude (sub-mV resolution on amplitude measurement)
- **Time detector:** sub-ns resolution measurement of peak time, low time-walk on peak time measurement with adjustable time-to-amplitude converter (TAC): 125, 250, 500, 1000 ns.
- **Logic:** direct time-over-threshold or time-to-peak output and Address in Real Time (trigger primitives)
- **Output:** 2 phase readout, PDO and TDO as analog and digital address of the channel
- **Monitor Output:** Analog pulse, pulsers DAQ, threshold (channel, global), temperature, reference voltage.
- **PROMPT** (courtesy of CERN): [export regulations \(ITAR\) compliance circuit](#)

ATLAS NSW-BNL, G. Iakovidis et al.

<https://agenda.infn.it/getFile.py/access?contribId=55&sessionId=2&resId=0&materialId=slides&confId=8839>

GEMROC

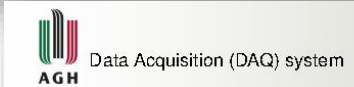


- 32 channels in one ASIC, each channel is split into: slow (energy) and fast (timing) sub-channel.
- Switchable gain (2.5 mV/fC for low gain, 5 mV/fC for high gain for slow channel) and signal polarity selection, input charge 0-500 fC.
- Derandomization of data and zero suppression in the token-based readout.
- Self triggering mode - readout initiated by the input signals.
- Noise defined as the ENC below 0.5 fC for timing and 0.43 fC for energy sub-channel.
- Minimum discrimination threshold 2.5 fC input equivalent.

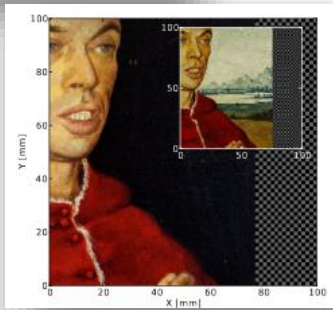
Fiutowski T. *IEEE Nuclear Science Symposium Conference Record*, pages 1540–1544, 2011.

Barozz (Mindur) (AGH) An application of GEM detectors for XRF imaging 7 / 21

- Entire acquisition time of about 5.5 h.
- Intensity 0.45 kcps.

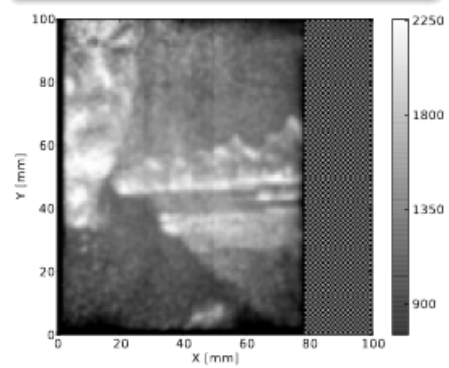


- Parameters of the system
- Four ASIC boards each one comprising 2 GEMROCs.
 - Custom ADC board hosting Virtex 5 FXT70 FPGA Mini Module Plus.
 - ▶ Capable to read out 4 ASIC with full speed.
 - ▶ Master/slave board connection for simultaneous X and Y coordinates readout.
 - ▶ Generates clock, reset and test pulse signals for ASICs.
 - ▶ Provides the PC slow control.
 - ▶ Output throughput up to 1 Gb/s using standard Ethernet link.
 - Two modules in order to read X and Y planes.
 - High count rate capability up to 5×10^6 cps.

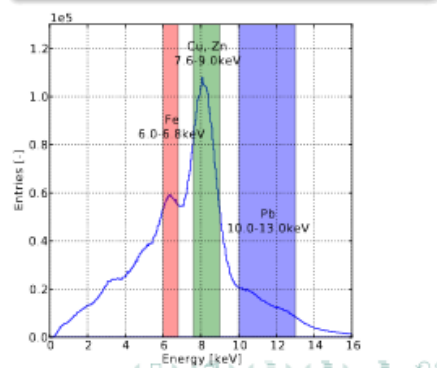


- Charge & time information
- Self triggering
- High readout rate

Total intensity map for XRF



Cumulative energy spectrum

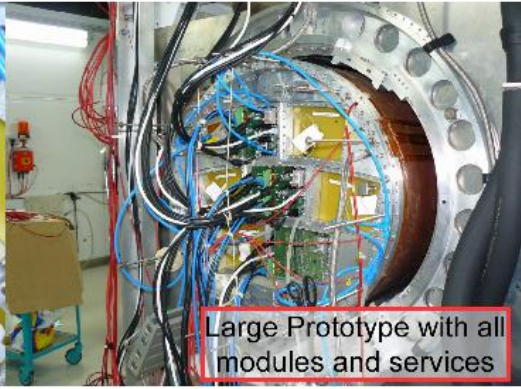
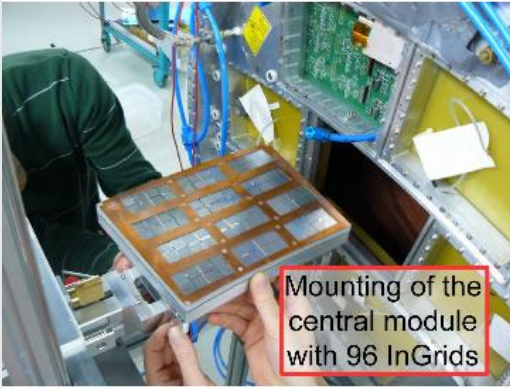


GEMROC –AGH Krakow, B. Mindur et al.

<http://indico.vecc.gov.in/indico/getFile.py/access?contribId=26&sessionId=8&resId=0&materialId=0&confId=31>

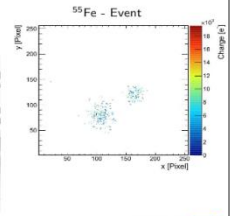
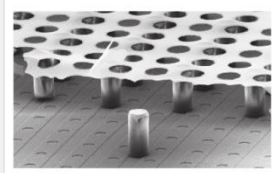
Test beam setup

Feasibility demonstration of the Pixel-TPC: March/April 2015



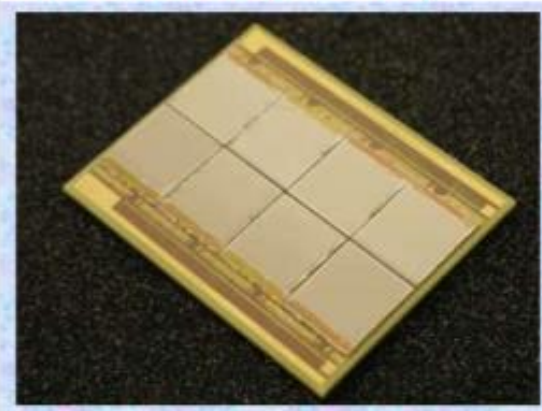
Timepix+Micromegas=InGrid

- Aluminium grid on chip
- Photolithographic process
 - Align holes to pixel
 - Uniform pillar height



Michael Lupberger TWEPP2015 universitätbonn

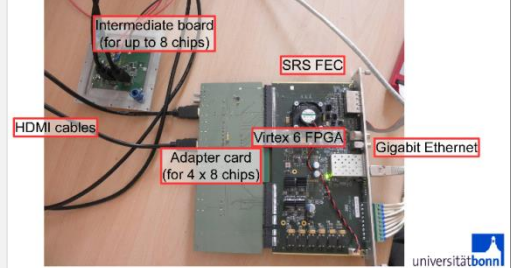
Octopuce Board (8 "Ingrid" Detectors Readout Matrix (~ 3*6 cm²))



→ TimePix3

Implementation of the ASIC

Readout chain:
Chip carrier/Intermediate board ↔ adapter board/FEC ↔ (Switch) ↔ PC/DAQ



Michael Lupberger TWEPP2015 universitätbonn

Ingrid [TimePix+mM] (LC-TPC) – Bonn/Desy - K. Desch, J. Kaminski, M. Lupberger

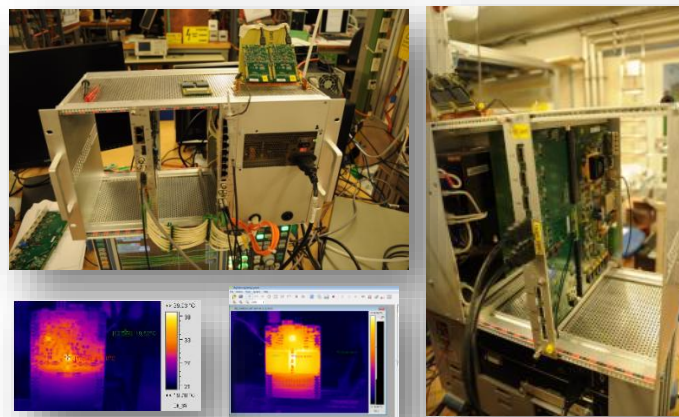
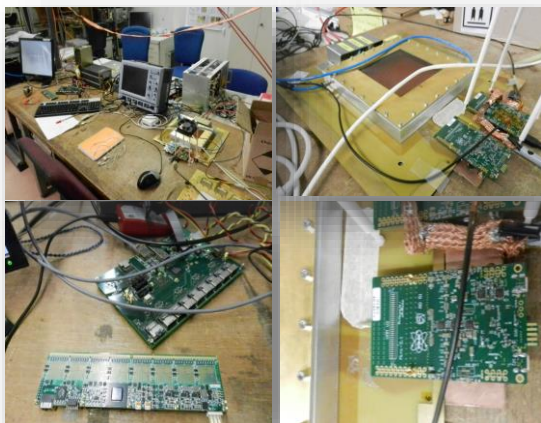
https://indico.cern.ch/event/357738/session/6/contribution/98/attachments/1161455/1672364/MLupberger_ID98.pdf

	Task 13.3.1	AIDA 2020 <u>Key</u> /Partner Institutes
Milestone [M36]	VMM (ongoing activities from ATLAS NSW, ESS, RD51, ALICE FoCal)	<u>CERN</u> : H. Muller, E. Oliveri

Status: Activity going on (**without support from AIDA2020 until now**) on the development of a VMM hybrid compatible with the SRS and of a Digital Interface Card (D-CARD).

New bunch of chips (version 2) ~~will be purchased in the next few months~~ to progress on the characterization of the chip using SRS as DAQ and control system.

ATLAS VMM2 NSW setup in GDD laboratory (ATLAS and RD51 SRS hybrid tests)



H.Muller & ALICE FoCAL Setup in GDD laboratory VMM2-SRS hybrids and D-Card.

AIDA2020 resources to support development for R&D and Generic use of the chip in our community.

	Task 13.3.1	AIDA 2020 <u>Key/Partner</u> Institutes
Milestone [M36]	GEMROC	<u>AGH Krakow</u> : B. Mindur CERN: E. Oliveri

Status: ~~ongoing technical discussion with eicSys (ATCA SRS)~~ for the development of the parts needed to interface the FE chip with the SRS (hybrid and adapter card).

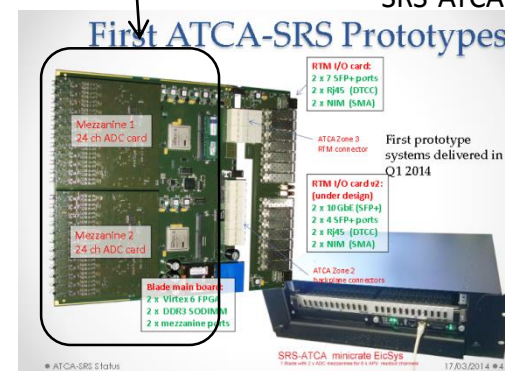
~~If the technical discussion will converge in the next weeks (most likely),~~ a production of about 100 GEMROC chips will be done in end 2015/beginning 2016 (covered by AIDA 2020).

First half of 2016, first SRS compatible prototype of the hybrid (based on the existing version), end of 2016 adapter cards for ATCA SRS ready for test and debugging.

Redesign
of Hybrid
and ATCA
SRS FEC
Adapter
Card



SRS-ATCA



	Task 13.3.1	AIDA 2020 <u>Key/Partner Institutes</u>
Milestone [M36]	Timepix3 (LC-TPC)	<u>University of Bonn</u> : K. Desch, J. Kaminski

Status: PCB layout of chip carrier/FEC extension cards ongoing. On schedule with the original plan.

CERN, as leading institute and beneficiary of the EU fund , will transfer part of the AIDA 2020 resources to Bonn University (thanks to the involvement of Bonn University as leader of other AIDA2020 WPs).

This will allow us to use the EU resources in the best and more efficient way .

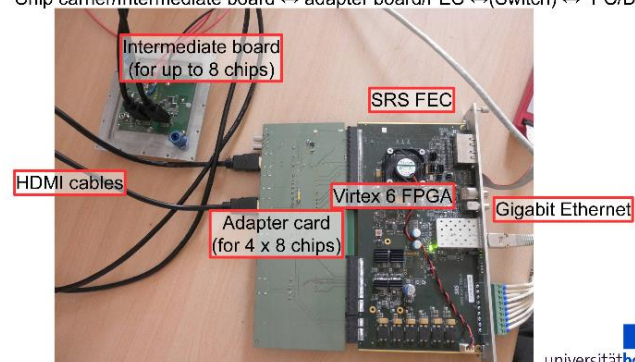
Based on the existing TimePix-SRS interface developed @ Bonn/Desy

Implementation of the ASIC



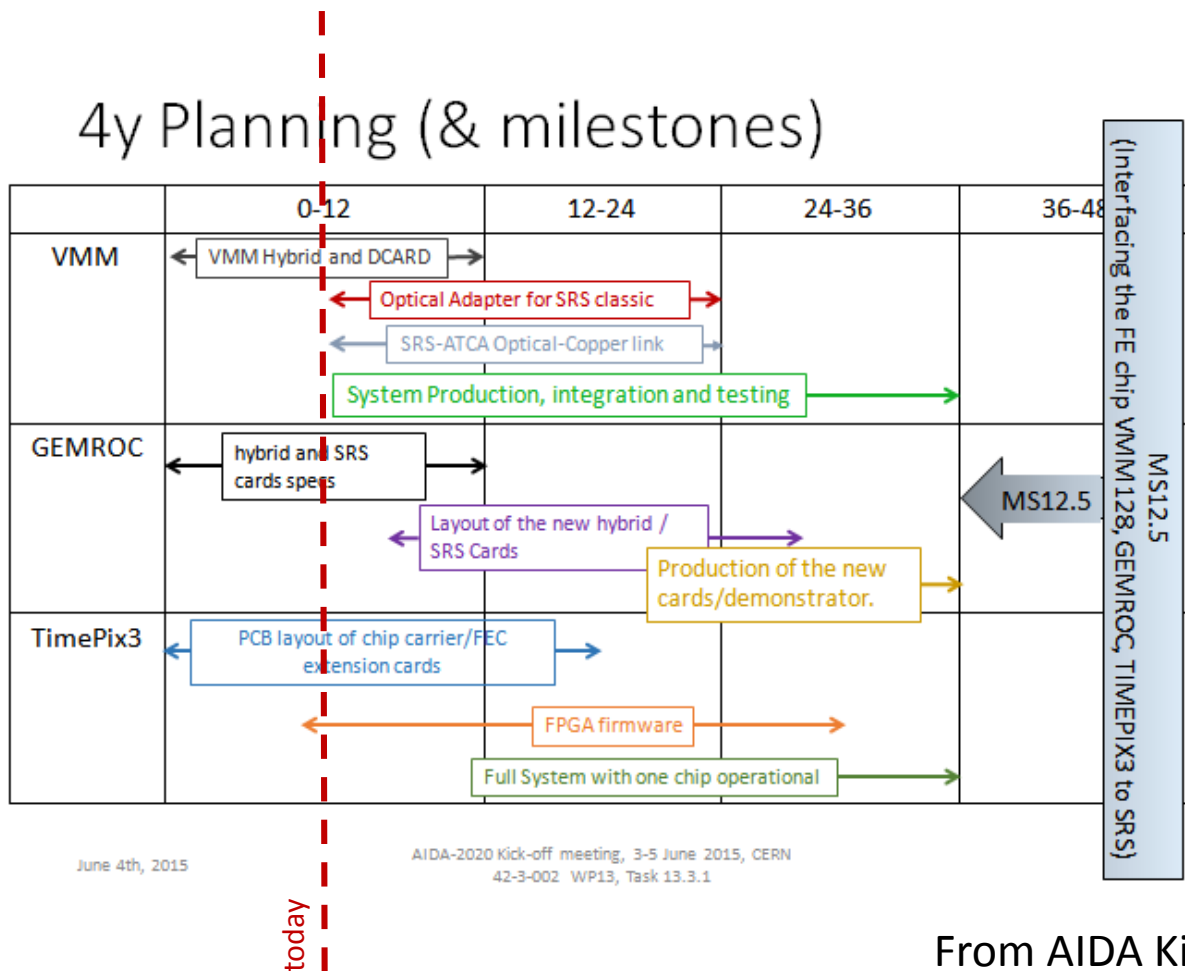
Readout chain:

Chip carrier/Intermediate board ↔ adapter board/FEC ↔(Switch) ↔ PC/DAQ



Michael Lupberger TWEPP2015

4y Planning (& milestones)



From AIDA Kick-Off Meeting

WP13 Task 13.3.2: Development of cheap, standard MPGD dedicated laboratory instruments

High Voltage

Pico-Amps
detection



Preamp/Amp
readout...
Event by event
signal detection,
Triggering

Laboratory instrumentation for MPGDs (characterization)...

WP13 Task 13.3.2:

Development of cheap, standard MPGD dedicated laboratory instruments

	Task 13.3.2	Ref. Institute/Person
Deliverable [M24]	High Voltage Power Supply for MPGD	<u>CERN</u> : H. Muller, E. Oliveri; <u>CEA</u> : P. Colas Wigner: D. Varga; <u>INFN Trieste</u> : S. Dalla Torre
	(Floating) Pico ammeter	<u>CERN</u> : H. Muller, E. Oliveri, <u>INFN Trieste</u> : S. Dalla Torre, S. Levorato; Wigner: D. Varga
	Signal Processing	<u>CERN</u> : H. Muller, E. Oliveri
	Monitoring and Control Unit	<u>CERN</u> : F. Brunbauer, F. Resnati, H. Muller, E. Oliveri
	Regeneration Gas System	<u>CEA</u> : P. Colas

	Task 13.3.2	Ref. Institute/Person
Deliverable [M24]	High Voltage Power Supply for MPGD	<u>CERN</u> : H. Muller, E. Oliveri; CEA: P. Colas Wigner: D. Varga; INFN Trieste: S. Dalla Torre

Instr.1: Compact HV for MPGD [Deliverable – M24]

Status: Compact active voltage divider to provide high voltage with high precision to multi electrodes MPGDs. Prototype for GEM detectors under test. Zero-version of protection circuit and monitoring unit under test now.

3D CAD of AVD, protection and monitoring circuit

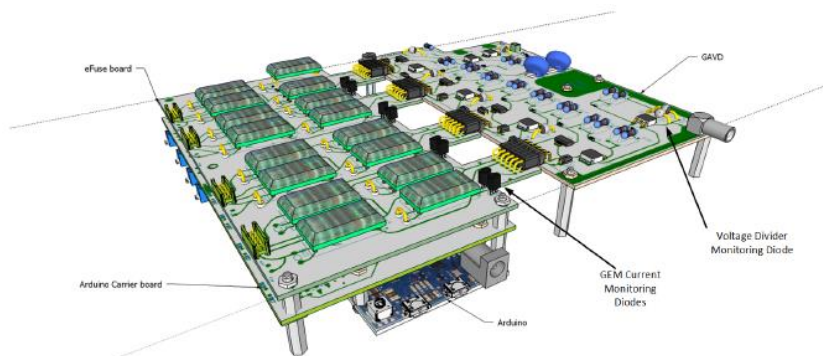


FIGURE 1.7: Complete circuit design for power supply and monitoring

H. Muller et al.

AVD Kept as deliverable for this task because of its status. AIDA2020 support can be nevertheless used for parallel developments carried on by partners.

	Task 13.3.2	Ref. Institute/Person
	(Floating) Pico ammeter	<u>CERN</u> : H. Muller, E. Oliveri, <u>INFN Trieste</u> : S. Dalla Torre, S. Levorato; Wigner: D. Varga
	Signal Processing	<u>CERN</u> : H. Muller, E. Oliveri
	Monitoring and Control Unit	<u>CERN</u> : F. Brunbauer, F. Resnati, H. Muller, E. Oliveri

Ongoing activities in the involved institutes

[Low current measurements (not floating - FemtoBox (CERN), floating (Trieste)), Signal Processing (Pick-Up Box (CERN)), Monitoring & Control system (MoCos (CERN)).]

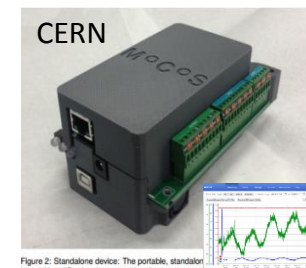
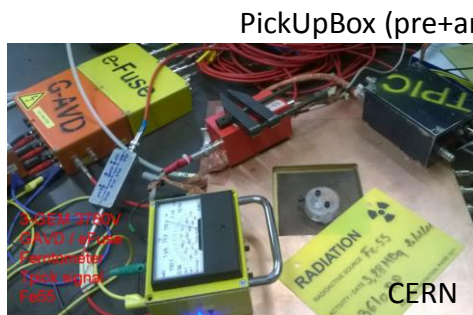


Figure 2: Standalone device: The portable, standalone housed in a 3D printed case and has its connectors arranged around one device.

Arduino Based Monitoring and Control Unit

Status: prototypes existing or almost finalized.

AIDA2020 planned to be used on the final Engineering steps and for improvement.

	Task 13.3.2	Ref. Institute/Person
	Regeneration Gas System	<u>CEA</u> : P. Colas

Gas System Regeneration (to be better defined and discussed with our partners (CEA))

E-Fuse Circuits

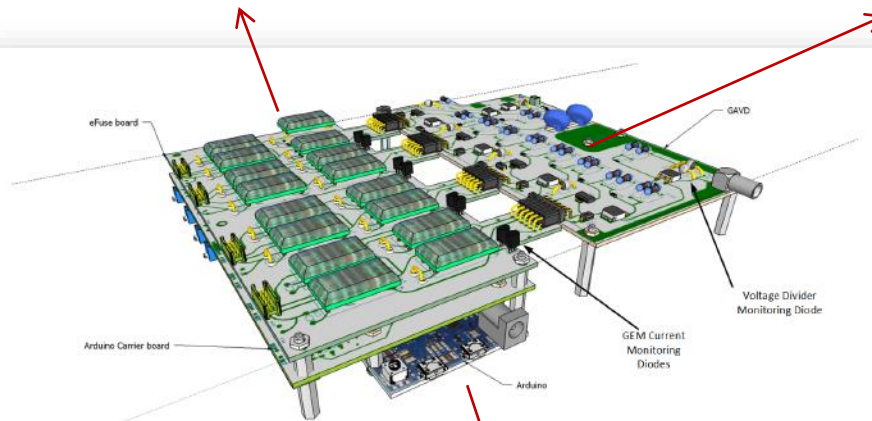
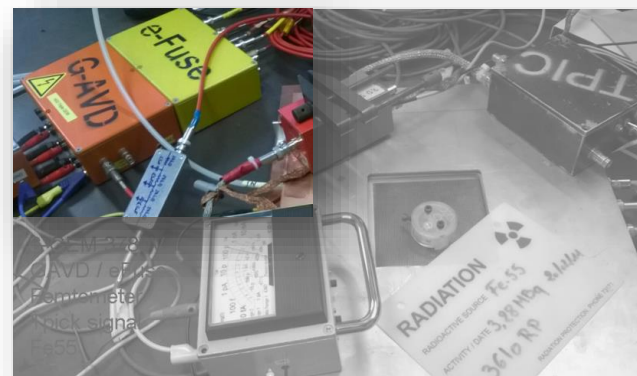


FIGURE 1.7: Complete circuit design for power supply and monitoring

AVD (Active Voltage Divider) Suitable for multistage MPGDs

Voltage Ratio between
all stages hardware
defines (resistors)



Chapter 1. Summer Student Report - V. Karaventzas

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Arduino-based monitoring Units

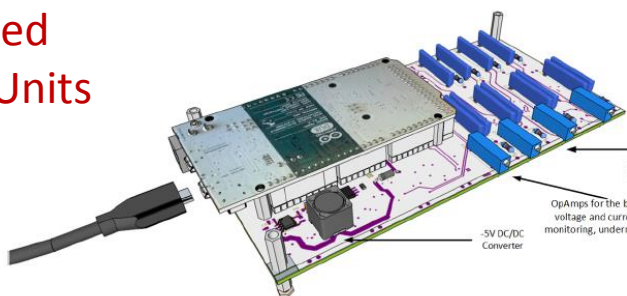
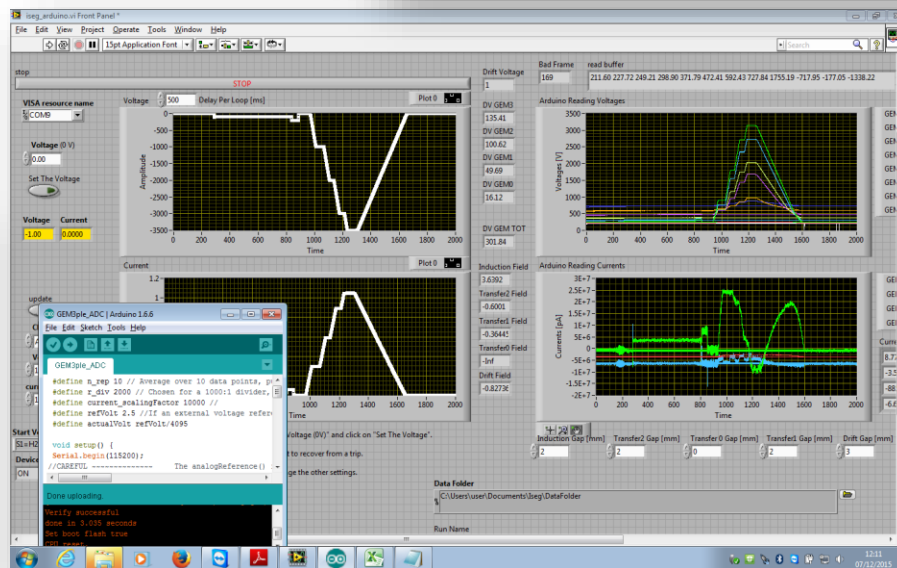


FIGURE 1.8: Arduino carrier board with the voltage and current measuring schemes

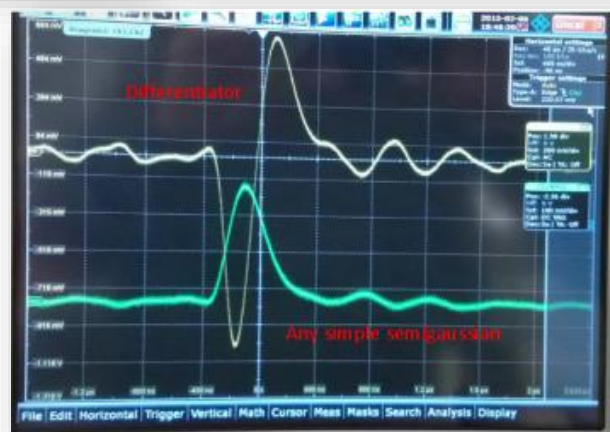
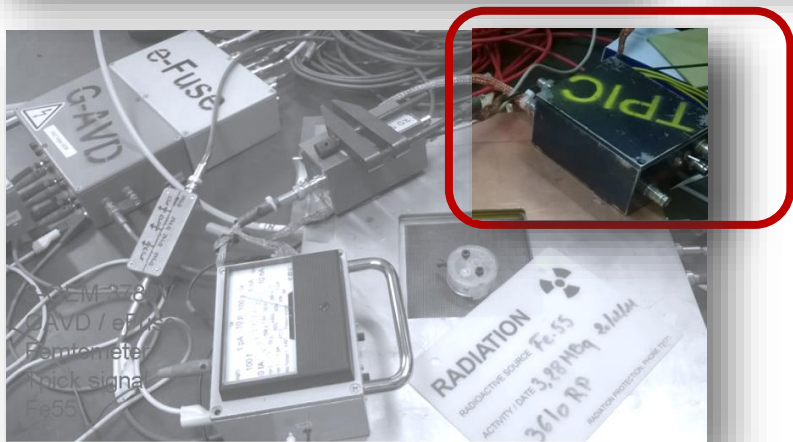
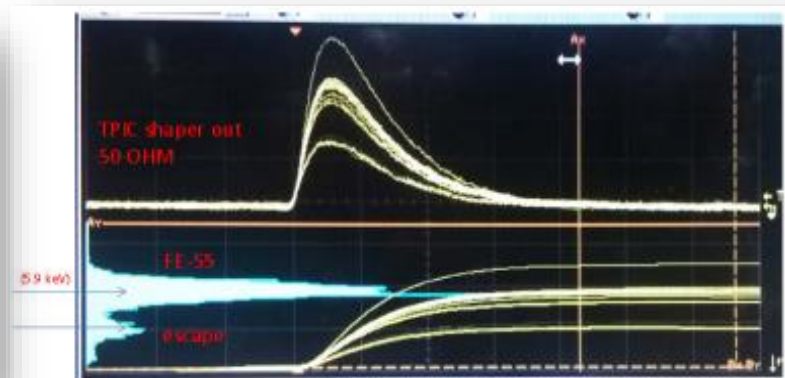
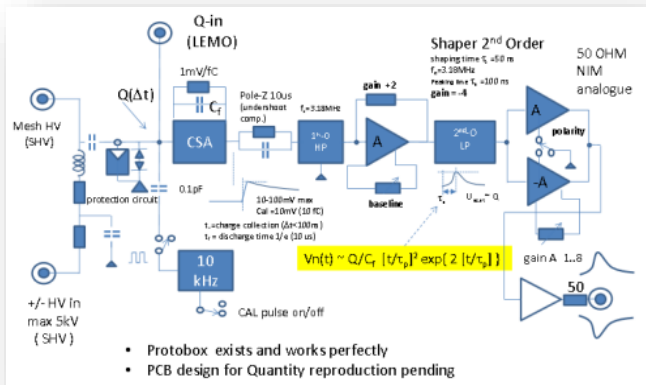


Control and Monitoring Software

H. Muller et al.

Voltages
Currents

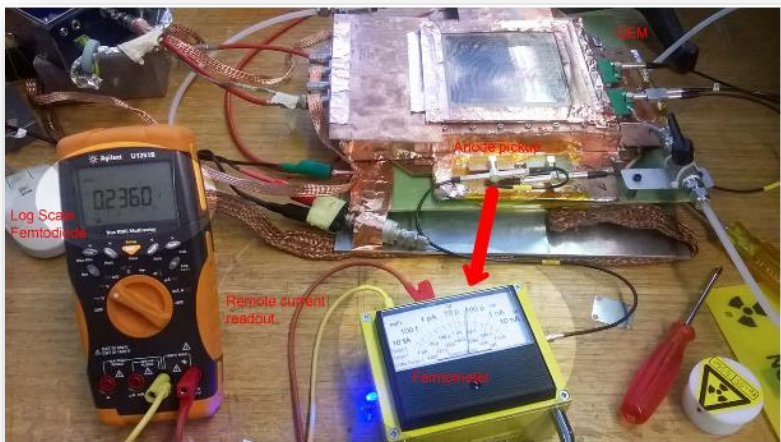
APIC and TPIC: analog and trigger pickup



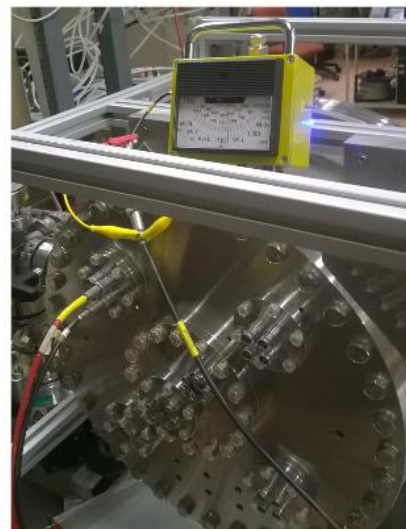
Energy, S/N ratio, signal shape optimization, triggering

H. Muller et al.

https://indico.cern.ch/event/365380/session/4/contribution/34/attachments/726462/996914/Project_News_GAVD_TPIC_FEMTO.pdf



Application GEM-foils resistivity in vacuum*



With increasing vacuum and externally applied HV field, the GEM foil leakage current after some time indicates Orders > 50 GOHM

17/01/2014

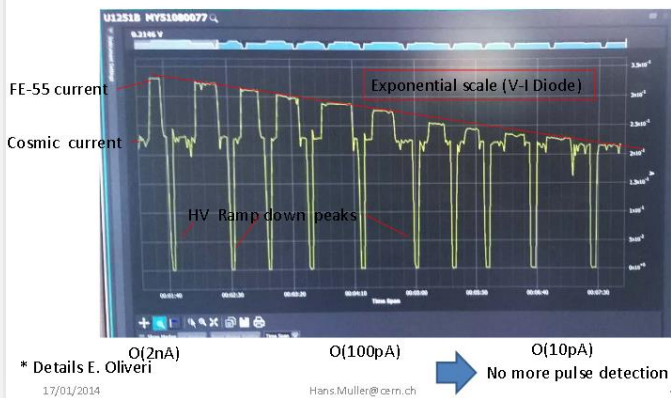
Hans.Muller@cern.ch

* Details F. Resnati

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Leakage Current Measurements

GEM Amplification Ramp-down*



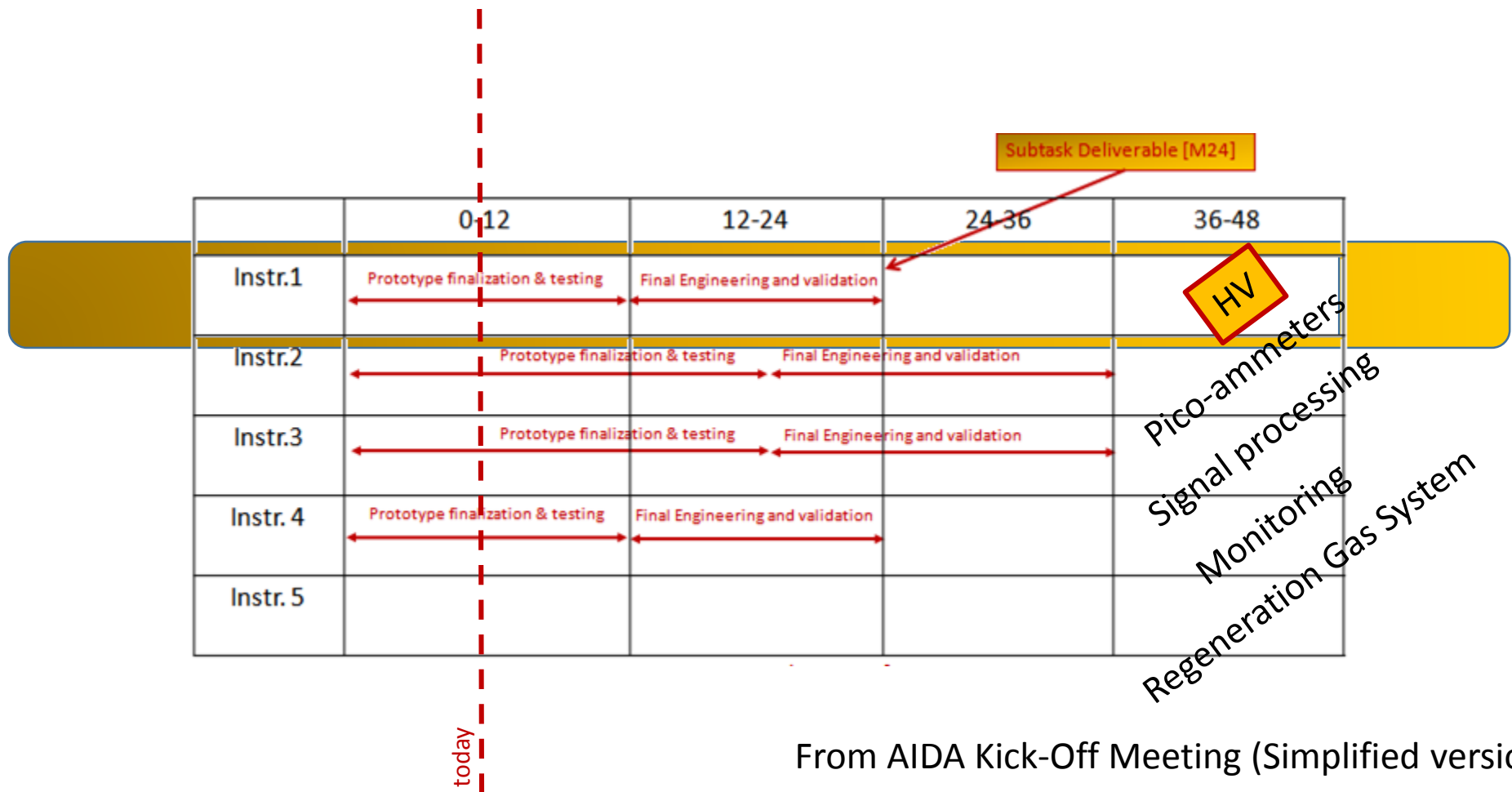
Gain Calibration

* Details E. Oliveri

17/01/2014

Hans.Muller@cern.ch

40



From AIDA Kick-Off Meeting (Simplified version)

Task 13.3.1 Budget (FE Chip for SRS)

AIDA 2 - WP Frontier Gas Detectors - Task 12.3.1: Tools to easy the detector progress: interfacing FE-chips specific to gas detectors to th

For input data, only fill the white areas below
Please fill out the Beneficiary and Institute short name columns (see example below for CERN and INFN)

Beneficiary short name*	Institute	Person - months	Monthly personnel costs	Personnel direct costs	Travel direct costs	Equipment and consumables	Other direct costs	Sub-contracting costs
CERN		10.00	7,300.00	73,000.00	10,000.00	21,600.00		
Total		10.00	7,300.00	73,000.00	10,000.00	21,600.00	0.00	0.00

50k from EU

Material direct costs	Total direct costs	Total indirect costs**	Total costs (direct + indirect)	EC requested funding	Description of Partner Contribution to the Task
31,600.00	104,600.00	26,150.00	130,750.00	50,000.00	task responsibility and coordination (3 institutes in total)
31,600.00	104,600.00	26,150.00	130,750.00	50,000.00	

Task 13.3.2 Budget (Instrumentation)

AIDA 2 - WP Frontier Gas Detectors - Task 12.3.2: Tools to easy the detector progress: development of cheap, standard MPGD dedicated lab

For input data, only fill the white areas below
Please fill out the Beneficiary and Institute short name columns (see example below for CERN and INFN)

Beneficiary short name*	Institute	Person - months	Monthly personnel costs	Personnel direct costs	Travel direct costs	Equipment and consumables	Other direct costs	Sub-contracting costs
CERN		11.00	7,300.00	80,300.00	10,000.00	20,000.00		
Total		11.00	7,300.00	80,300.00	10,000.00	20,000.00	0.00	0.00

70k from EU

Material direct costs	Total direct costs	Total indirect costs**	Total costs (direct + indirect)	EC requested funding	Description of Partner Contribution to the Task
30,000.00	110,300.00	27,575.00	137,875.00	70,000.00	task responsibility and coordination (4 institutes in total)
30,000.00	110,300.00	27,575.00	137,875.00	70,000.00	

Possibility of changing the resource sharing between the two subtask