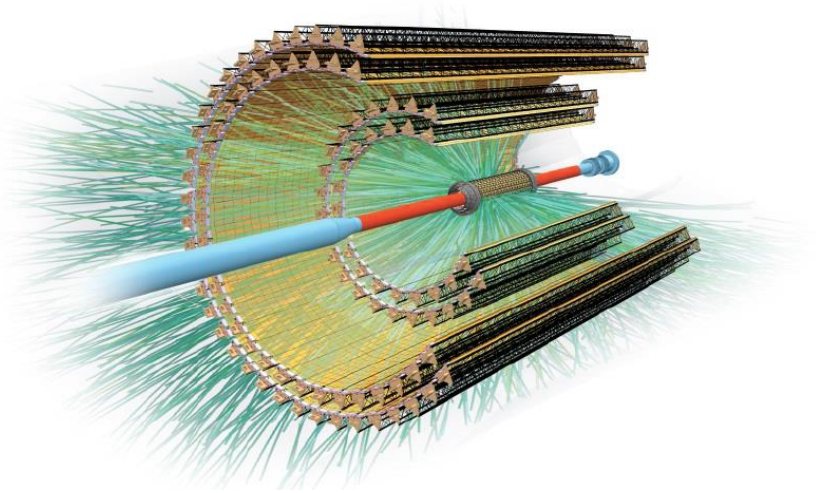
Update on Pixel Chip for the ALICE ITS Upgrade

Luciano Musa - CERN



LHCC Week – Detector Upgrade Session
1st December 2015

Update on the Pixel Chip for the ALICE ITS Upgrade

A Large Ion Collider Experiment

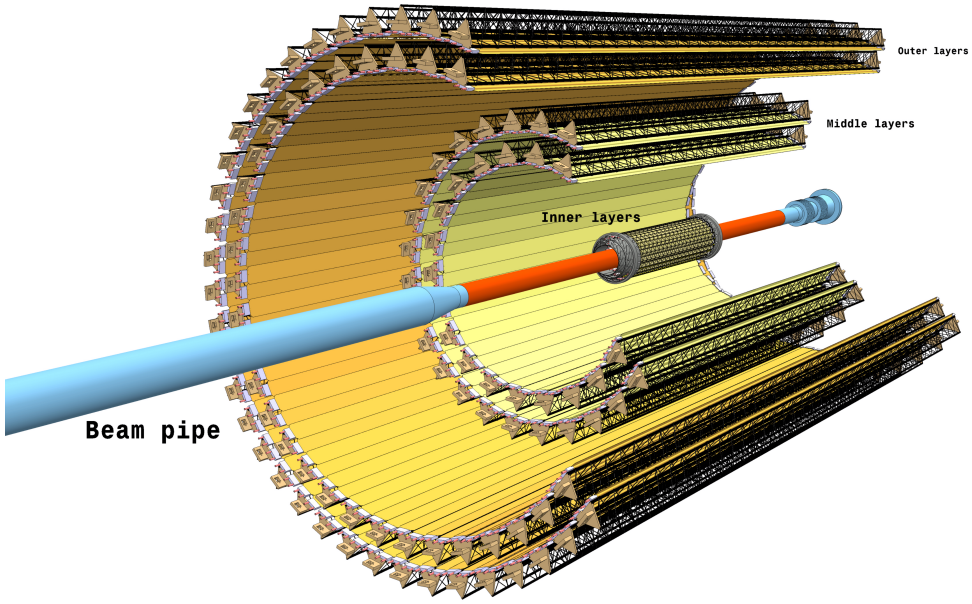
OUTLINE

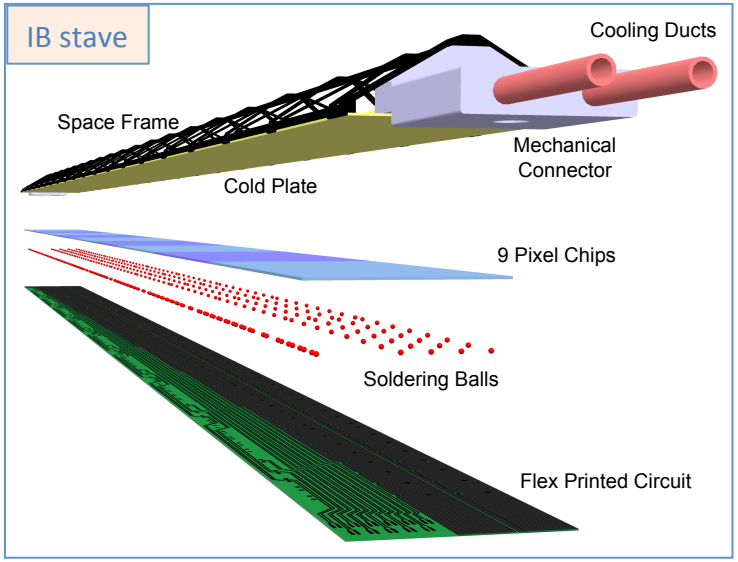
- ITS layout and Pixel Chip General Requirements
- Pixel Chip (ALPIDE) Overview and Status
- pALPIDE-2 Main Design Features and Performance
- Engineering Design Review
- pALPIDE-3 Preliminary Results
- Towards final chip

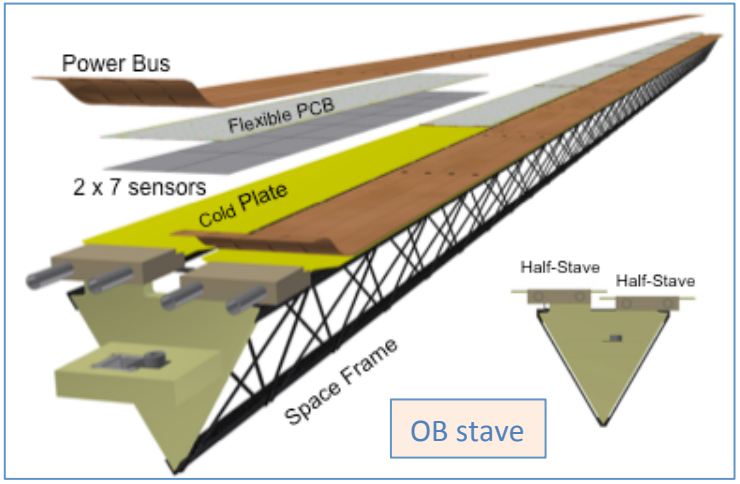
New ITS Layout

A Large Ion Collider Experiment

ALICE







- 7-layer barrel based on CMOS sensors
- Radial coverage 22 – 400 mm
- Total active area ~10m^2
- ~ 24,000 pixel chips (12.5 G pixels)
- Radiation: ~2.7 Mrad (~1.7x10^{13} 1MeV n_{eq}/cm^2) including safety factor 10

PIXEL Chip – General Requirements

A Large Ion Collider Experiment

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General Requirements and ALPIDE Specifications(*)

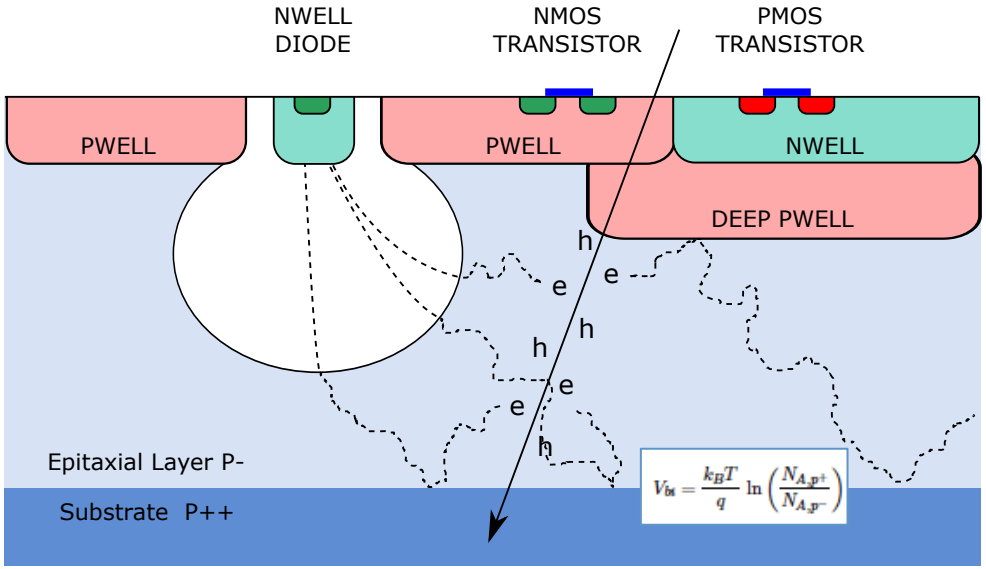
Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	$< 10^{-5}$ evt^{-1} pixel^{-1} (>> ALPIDE)	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~35)	< 100 (~20)
TID radiation hardness (krad) (*)	2700	100
NIEL radiation hardness (1MeV n_{eq}/cm^2) (**)	1.7 x 10^{13}	1.7 x 10^{12}

(*) Colour code: ALPIDE specifications if different from requirements

(**) 10 x radiation load integrated over approved programme (~ 6 years of operation)

ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process



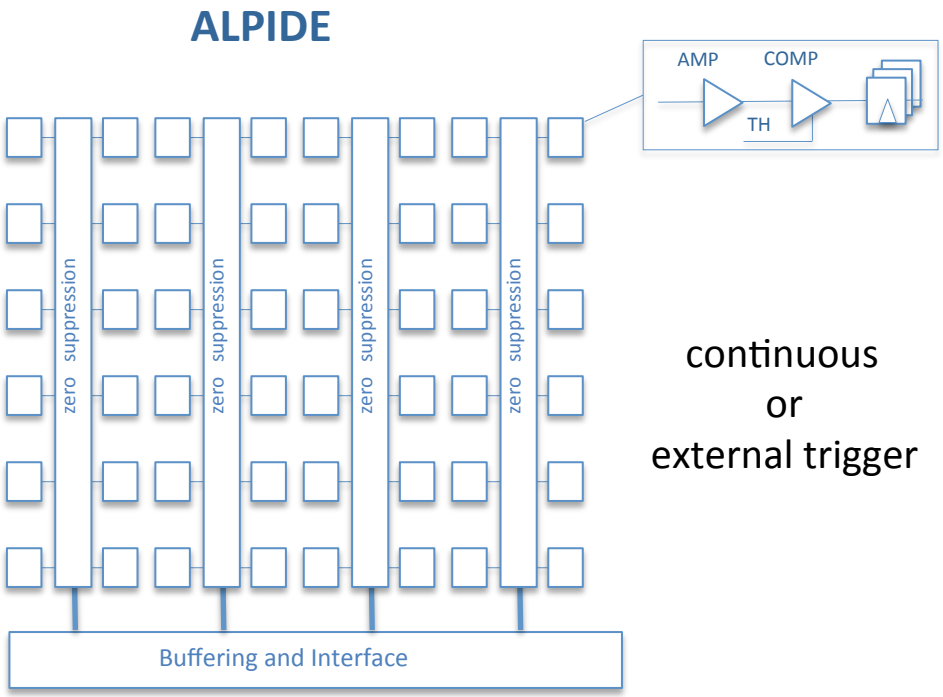
Tower Jazz 0.18 μm CMOS

- feature size 180 nm
- metal layers 6
- gate oxide 3nm

substrate: $N_A \sim 10^{18}$
epitaxial layer: $N_A \sim 10^{13}$
deep p-well: $N_A \sim 10^{16}$

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18μm to 30μm) on p-type substrate
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate (contact from the top) can be used to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors to allow for full CMOS circuitry within active area

ITS Pixel Chip - ALPIDE



continuous
or
external trigger

Architecture

- In-pixel amplification
- In-pixel discrimination
- In-pixel (multi-) hit buffer
- In-matrix sparsification

Key Features

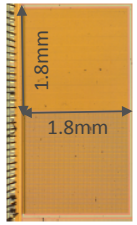
- 28 μm x 28 mm pixel pitch
- Continuously active, ultra-low power front-end (40nW/pixel)
- No clock propagation to the matrix ➔ ultra-low power matrix readout (2mW whole chip)
- Global shutter (<10μs): triggered acquisition or continuous

ALPIDE Development

A Large Ion Collider Experiment

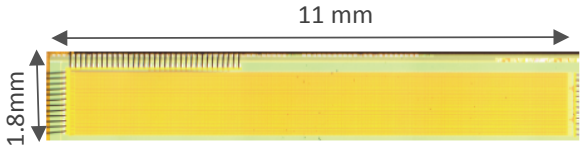
2012 — Explorer

- 20μm x 20μm and 30μm x 30μm pixels (analogue readout)
- pixel geometry, starting material, sensitivity to radiation



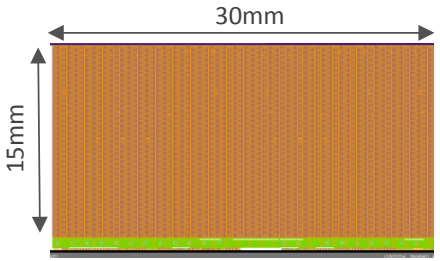
2013 — pALPIDEss-0

- Matrix with 64 columns x 512 rows
- 22μm x 22μm pixels
- (in-pixel discrimination and buffering)
- zero suppression within pixel matrix



May-2014 — pALPIDE-1

- **Full-scale prototype:** 1024 x 512
- 4 sectors with different pixels
- pixel pitch: 28μm x 28μm
- 1 register/pixel, no final interface



May-2015 — pALPIDE-2

- Optimization of several circuit blocks
- final interface: allows integration into ITS modules
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)

Oct-2015 Design Review

Oct-2015 — pALPIDE-3

- 8 sectors with different pixel variants, 3 registers / pixel
- Final interfaces, more features including 1.2 Gbit/s output serial link
- Some optimization for yield improvement
- Characterization ongoing

pALPIDE-1&2 – Main Design Features

A Large Ion Collider Experiment

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ALPIDE full-scale prototypes vers. 1 (2014) and ver.2 (2015)

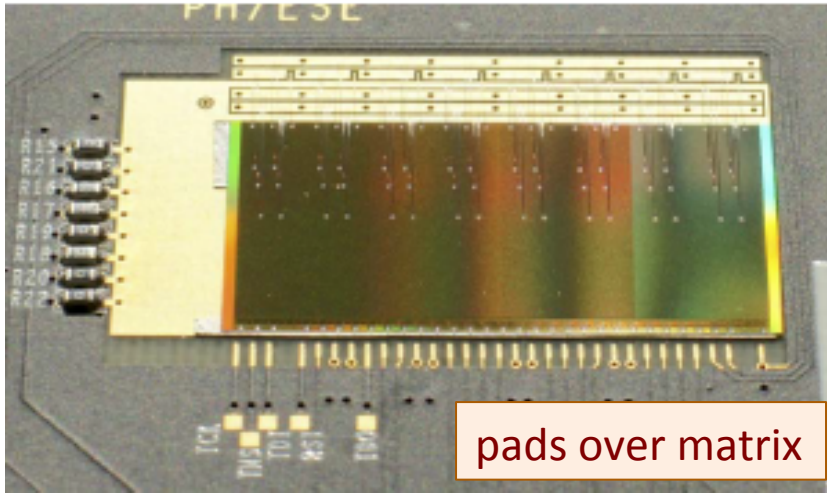


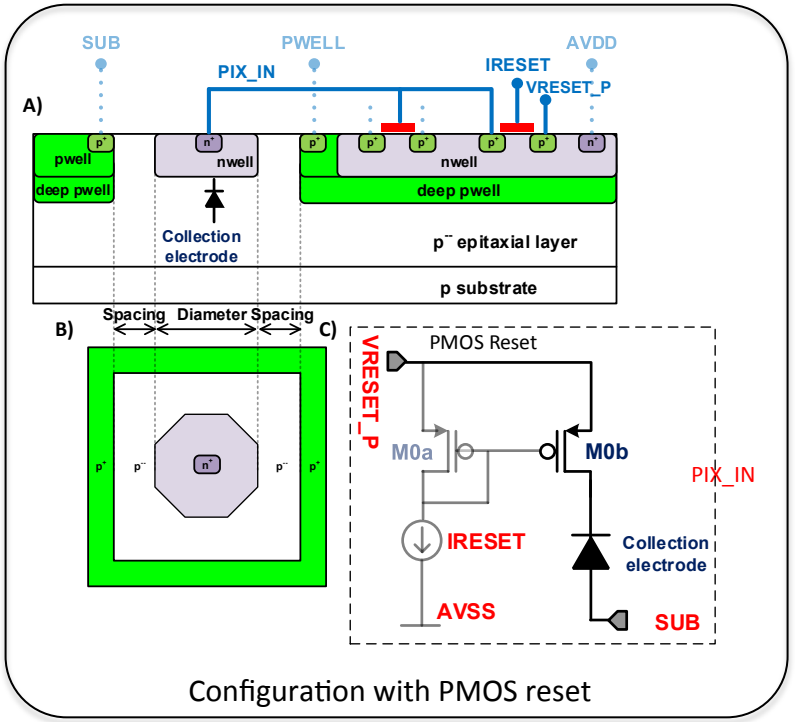
Figure: picture of pALPIDE-2

Main parameters

- Dimensions: 30mm x 15 mm
- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 28μm x 28μm
- Integration time: <10μs
- Power consumption: < 40mW/cm^2
- 4 sectors with different pixels

Matrix divided in 4 sectors, each with 256 cols x 512 rows

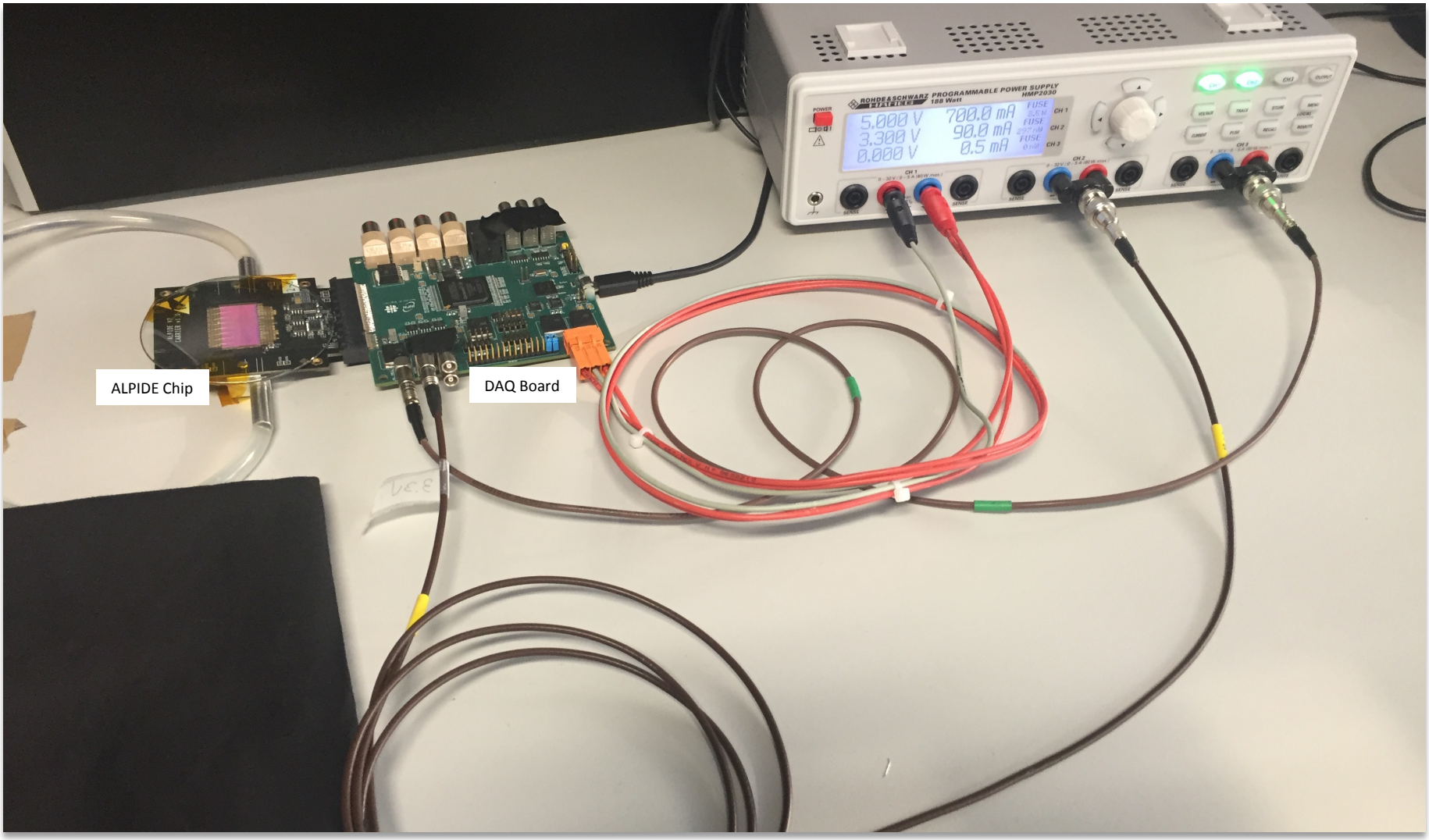
- Collection node: octagonal 2μm diameter
- Spacing NWELL and PWELL: 2μm to 4μm
- 2 reset mechanism: diode, PMOS
- 1 sector with larger (x2) input transistor



Configuration with PMOS reset

Experimental Results

Laboratory Measurements ➔ e.g. noise and thresholds



Experimental Results

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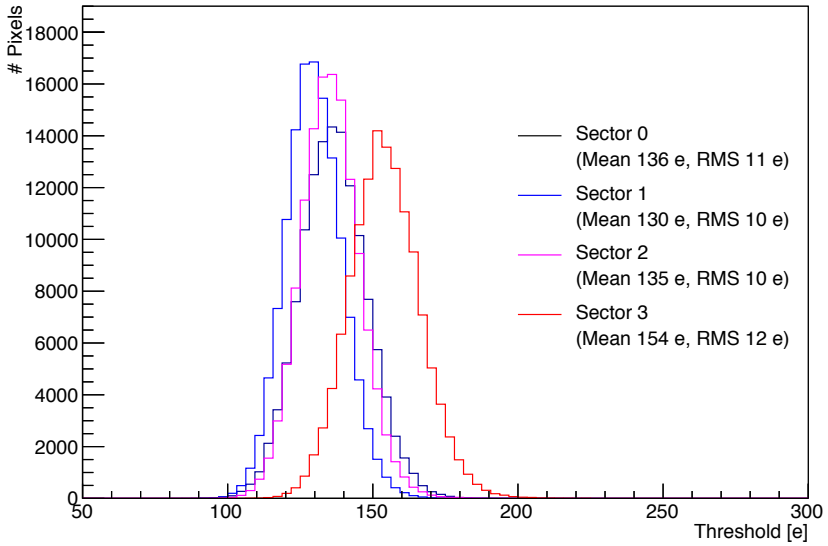
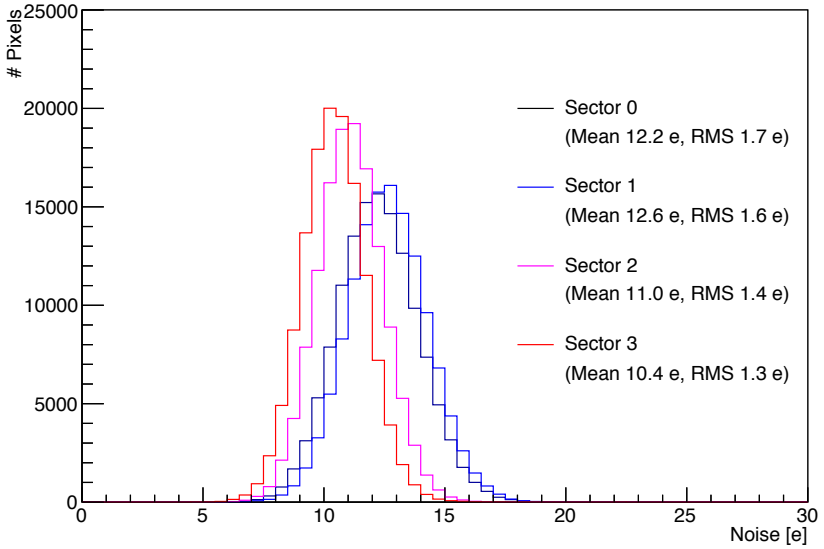
Example of Threshold and Noise Distributions





V_{SUB} = -3V, I_{THR} = 0.5nA, V_{CASN} = 0.95V

- All sectors behave qualitatively similarly
- Noise is about the same value as threshold RMS
- Threshold about 10 x higher than noise
- Threshold 7 x smaller than most-probable energy loss signal of a MIP in 18μm of silicon

Experimental Results

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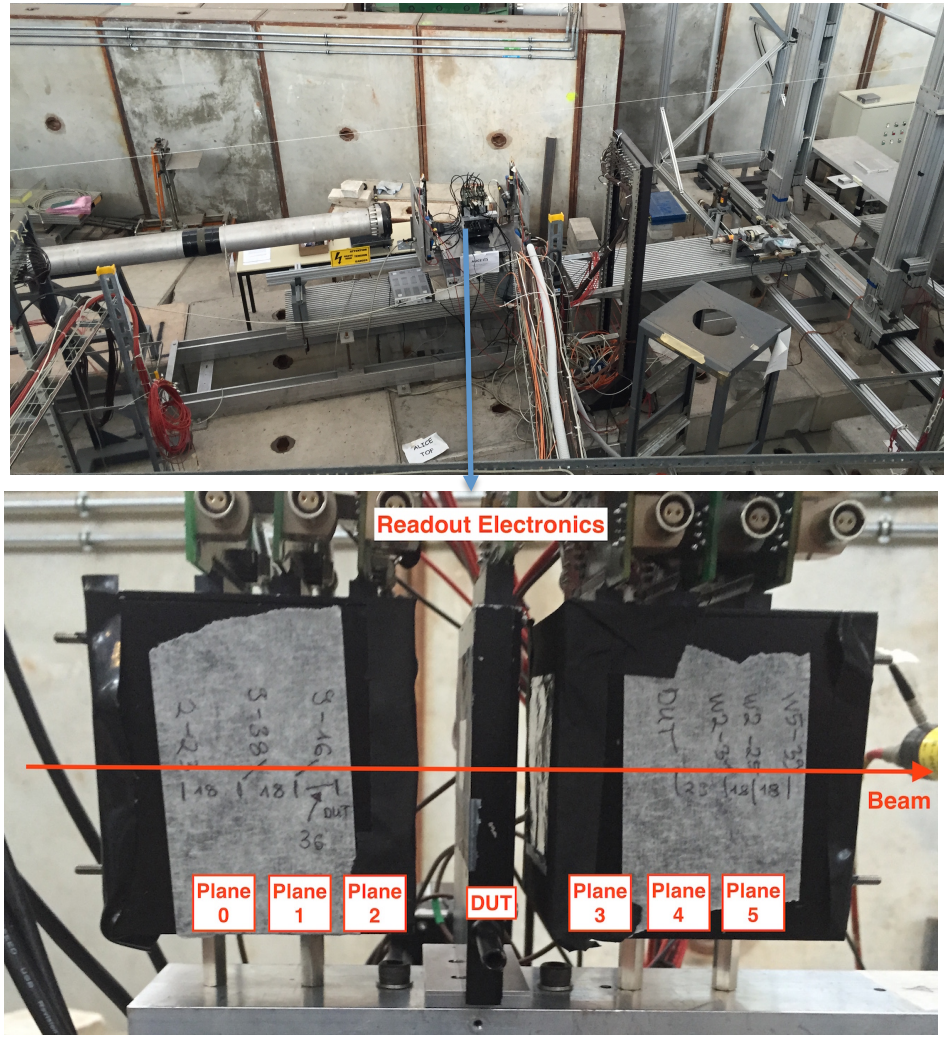
Test Beam Set-up

- 6 GeV/c π^- beam at CERN PS
- 6 reference planes based on pALPIDE-1
- Single pALPIDE-2 as Device Under Test (DUT) in the center
- Track resolution of about 2.8μm (<< 28μm)

Analysis Method

- Extrapolate track from referecne planes trough DUT
- Search for clusters next to extrapolated impinging point ➔detection efficiency
- Obtain **cluster size**
- Compare extrapolated and actual position ➔ **position resolution**

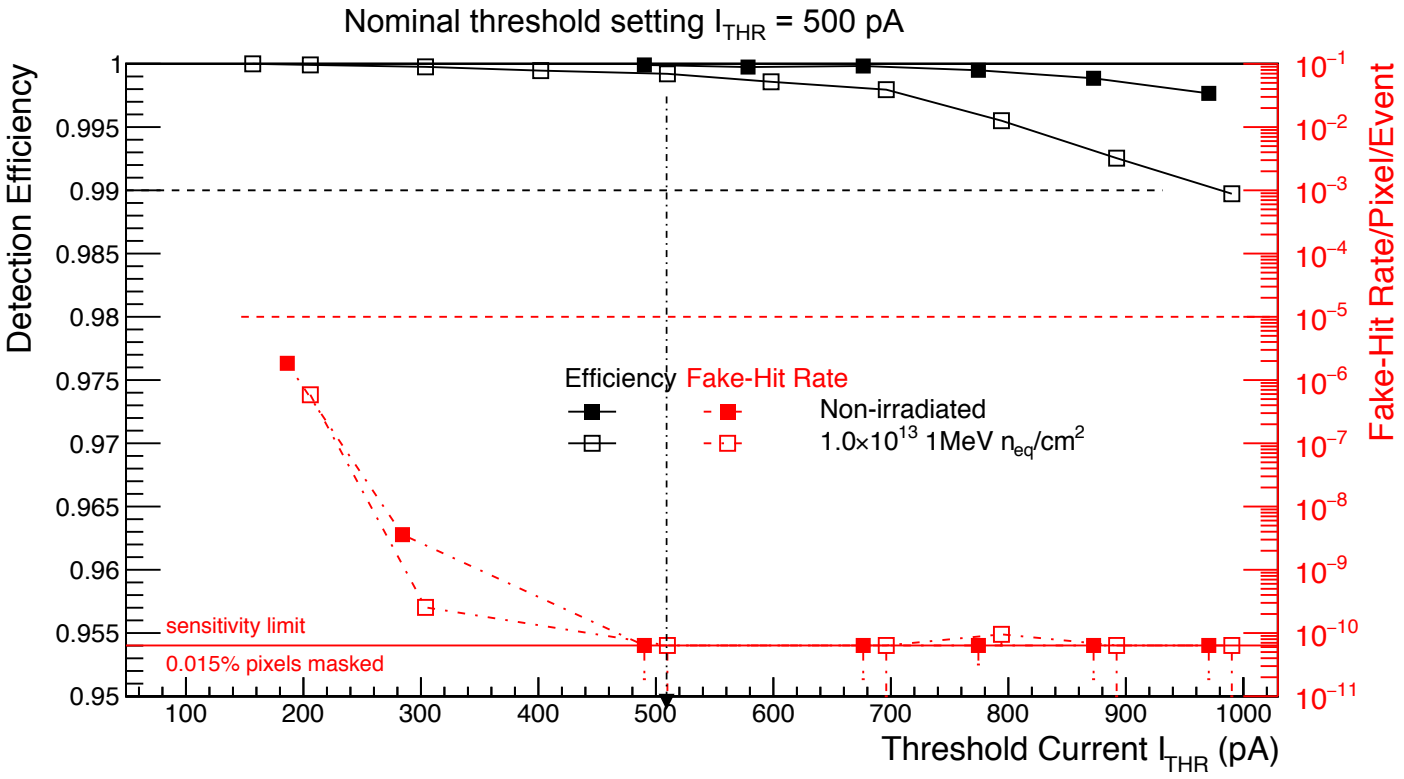


Experimental Results – pAlpide-2

A Large Ion Collider Experiment

Efficiency and fake hit rate

epi=25μm, V_{BB}=-6V, spacing=2μm



$\varepsilon_{det} > 99\%$ @ $\lambda_{fake} << 10^{-5}$ / event/pixel ➡ large margin over design requirements

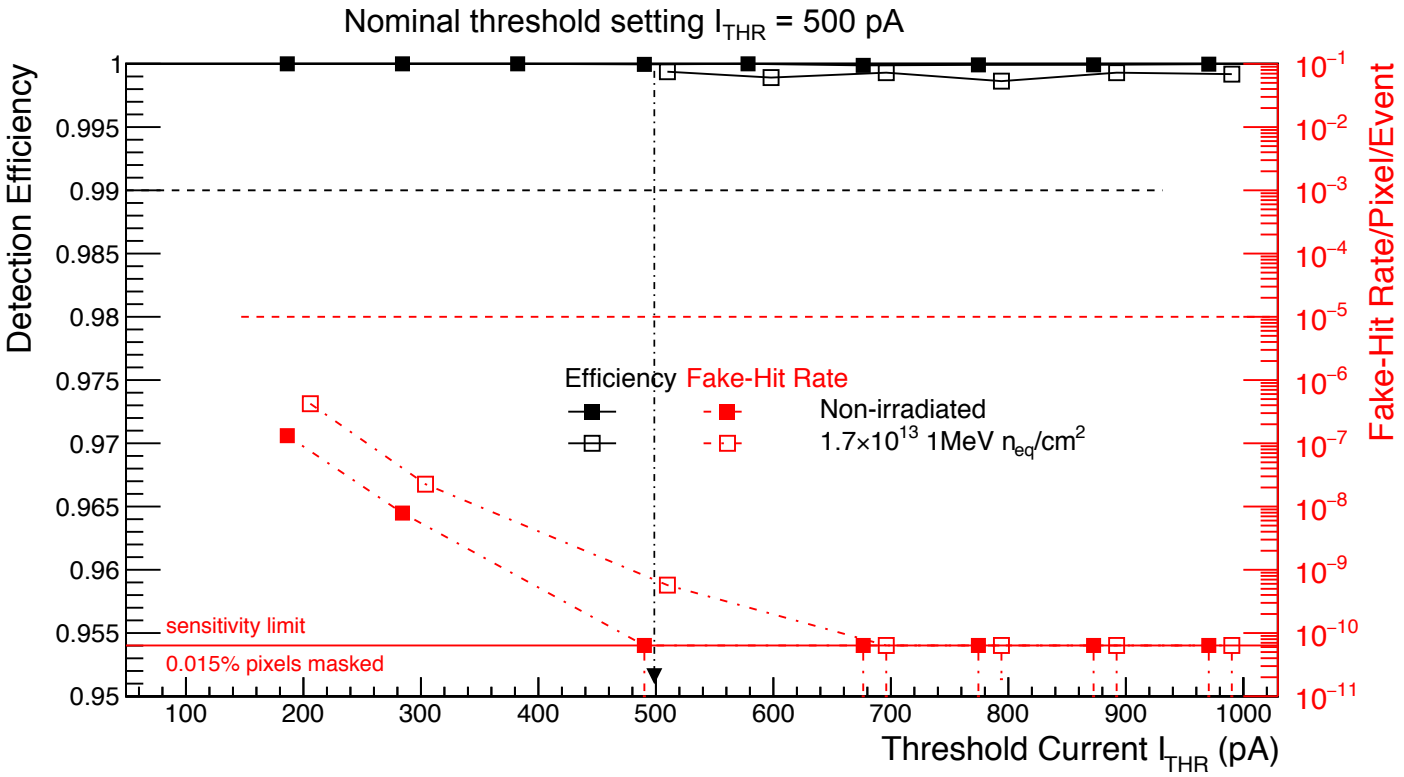
- Results refer to chips with 25μm high-res epi layer, thinned to 50 μm:
  1 non irradiated and 1 irradiated with 10^{13} 1MeV n_{eq} / cm^2

Experimental Results – pAlpide-2

A Large Ion Collider Experiment

Efficiency and fake hit rate

epi=30μm, V_{BB}=-6V, spacing=4μm



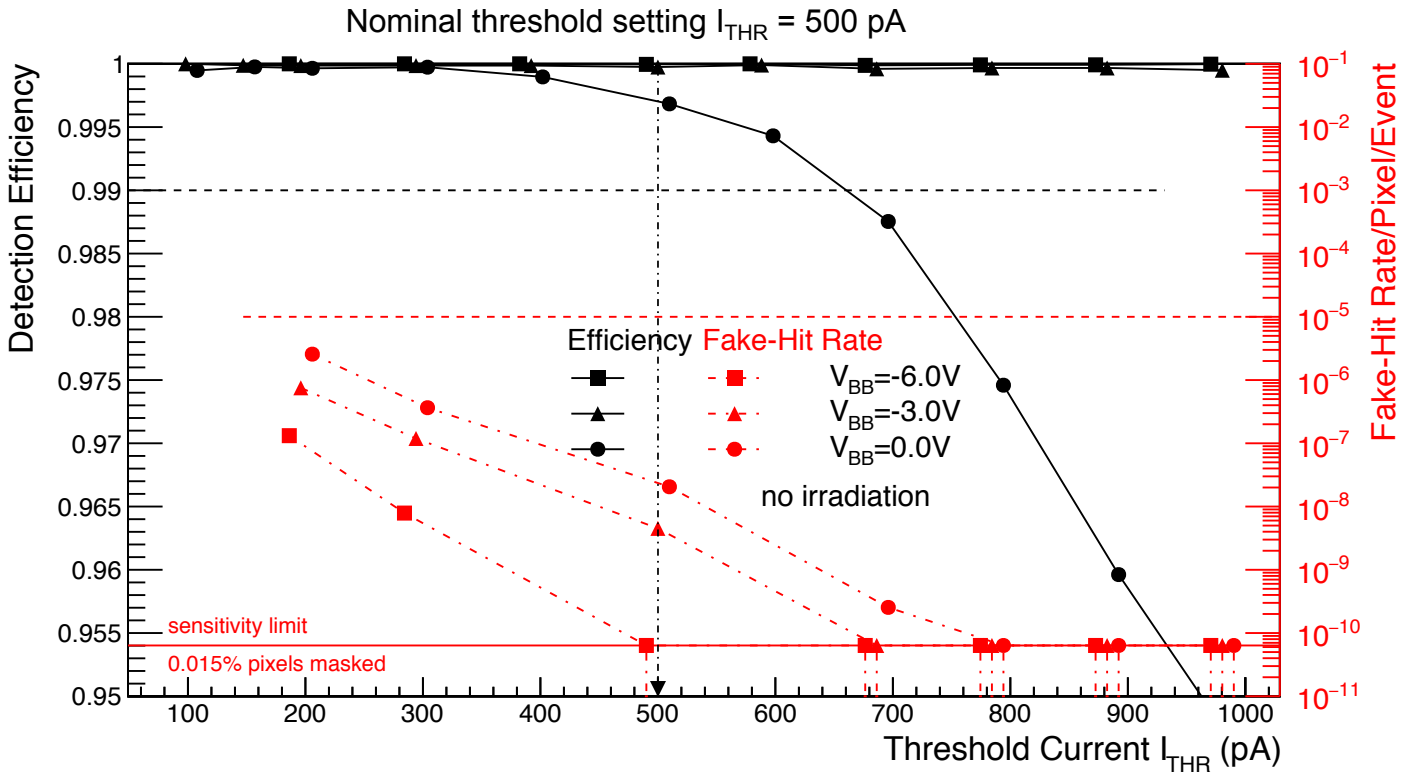
Even larger operation margin for 30μm epi layer and 4μm spacing

- Results refer to chips with 30μm high-res epi layer, thinned to 50 μm:
  1 non irradiated and 1 irradiated with 10^{13} 1MeV n_{eq} / cm^2

Experimental Results – pAlpide-2

Efficiency and fake hit rate

epi=30μm, spacing=4μm



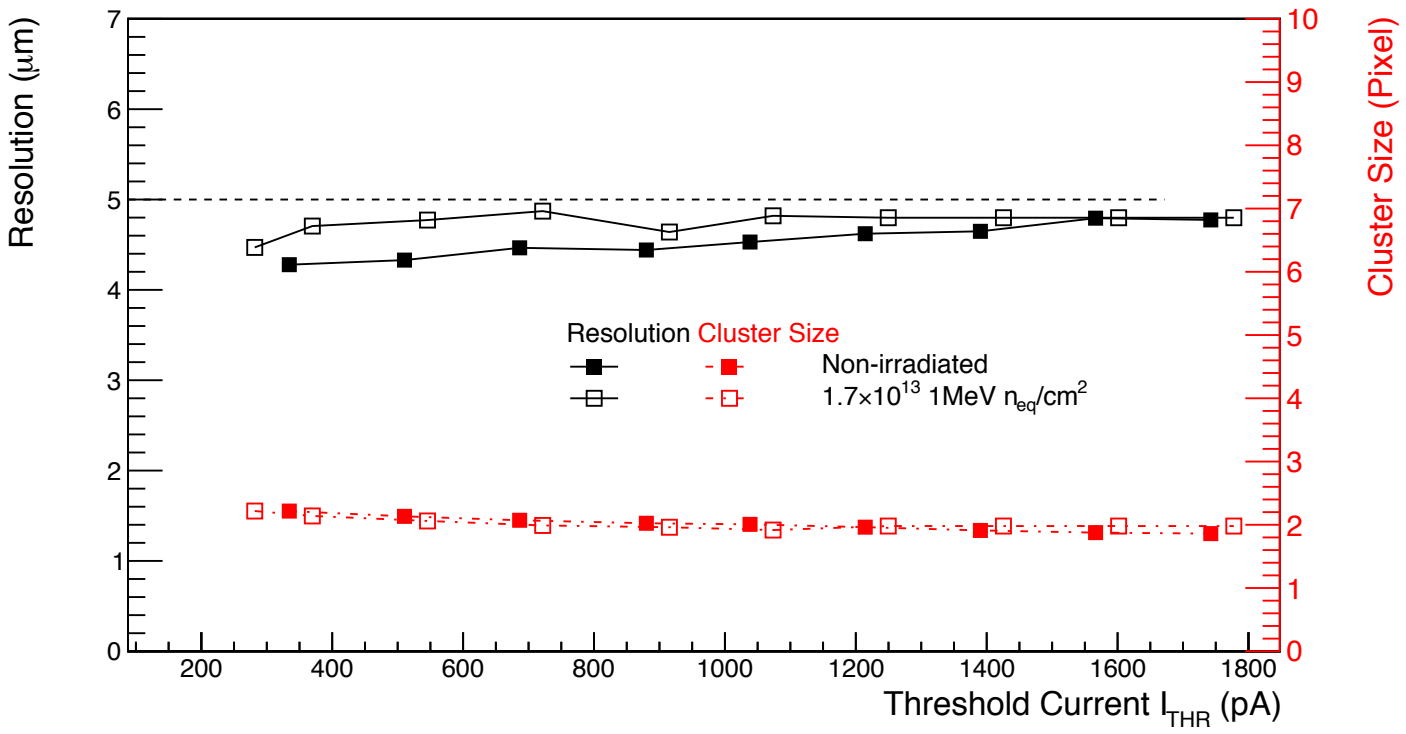
operation margin significantly increased reverse bias voltage

- Results refer to chips with 30μm high-res epi layer, thinned to 50 μm

Experimental Results – pAlpide-2

Spatial Resolution and Cluster Size

epi=30μm, V_{BB}=-6V, spacing=4μm



σ_{det} ≈ 5 μm is achieved before and after irradiation

- Results refer to chips with 30μm high-res epi layer, thinned to 50 μm
  1 non irradiated and 1 irradiated with 1.7x10^{13} 1MeV n_{eq} / cm^2

EDR: pALPIDE-2 results and pALPIDE-3 design

EDR (19 Oct 2015) - Review panel: A. Marchioro (CERN), W. Mueller (GSI), X. Llopart (CERN)

General Assessment

"The reviewers were impressed by the amount and the quality of information provided by the design team for the review. The design team has clearly worked very hard and thoroughly for this project and was orchestrated very competently and effectively by its management team.

The Alice ITS project aims at introducing some very original solutions in the area of pixelated detectors for particle physics, in particular the new technology, the sensor architecture, the extremely low power front-end circuitry and the mechanical thinning of the detector, all are pioneering significant innovations.

Unavoidably innovations cannot be decoupled from risks, but it seems to these reviewers that the team has studied in detail the various aspects of the design of the proposed chip and has used extensively simulation tools to understand its behavior. Of course the usage of simulation tools must be accompanied by and the results digested with a fair amount of common sense, which has been expressed during the review. The engineering team has shown to have worked proactively on a number of issues that were raised during the presentation.

It is also fair to notice that the learning in a new and very promising monolithic technology that this project will hopefully bring to the HEP community does by itself partly justify the risk taken with the project.

Finally, it was really a pleasure to see the enthusiasm and competence of the overall team working on this project."

pALPIDE-3 – Preliminary Results

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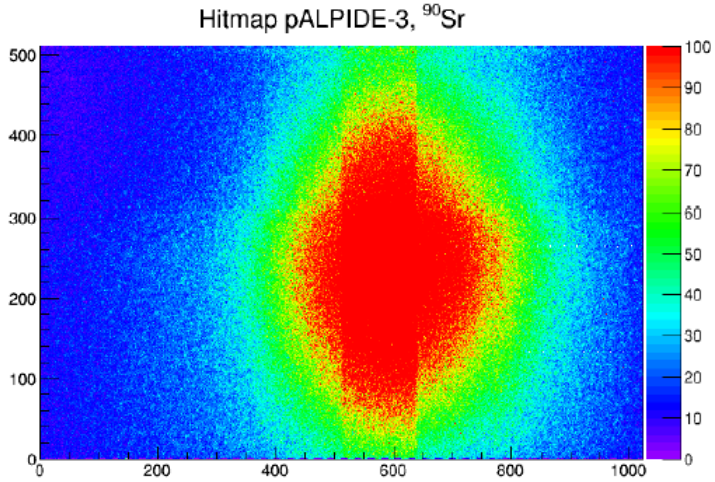
First Laboratory Results

- 29 chips mounted on carrier boards (12 x 18μm, 8 x 25μm, 9 x 30μm)
- 4 chips non working (still to verify whether is the chip or the assembly)
- 25 chips are working in standard tests (➔ 86% yield)

Irradiation tests

- Chips irradiated with neutrons and ionizing radiation
- Done first campaign of SEU/SEL measurements



Test beam

- Only 1 day of test beam at the PS
- Few measurements on one chip (18μm, V_{SUB}=0)

➔ Systematic test ongoing in laboratory

➔ Next test beam in Frascati starting on 7 December

following slides show some very partial and preliminary results

pALPIDE-3 – Preliminary Results

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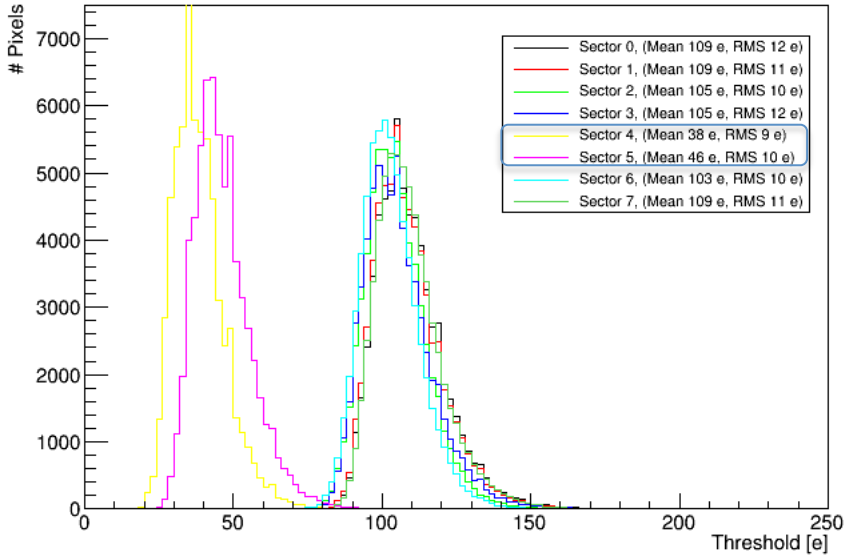
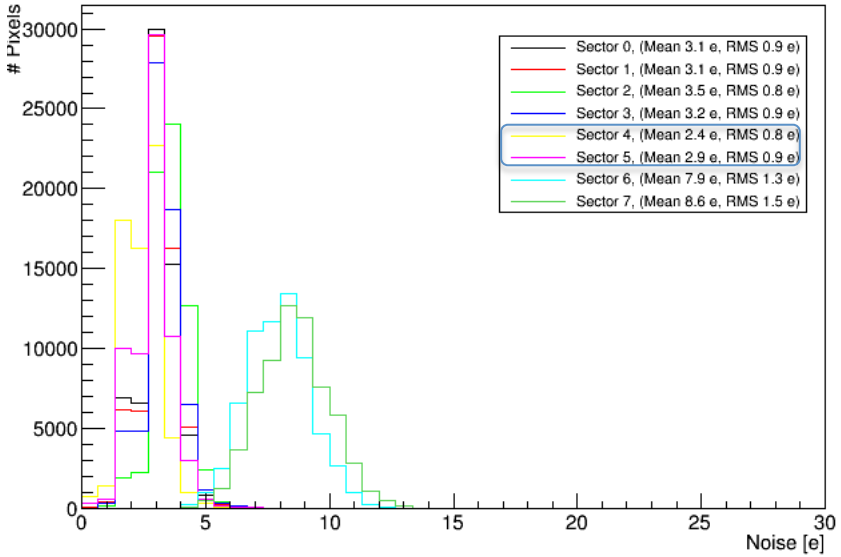
Example of Threshold and Noise Distributions





- Thresholds (left) and Noise (right) distributions for all sectors (ITRH=51)
- Sector 4 and 5 show lower thresholds due to (expected) higher gain
- Sector 6 and 7 PMOS reset, all others diode reset

pALPIDE-3 – Preliminary Results

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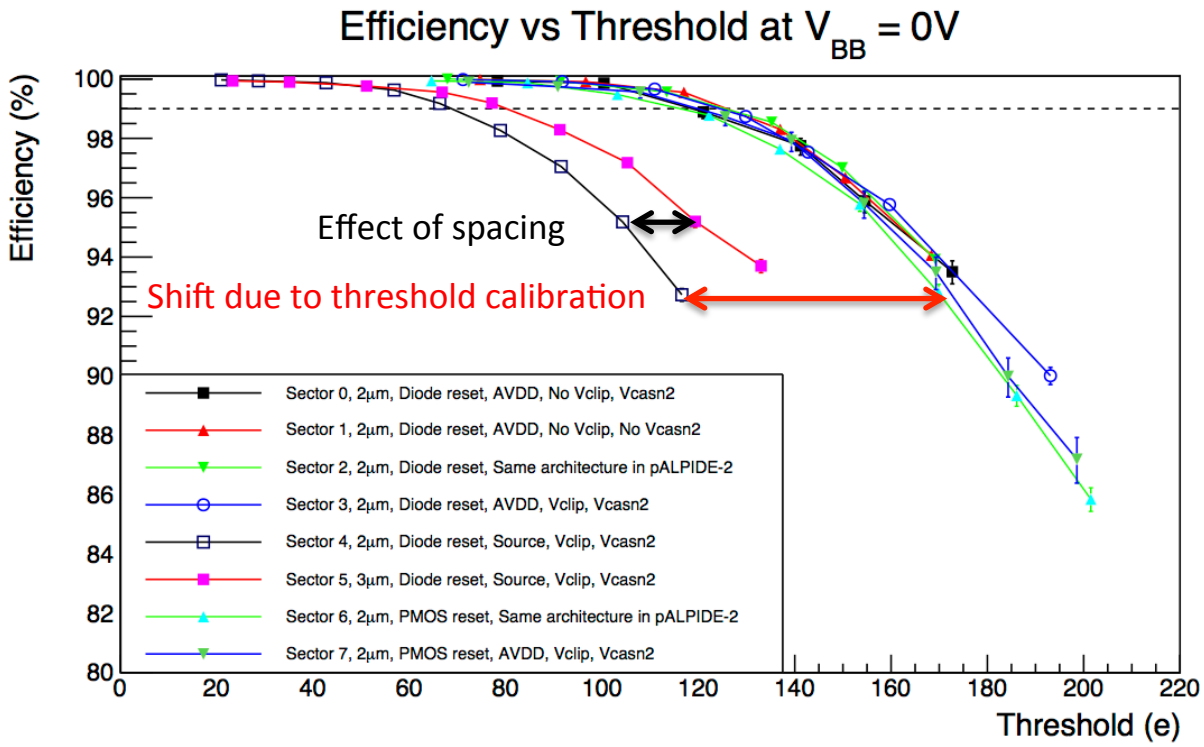
pALPIDE-3 PS test beam

- 1 chip tested for one day (last day of PS test beam)
- Measurements with NO reverse bias voltage



Experimental Results – pAlpide-3

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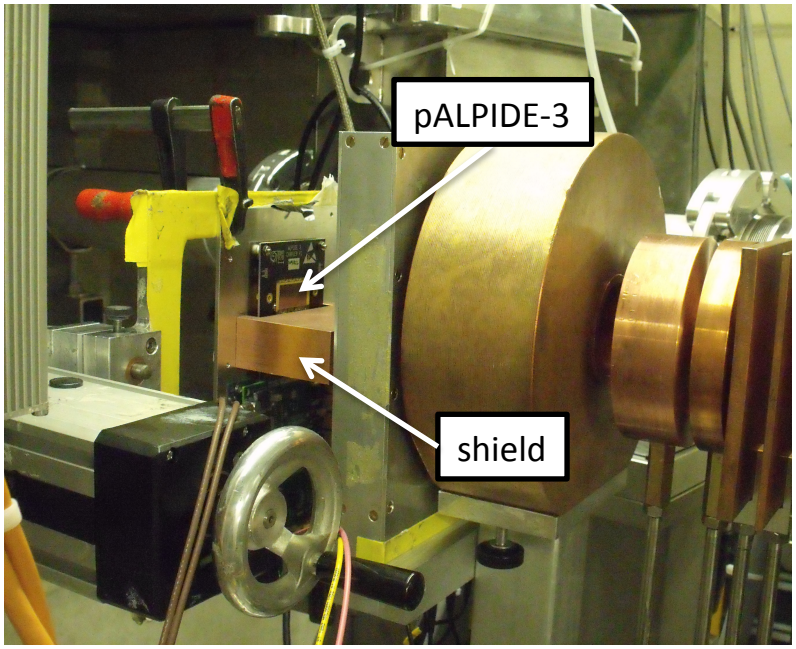
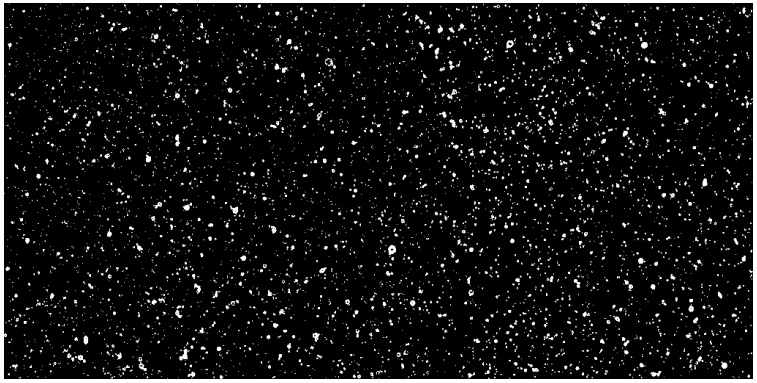
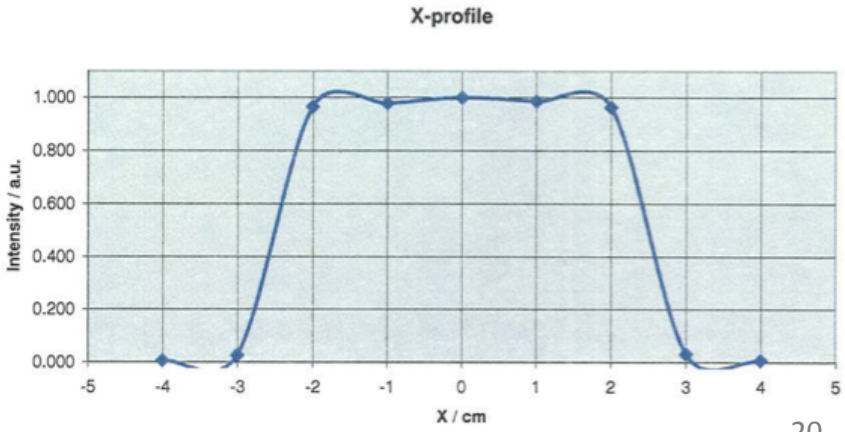
Single Event Upset - Setup

- Proton Irradiation Facility (**PIF**) @ PSI
- 200 MeV protons
- 1.6×10^8 p/cm^2
- Widened beam to cover full pALPIDE-3 chip
- Chip connected to standard readout system
- Cross-sections measured by digitally stimulating the pixels
- Unmasking cross-section verified by looking at beam particles



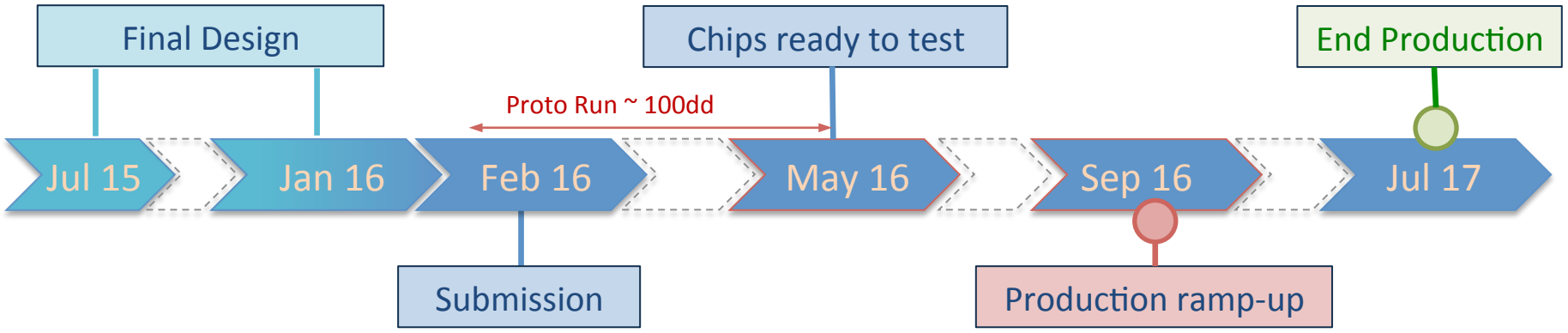
Picture of one event (w/o masking)





ALPIDE Finalization and Production

A Large Ion Collider Experiment



ALPIDE finalization and production timeline

- Enineering Design Review: Oct 15
- Complete design of final ALPIDE: Jan 16
- Proto-run: Feb – May 16
- Production Readiness Review: July 16
- Series Production (~25 wafer/week): Sep 16 – Jul 17

Spare Material

ALPIDE (4) Design Finalization

A Large Ion Collider Experiment

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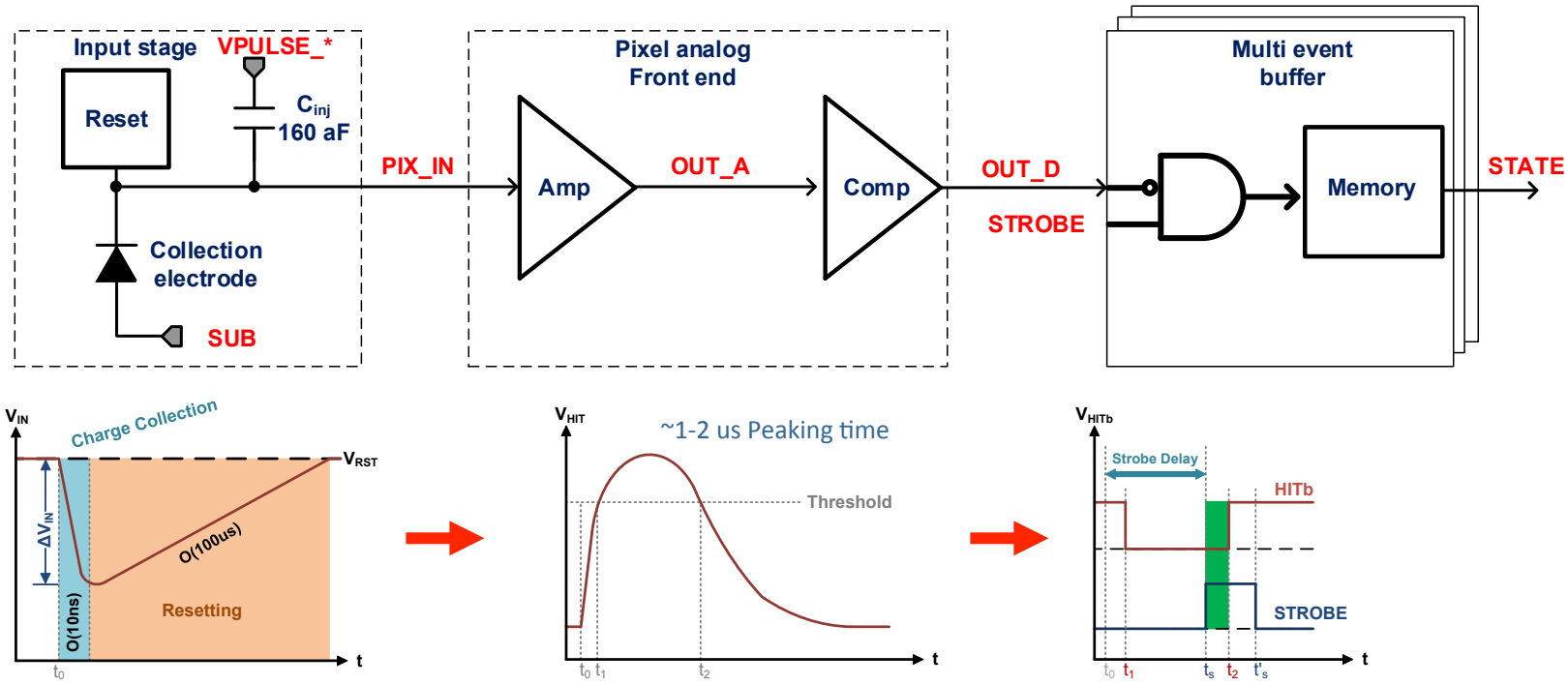
Main Design Activities (changes) wrt pALPIDE-3 (including EDR recommendations)

- Select **final pixel** (collection diode + front-end circuit)
- Improve detailed routing of pixel configuration control wires under Pads Over Circuits
- Improve handling of pixel configuration signals from periphery (EDR rec.)
  - Enable fast reload of pixel mask even during readout. Support active forcing of the mask bits from periphery
- Optimize distribution of global STROBING and PULSING signals from periphery (EDR recommendation)
  - Enable major speed-up of pixel tests with analogue scans and charge injeciton
  - Optimize supply current time profile (phase shift pulses in time) (EDR rec.)
- Power optimization of digital block (clock gating)
- Data Transmission Unit: power optimization
- MLVDS: experimental verification of new version with module power off protection
- I/O CMOS: re-simulation to evaluate signal integrity (EDR recommendation)
- POWER-ON RESET: triplication (together with global reset signals) (EDR recommendation)

ALPIDE Principle of Operation

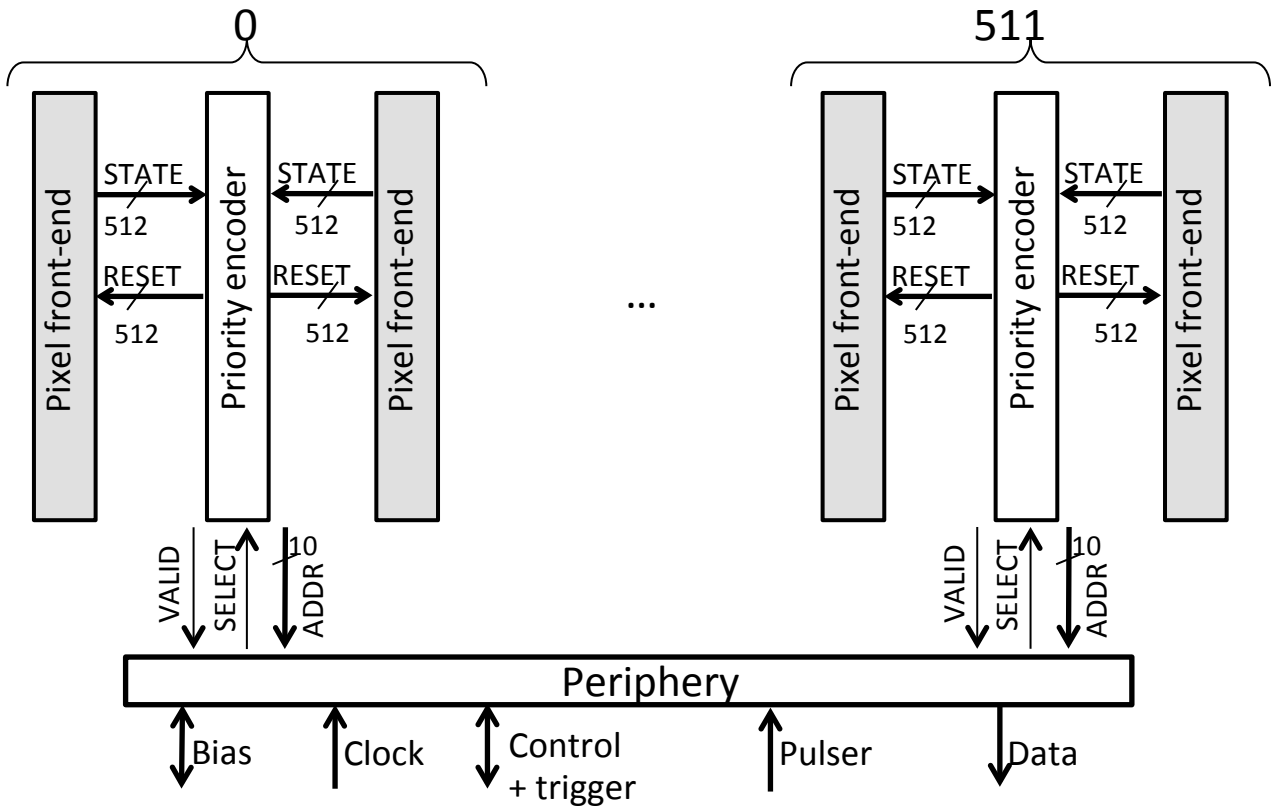


ultra low-power front-end circuit
40nW / pixel

Front-end acts as delay line

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with ~1-2μs peaking time
- Threshold is applied to form binary pulse
- Hit is latched into a (3-bit) memory if strobe is applied during binary pulse

ALPIDE Principle of Operation



Pixel Matrix - Hit driven architecture

low-power matrix readout ~ 2mW

- Priority encoder sequentially provides addresses of all hit pixels present in double column
- No activity if no hit (**no free running clock**) ➔ low power

Experimental Results

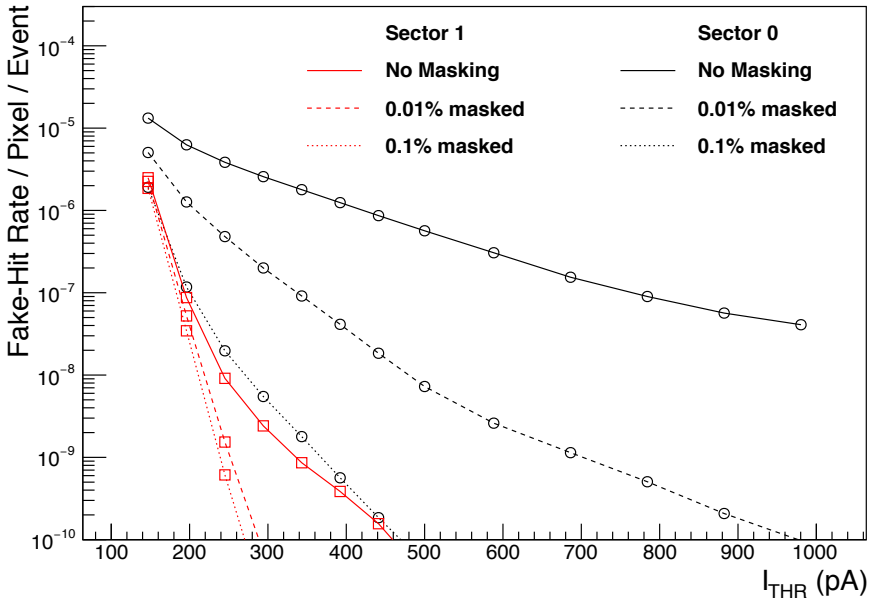
Fake-Hit Rate Measurements

- 120,000 (pseudo) random triggers
- No external signal
- Offline masking of 0.15% of the hottest pixels (20 per sector)
- Measurement reach / sensitivity limit

$$p_{\min} = \frac{1}{N_{Event} \cdot N_{Pixel}}$$

$$= 6.36 \cdot 10^{-11} \Big/ Pixel/Event$$

- Larger size input transistor (sector 1) reduces fake-hit rate significantly



8 chips, V_{SUB} = -3V, I_{THR} = 0.5nA, V_{CASN} = 0.95V

Experimental Results – pAlpide-2

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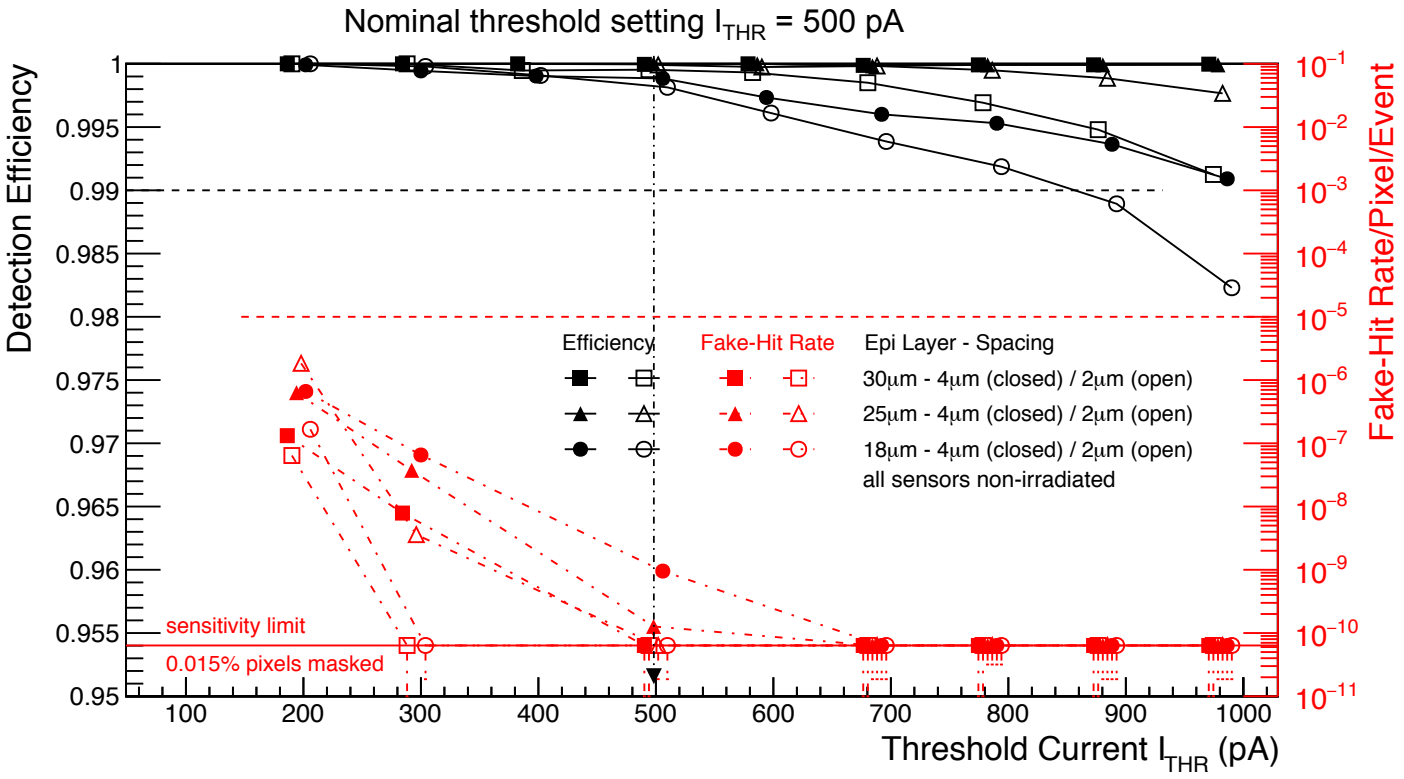
Efficiency and Fake Hit Rate

V_{BB}=-6V



Larger ¨spacing¨ shows better detection efficiency

- Results refer to chips with 30μm high-res epi layer, thinned to 50 μm

Experimental Results – pAlpide-3

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Single Event Upset - Results

- Cross-sections of data memories validated:

  $\sigma_{DP} \approx (4\text{-}8) \times 10^{-14}\ cm^2/bit$

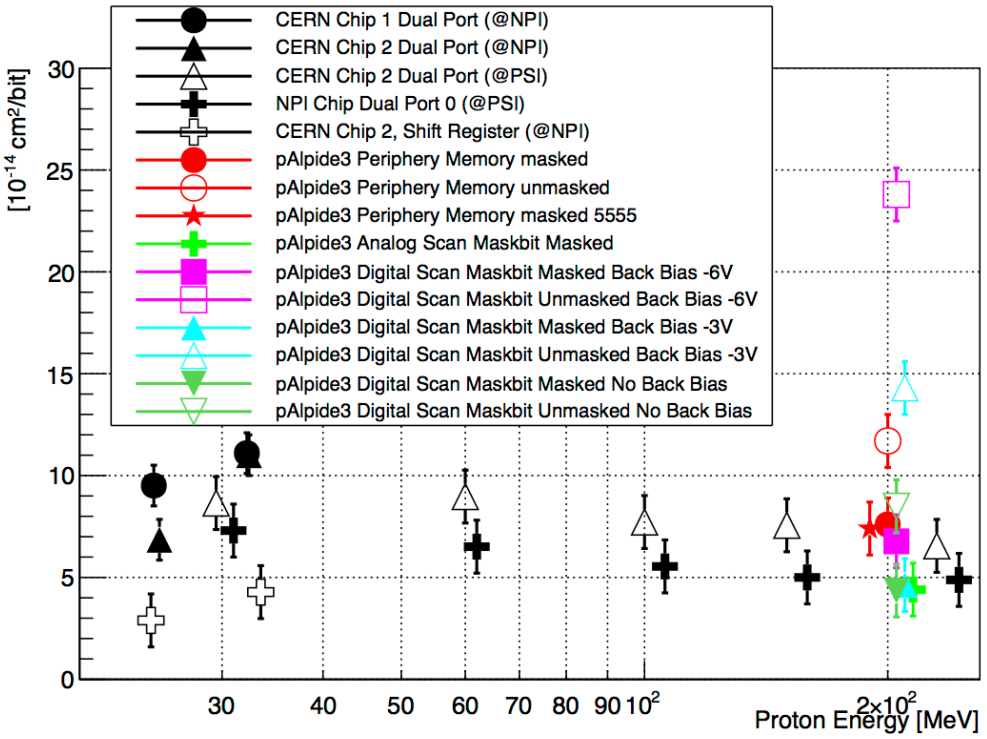
- Cross-section of mask register comparable to standard-cell version:

  $\sigma_{FF,0V} \approx (4\text{-}8) \times 10^{-14}\ cm^2/bit$

  (at 0V back-bias)

- Cross-section increases with back-bias.
  Upper limit:

  $\sigma_{FF,6V} < 2.5 \times 10^{-13}\ cm^2/bit$

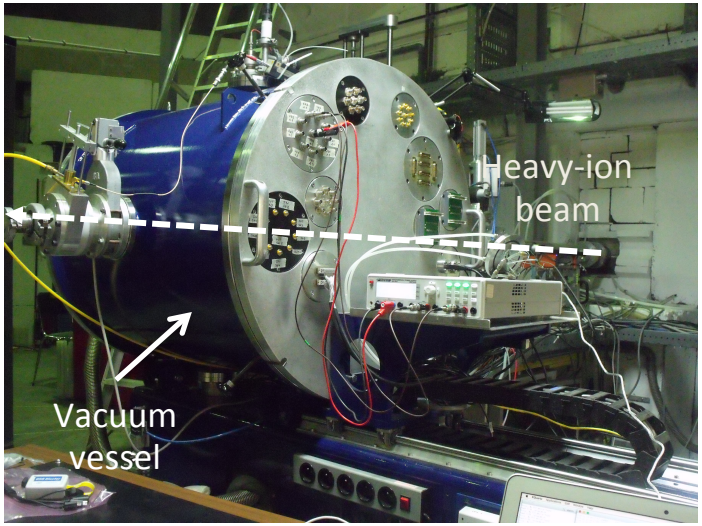


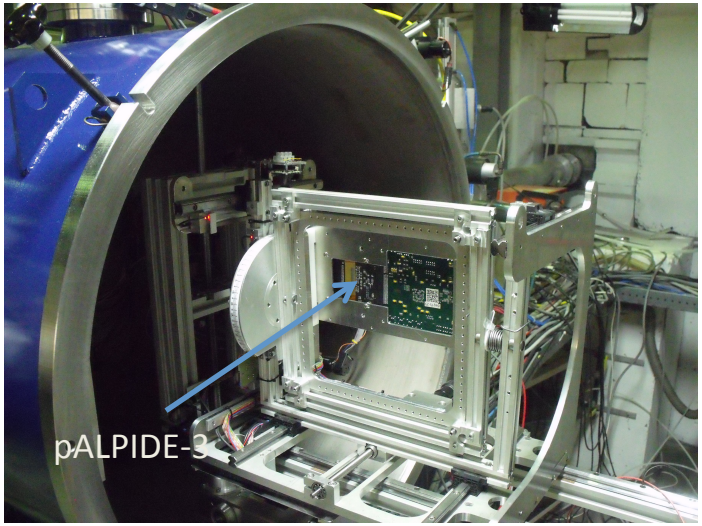
Experimental Results – pAlpide-3

ALICE

Single Event Latchup - Setup

- Heavy Ion Irradiation Facility (**HIF**) at Louvain-La-Neuve
- Particle flux: $10^4/cm^2/s$
- LETs: 10.0, 20.4, 32.5, and 62.5 MeV cm^2/mg
- First test: no back-bias



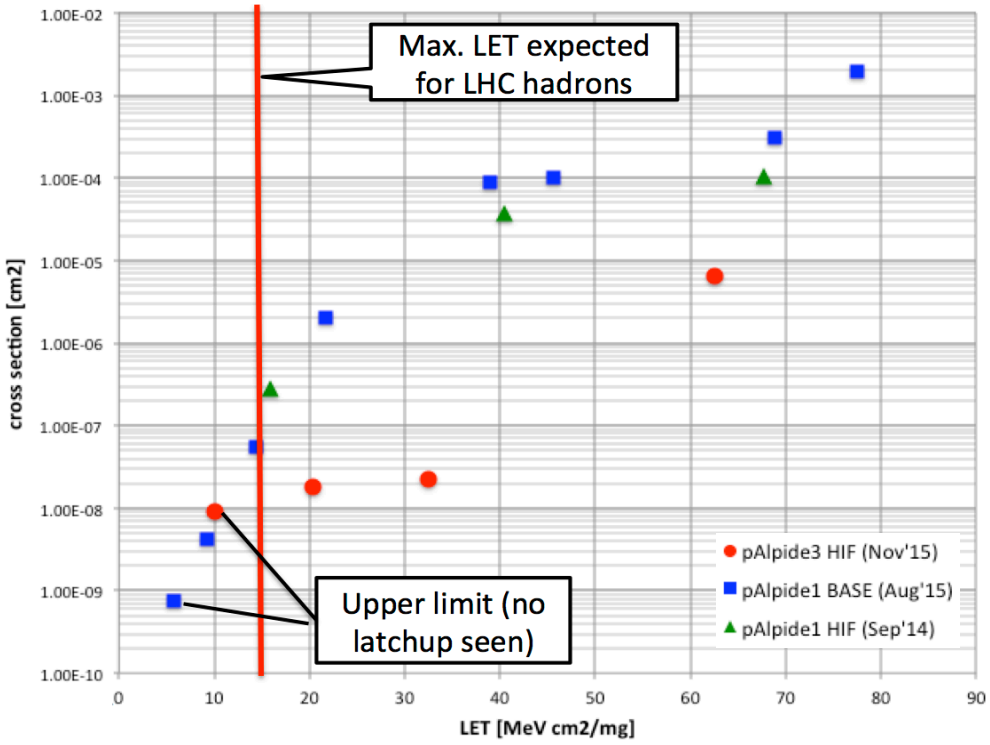


Experimental Results – pAlpide-3

ALICE

Single Event Latchup – Preliminary Results

- Analogue latch-up (present in pALPIDE-1) have disappeared as effect of the modifications implemented
- Cross-section reduced by 1-4 orders of magnitude



Experimental Results – pAlpide-3

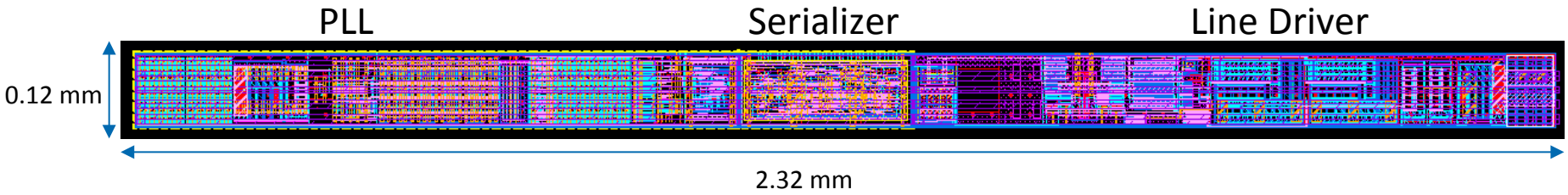
DTU – Data Transmission Unit (HSO)

DTU v2b

Implemented in **pALPIDE-3** (June 2015)

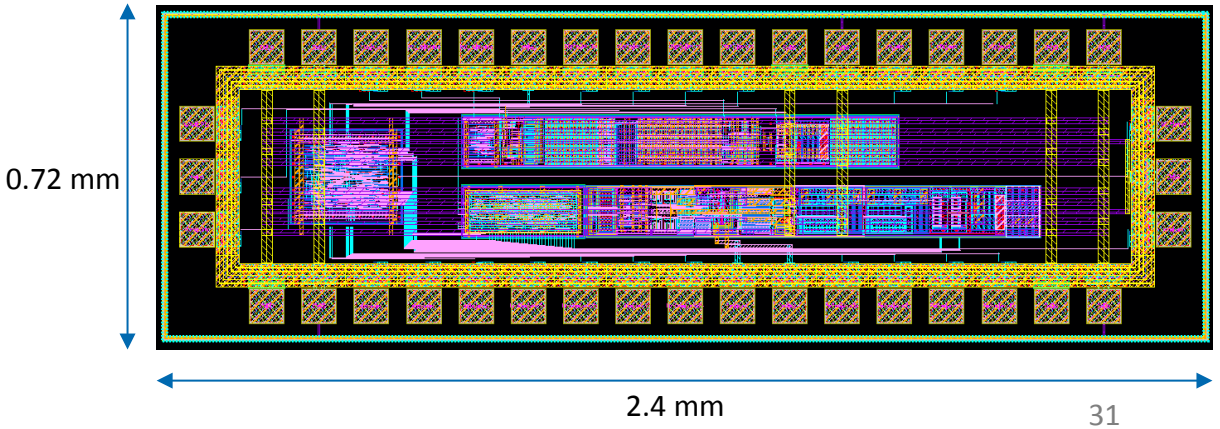
Layout 2.32 mm × 0.12 mm

Includes PLL + Serializer + Driver + Test Features



DTU v2b Test Chip

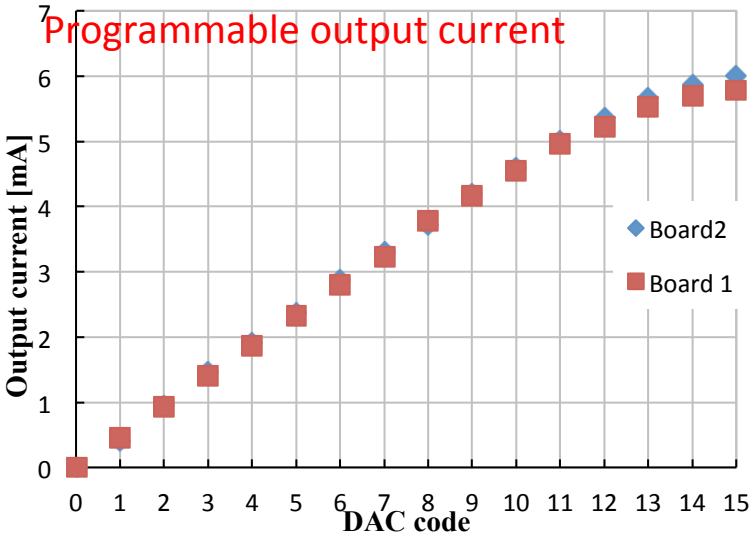
Submitted together with pALPIDE-3



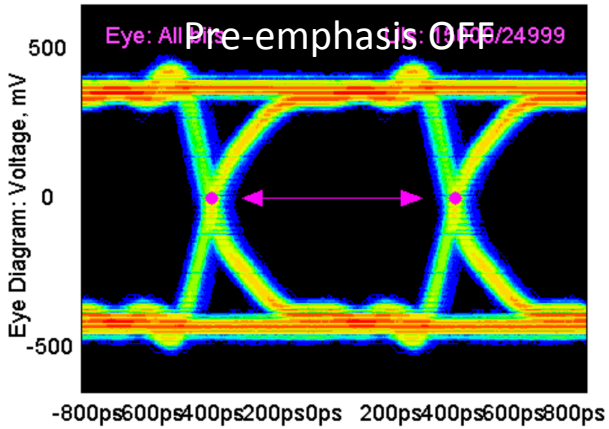
Experimental Results – pAlpide-3

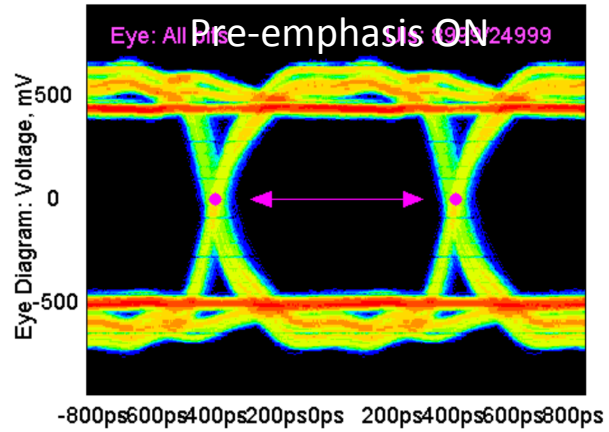
DTU – Laboratory characterization

- **Full DTU chain functional** (PLL+Serializer+Driver)
  - Test Chip Carrier + External clock source + Coax cables + Scope



Programmable Pre-Emphasis Current



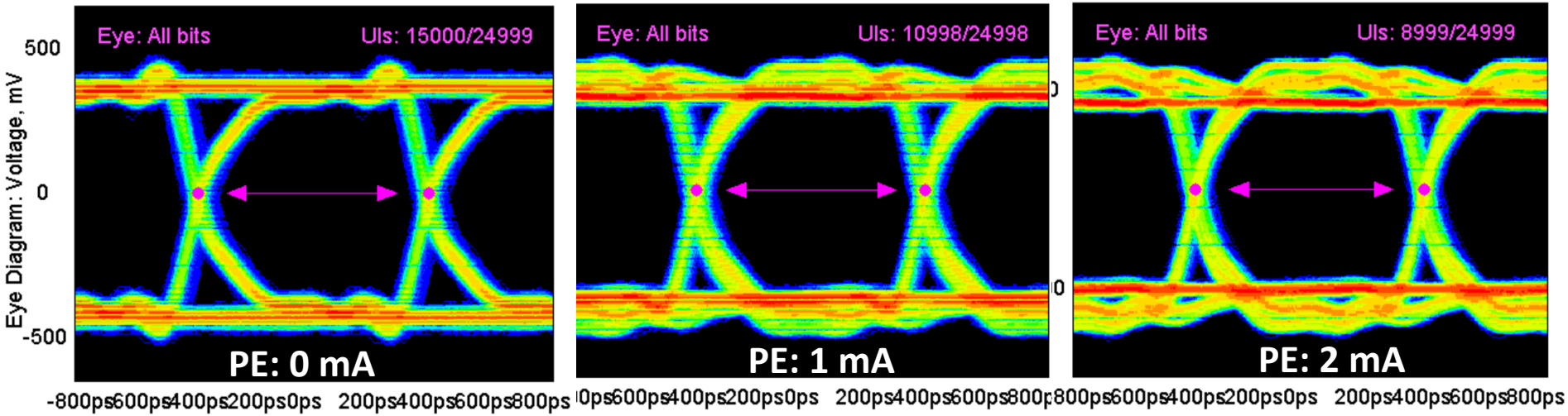


Experimental Results – pAlpide-3

ALICE

DTU – Laboratory characterization

Eye diagrams vs Pre-Emphasis



Bit rate: 1.25 Gb/s

Main driver current setting: 4 mA

Pre Emphasis	0 mA	1 mA	2 mA
Eye width	0.822 UI	0.826 UI	0.835 UI
Eye opening	0.738 UI	0.742 UI	0.716 UI
Random jitter	11.4 ps	10.9 ps	12.0 ps
Deterministic jitter	48.8 ps	52.8 ps	57.4 ps

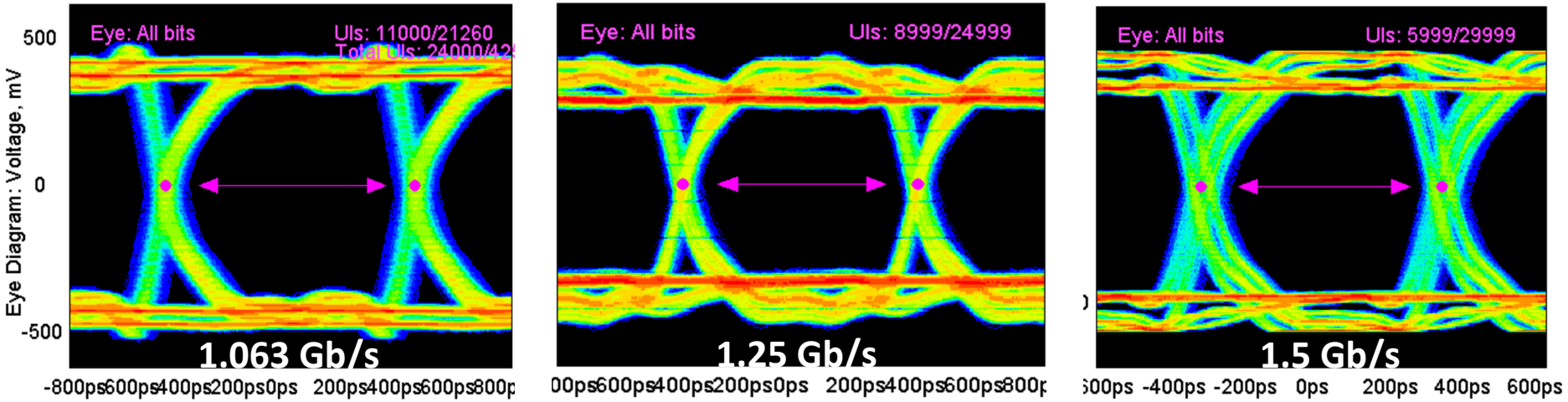
UI, Unit Interval: 1/1.25 Gbps = 0.8 ns

Experimental Results – pAlpide-3

ALICE

DTU – Laboratory characterization

Eye diagrams vs Bit Rate



Nominal (mid range) settings for main driver current and pre-emphasis current

	1.25 Gb/s	1.063 Gb/s	1.5 Gb/s
Eye width	0.835 UI	0.820 UI	0.779 UI
Eye opening	0.716 UI	0.713 UI	0.707 UI
Random jitter	12.0 ps	13.5 ps	8.0 ps
Deterministic jitter	57.4 ps	64.6 ps	82.6 ps