LHCb upgrade: status and milestones

G. Passaleva

On behalf of the LHCb collaboration

LHCC meeting December 1, 2015

Milestones

CALORIMETER	Front-End ASIC	EDR	May-15	24/04/2015
VELO	sensors	Sensor and thinned bump bonding EDR	Jun-15	01/06/2015
UPSTREAM TRACKER	SALT Chip	SALT EDR	Jun-15	22/06/2015
UPSTREAM TRACKER	FLEX cables	FLEX CABLE EDR	Jun-15	23/06/2015
UPSTREAM TRACKER	Staves	Stave EDR	Jun-15	19/06/2015
SCIFI	Fibres, mats, modules	Joint EDR	Jul-15	16/07/2015
UPSTREAM TRACKER	Sensor	SENSOR EDR	Jul-15	18/06/2015
UPSTREAM TRACKER	ELECTRONICS	PEPI/LV EDR	Jul-15	23/06/2015
VELO	electronics	ASIC EDR	Aug-15	29/06/2015
RICH	MaPMT	Place MaPMT order and start production	Nov-15	01/11/2015
VELO	cooling substrate	Cooling Substrate EDR	Nov-15	25/11/2015
MUON	nSYNC	EDR	Dec-15	24/11/2015
MUON	nODE	EDR	Dec-15	24/11/2015
MUON	nPDM	EDR	Dec-15	24/11/2015
MUON	nSB	EDR	Dec-15	24/11/2015
VELO	electronics	hybrid EDR	Dec-15	17/11/2015

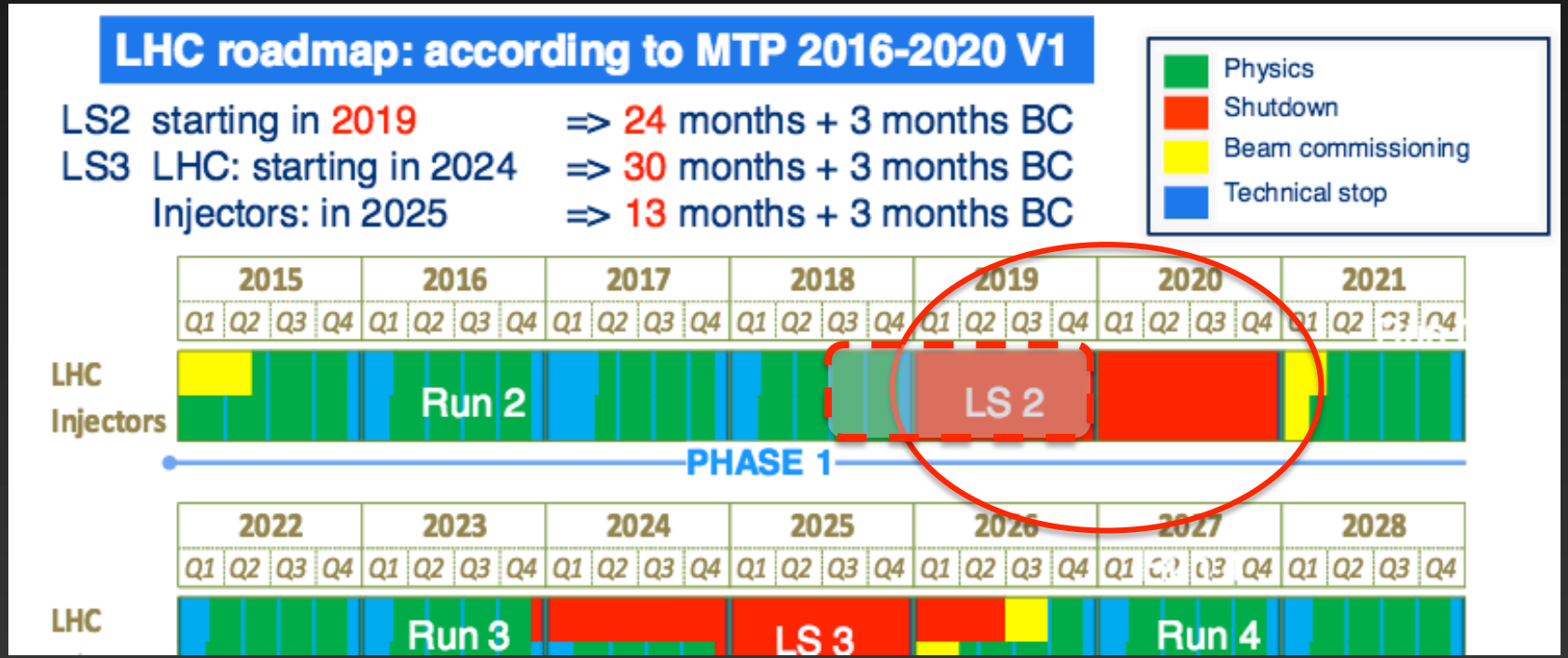
Several internal milestones also achieved

- A set of important EDRs took place since last meeting, will discuss some of them in this report

Milestone revision

As discussed at previous LHCC meetings, a revision of the milestones have been made. Two main drivers for this revision:

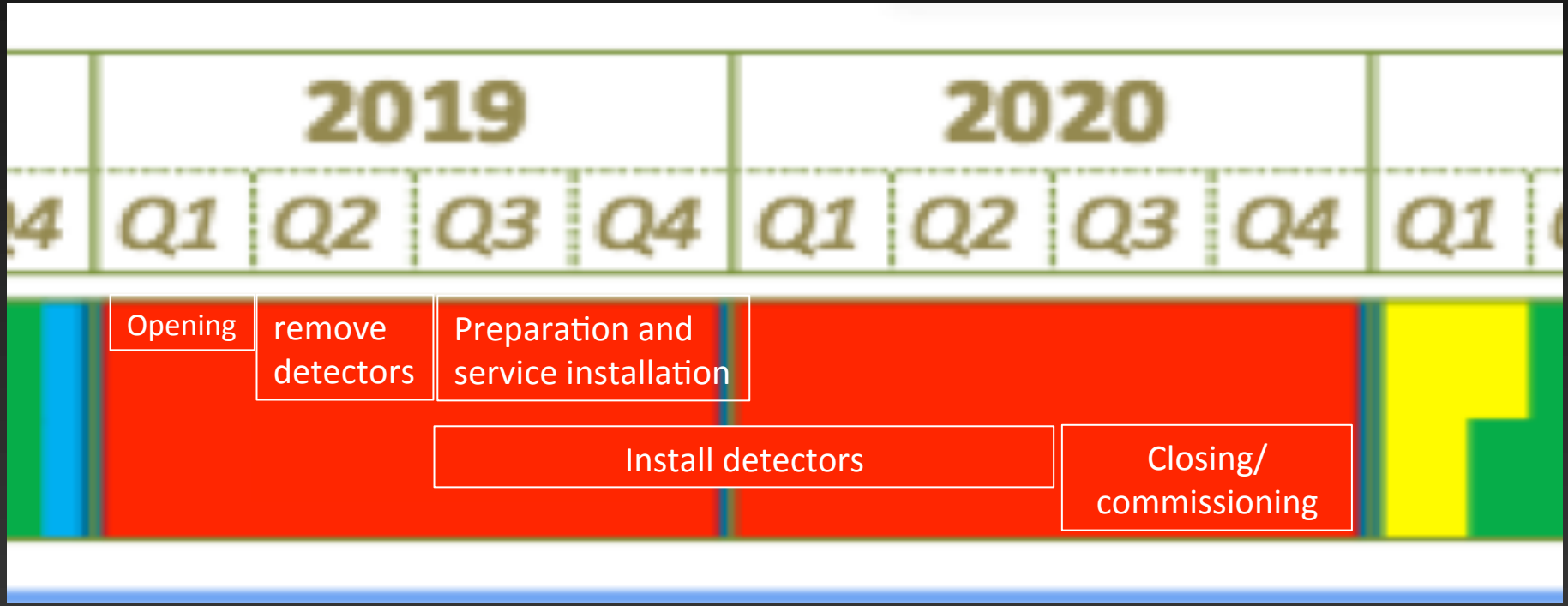
1. New LHC schedule



Milestone revision

Two main drivers for this revision:

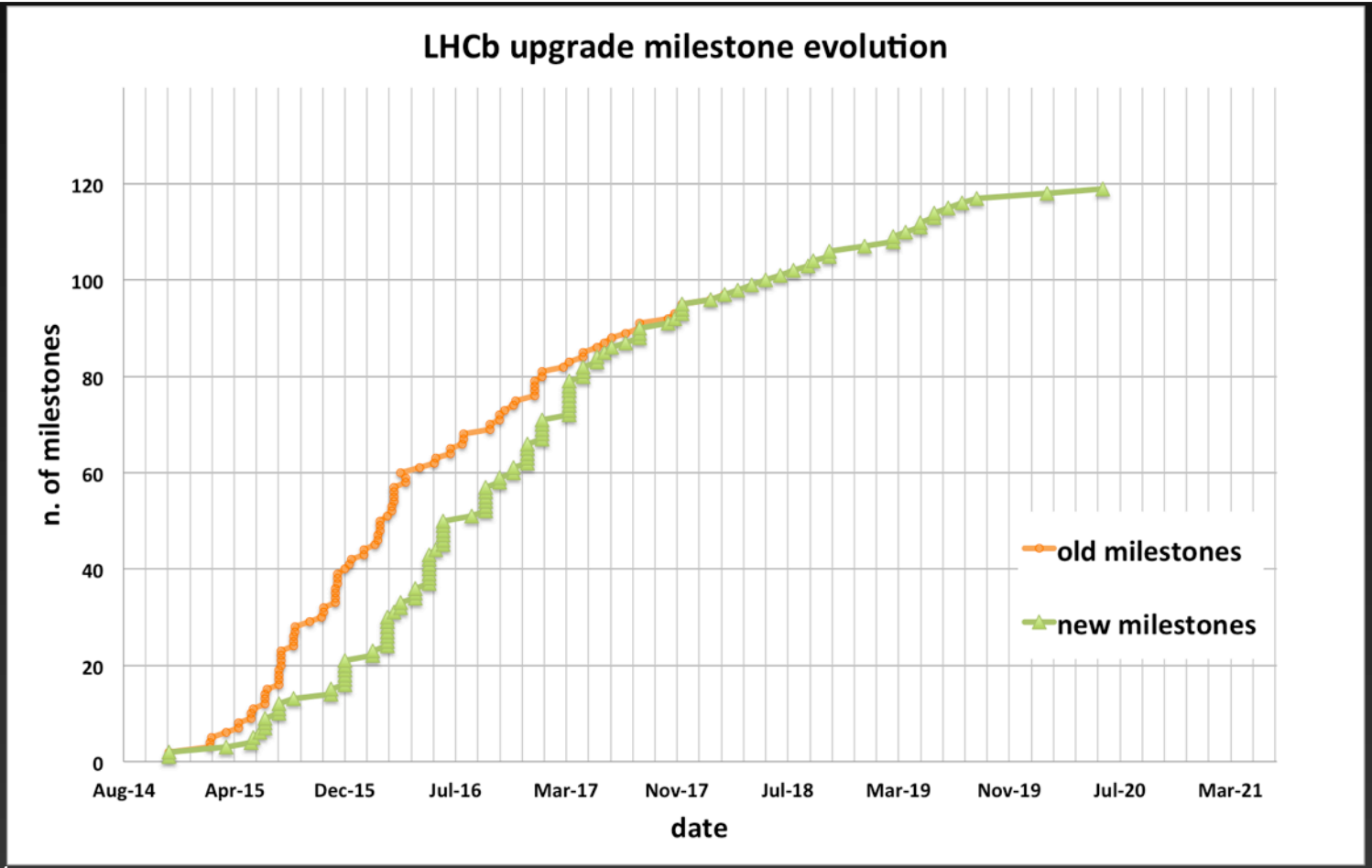
2. Preliminary installation schedule (R. Lindner, Technical Coordinator)



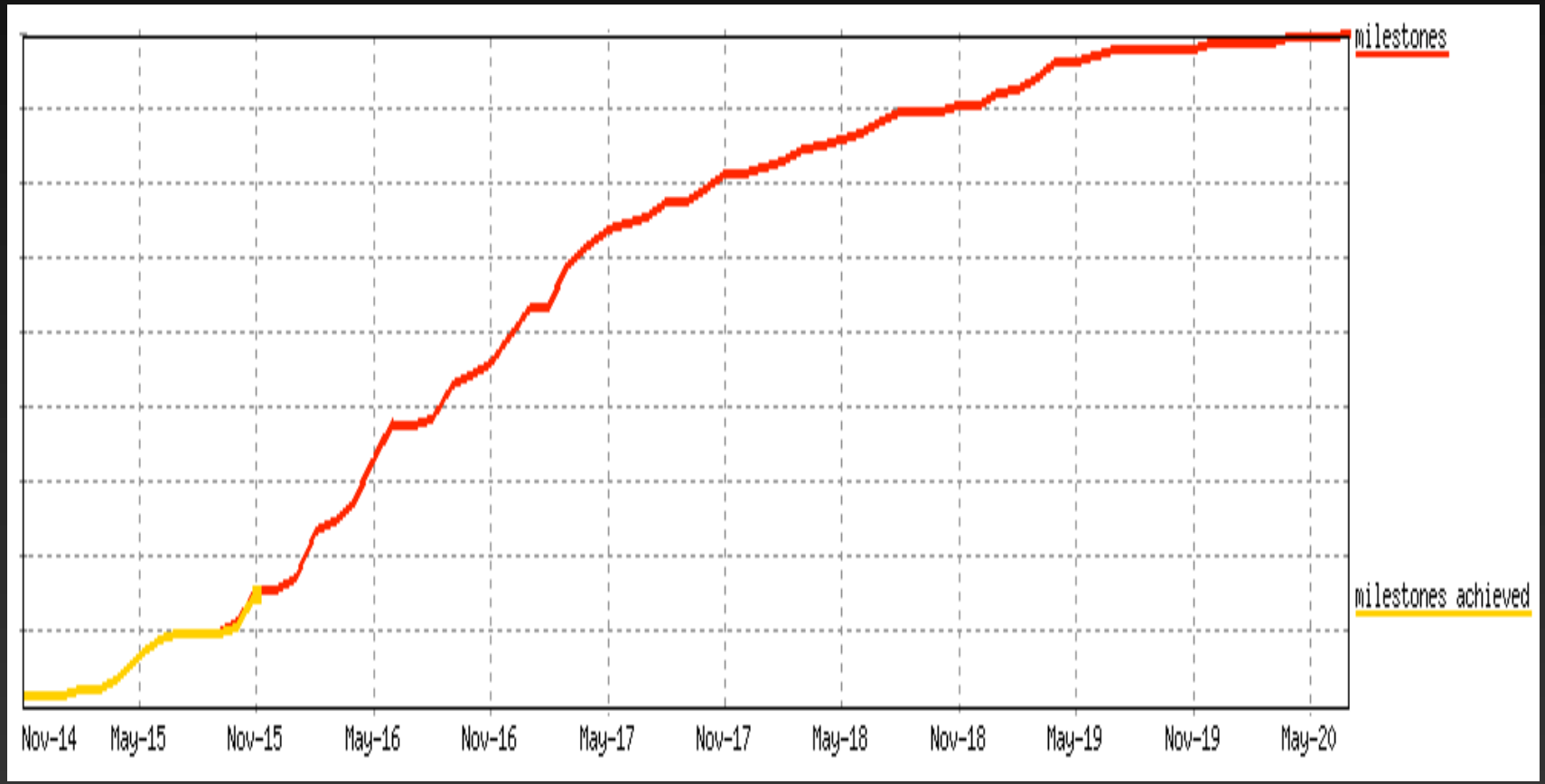
Milestone revision

- Modifications wrt previous schedule take into account:
  - ★ New LHC schdule (+1 year)
  - ★ Preliminary installation schedule by the technical coordinator
  - ★ Better and more realistic assessment of production schedule after the first round of EDRs → additional milestones!
- Milestones shifted generally by 3-7 months (reflecting the new LHC schedule)
- Globally the upgrade project fits well in the new LHC schedule

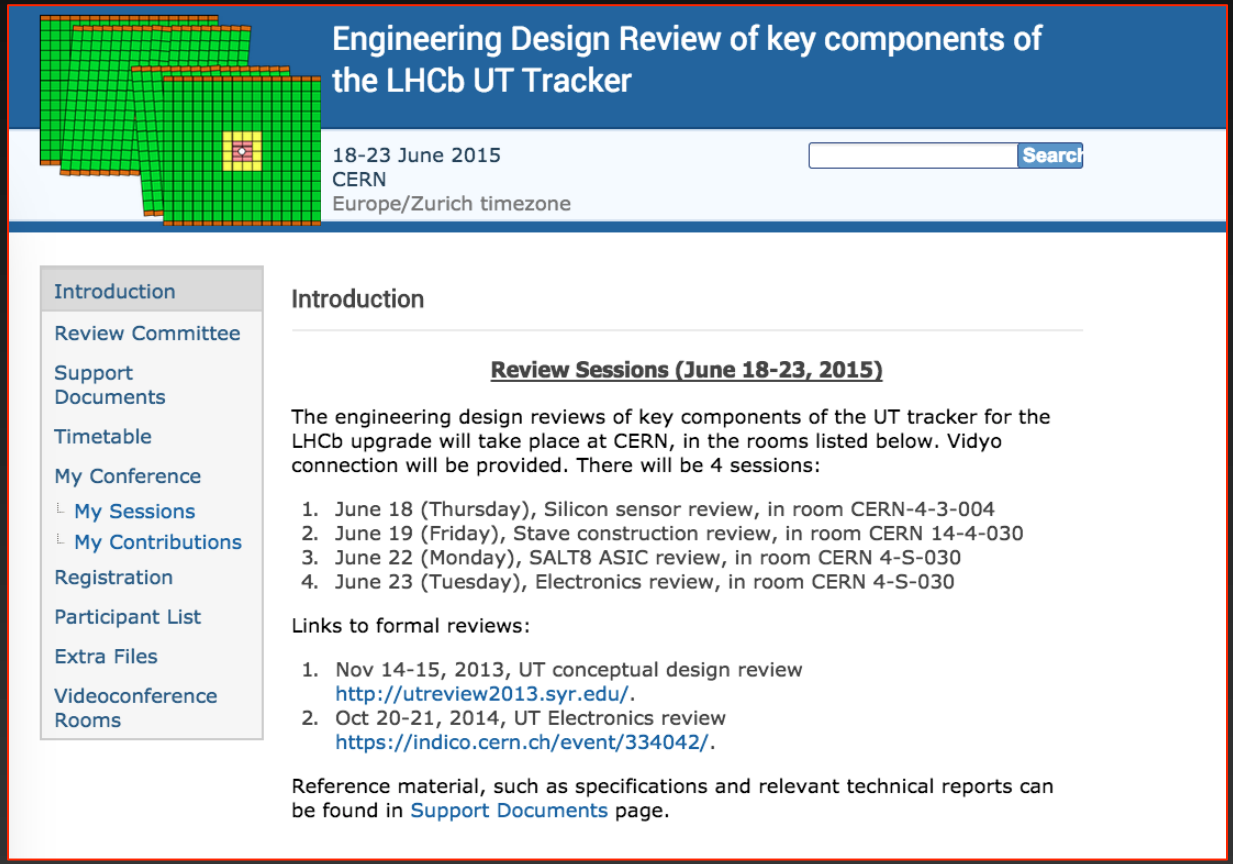
Milestone revision



Milestone status



Progress report: UT



Engineering Design Review of key components of the LHCb UT Tracker

18-23 June 2015
CERN
Europe/Zurich timezone

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Introduction

Review Sessions (June 18-23, 2015)

The engineering design reviews of key components of the UT tracker for the LHCb upgrade will take place at CERN, in the rooms listed below. Vidyo connection will be provided. There will be 4 sessions:

1. June 18 (Thursday), Silicon sensor review, in room CERN-4-3-004
2. June 19 (Friday), Stave construction review, in room CERN 14-4-030
3. June 22 (Monday), SALT8 ASIC review, in room CERN 4-S-030
4. June 23 (Tuesday), Electronics review, in room CERN 4-S-030

Links to formal reviews:

1. Nov 14-15, 2013, UT conceptual design review http://utreview2013.syr.edu/.
2. Oct 20-21, 2014, UT Electronics review https://indico.cern.ch/event/334042/.

Reference material, such as specifications and relevant technical reports can be found in Support Documents page.

Four EDRs in June:

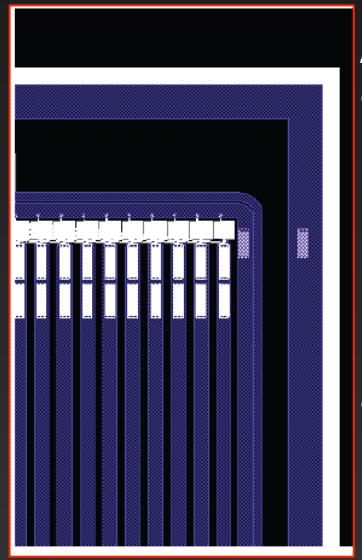
- Silicon sensors
- Staves
- SALT ASIC
- Electronics/FLEX cables

- Reports from the reviewers received
- Generally positive
- Main remarks and actions taken discussed in the following

Progress report: UT sensors

Remarks on:

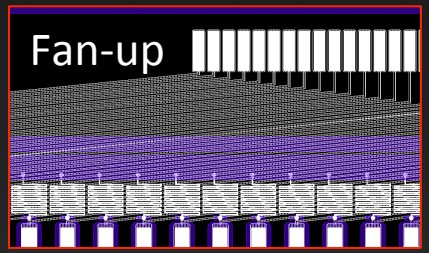
- top biasing: test long term stability and radiation effect
- embedded pitch adapter: test charge collection efficiency, cross-talk, radiation effects

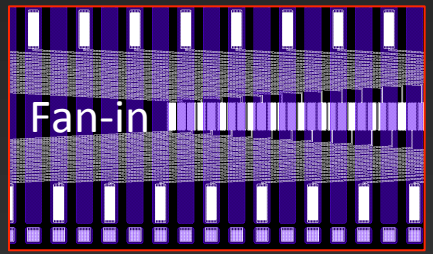


Top side bias

Actions:

- Irradiated sensors with top side biasing tested in July test beam; more data acquired in September and November.
- Back side biased sensors will also be irradiated for comparison





Embedded pitch-adapters

Actions:

- two designs tested
- Irradiated sensors with different configurations tested in July test-beam
- Charge collection lab tests with laser ongoing

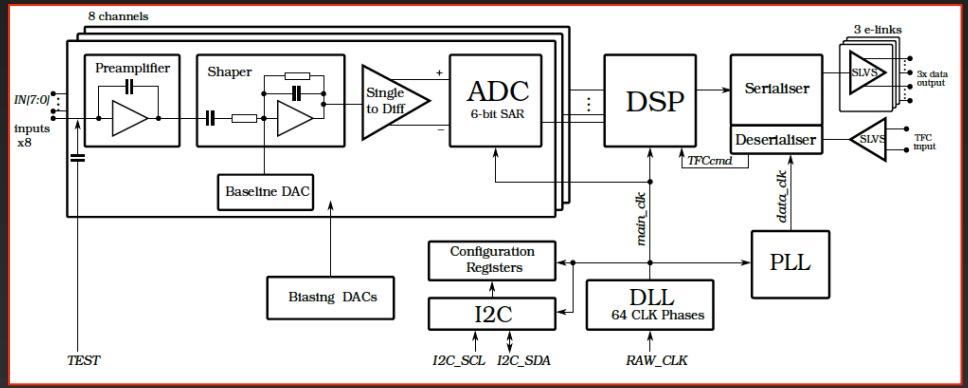
test-beams in September and November

PRR: Q1 2016

Progress report: UT SALT ASIC

- In depth review of SALT8 version by a team of TSMC technology experts (mainly from CERN)
- 9 chips submitted (full SALT8 plus building blocks: ADC, PLL, DLL, …)
- Many remarks, most of them will be incorporated in a second version of SALT8
- Tests of first version still ongoing, test infrastructure developed in parallel

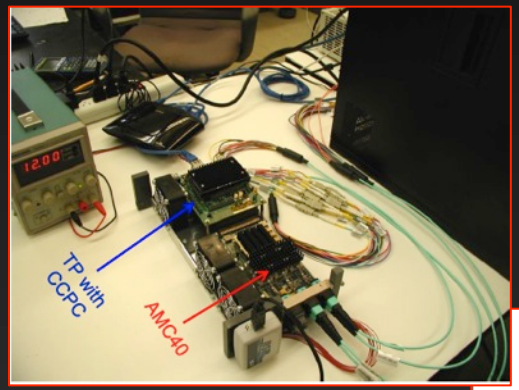
- Schedule:
  - ★ SALT8 V2 submission: end 2015 ✔
  - ★ First version of SALT128: spring 2016
  - ★ Engineering run: end 2016
  - ★ Production: Q2 2017



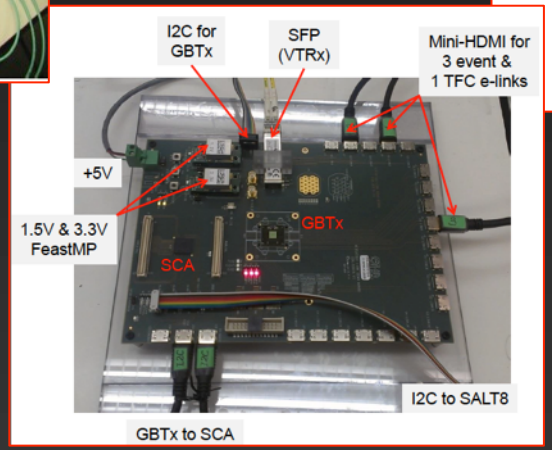
- Very aggressive/critical schedule. Test infrastructure crucial !

Progress report: UT SALT ASIC tests

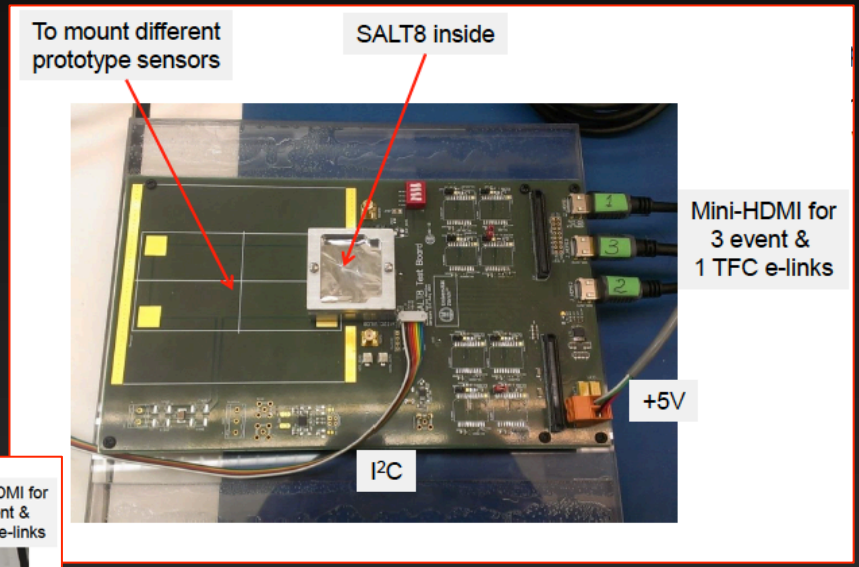
- Test setup of SALT chip is progressing
- Long learning curve and complex setup



MINI-DAQ board



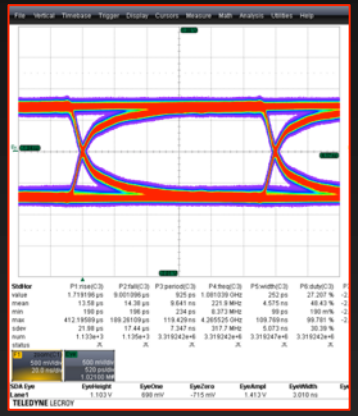
VLDB board (GBTX + optcal links)



SALT test board board

Progress report: UT FLEX cables, power distribution, staves

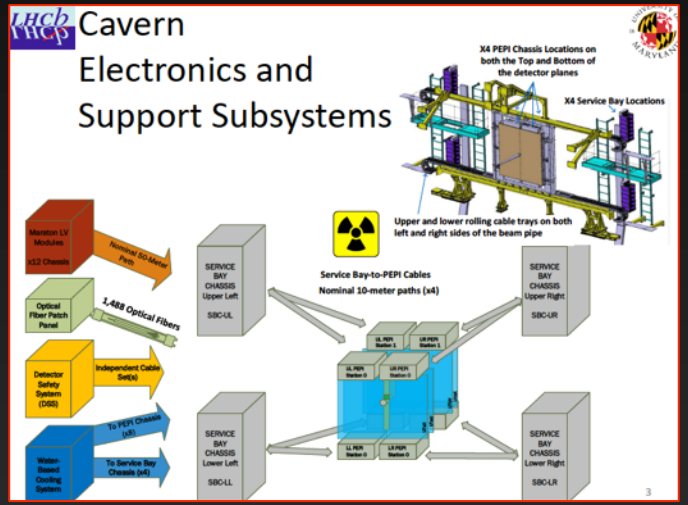
FELX cables



First batch of cables tested in Milano, Syracuse and Maryland. Test results positive. Remarks by reviewers already implemented in a new versions made at CERN and now under test
Another manufacturer identified in USA

PRR: Q3 2016

Power distribution



Very complex layout. Constraints come from the amount of material in the sensitive area.
Concerns were raised about CM noise due to grounding and coupling of conducting planes
Action: An accurate test setup is already in place in Maryland and all the aspects of the layout are being extensively tested

PRR: Q2 2017

Staves

Design well advanced also concerning the integration with the supporting infrastructure

Construction will start soon !

Reviewers recommended extensive thermal and mechanical stress tests during the various phases of the construction.

Action: final design incorporates rev. suggestions;
construction procedure will incorporate some of the proposed checks

Progress report: VELO

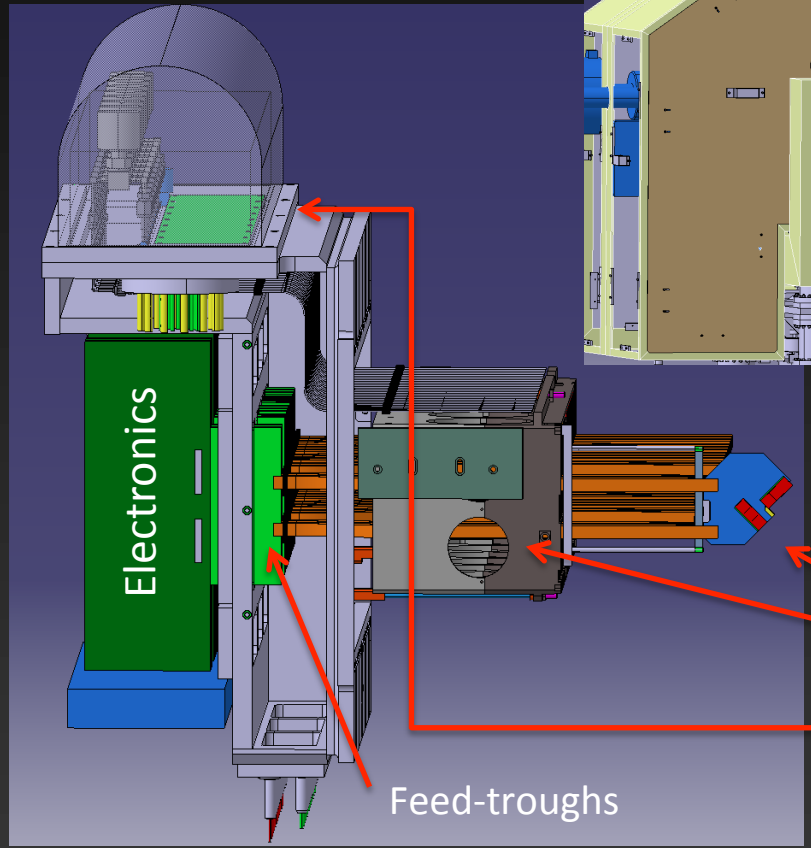
Four EDRs since June

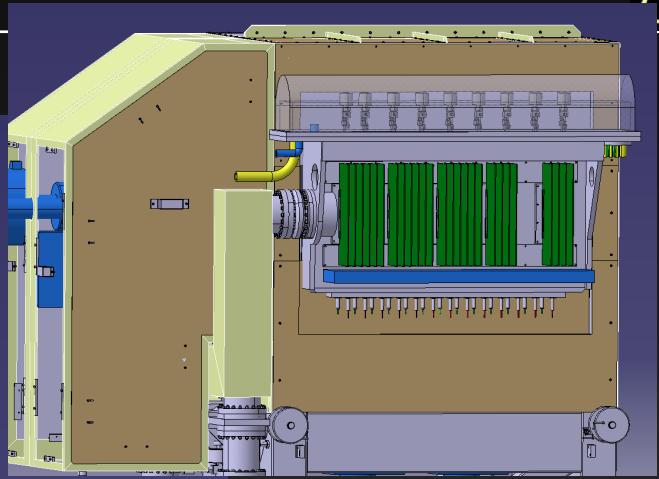
- Sensors
- VELOPIX ASIC
- Hybrid and electronics
- Microchannel cooling

Mechanics workshop

- All aspects of VELO mechanics reviewed

EDR: end 2016





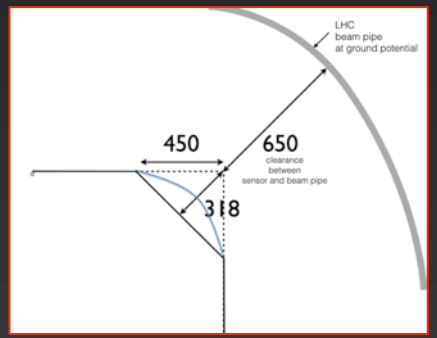
VELO mechanics
Above: the hood with electronics and services
Left: detail of:
modules,
base
Feed-throughs
tertiary vacuum for safety valves

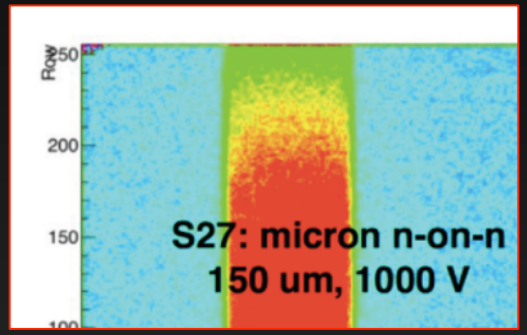
Progress report: VELO sensors

- Main remarks concerning: use of parylene coating for HPK p-on-n sensors which prevents bias at 1000 V on non uniformly irradiated sensors; hot spots on Micron sensors; rounded corners. Recommendations were made on the final design (thickness, pixel size etc.)

- Intense test beam activity to face the open problems
- A pre-series with rounded corners is in preparation

PRR: Q2 2016





sensor T6 Irradiated at KIT HPK parylene Coated
sensor T21 Irradiated at KIT MicronN-on-N
sensor T2 Irradiated at KIT HPK parylene Coated
sensor S4 Irradiated at KIT HPK parylene Coated
sensor S22 Irradiated at JSI annealed
sensor S27 Irradiated at JSI N-on-N Micron Annealed
sensor S8 NonIrrad HPK35um
sensor S25 NonIrrad Micron
sensor S11 NonIrrad 39um
sensor S30 NonIrrad N on N Micron GR 450
sensor S16 Irradiated at KIT HPK3 5um
sensor S34 Before Irrad NonN Micron GR 250
sensor T1 Irradiated at KIT HPK
sensor S23 Irradiated at JSI N On P Micron
sensor S6 Irradiated at JSI Coated HPK 39um
sensor S24 Irradiated at JSI N On P Micron

Assemblies tested in July

Progress report: VELOPIX

Pixel size	55 µm x 55 µm
Pixel matrix	256x256
Chip size	14 mm x ~16 mm [note 1]
Input charge	Optimized for e- (h+ if possible)
Input coupling	DC
Leakage current compensation	20 nA per pixel [notes 2-4]
Input referred noise (ENC)	σ < 100 e- (Cdet < 50 fF, planar silicon)
Minimum threshold, full chip	<800 e-
Threshold spread after equalisation	σ < 30 e-
Timewalk	< 25 ns for 1 ke-
Time over Threshold	No, binary readout, ToT only for monitoring [note 5]
ToT: pixel to pixel spread	< 5 %
Average max. hit rate	> 590 (880) MHits/s [note 6]
Allowed hit loss at max. rate	< 1% [note 7]
Technology	130 nm CMOS
System clock frequency	40 MHz
Output data format	Data-driven, zero-suppressed, grouping of hits to reduce bandwidth (superpixel concept)
Data output	At least 4 GWT links [note 8]

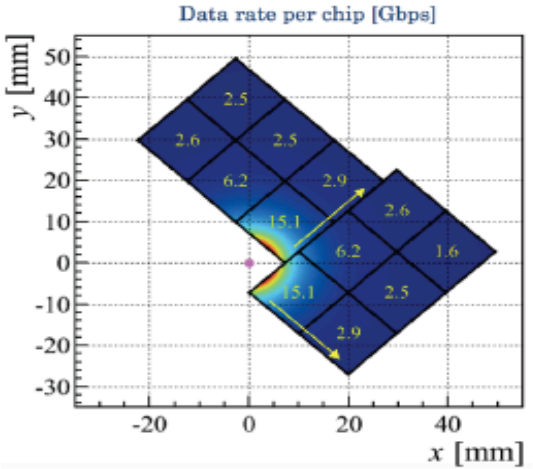
Operational temperature range	-40 °C to + 60°C
Startup temperature range	-60 °C to + 60°C [note 9]
Power consumption	< 3W/ full chip
Radiation hardness	> 400 MRad [note 10]
SEU protection	yes [note 11]
Timing and fast control (TFC)	See note 12
Slow control	Compatible with LHCb ECS: e.g. SPI over GBT [note 13]
Monitoring	Voltage, temperature
Pixel status counters	see note 14
Front-end disable	yes (shutter-like mode), see TFC
Fast (data) reset / clear buffers	yes
Bump pad window diameter	12 µm, like Timepix3
IO signal levels	SLVS
Global (trigger) OR	Yes
Calibration	Internal and/or external testpulse (1-2 ns time resolution), internal delay in case of external TP.
Power on reset (pin)	Yes

VeloPix Specifications

- Floorplan
- High speed output circuit
- ECS/TFC
- analog front end
- digital architecture

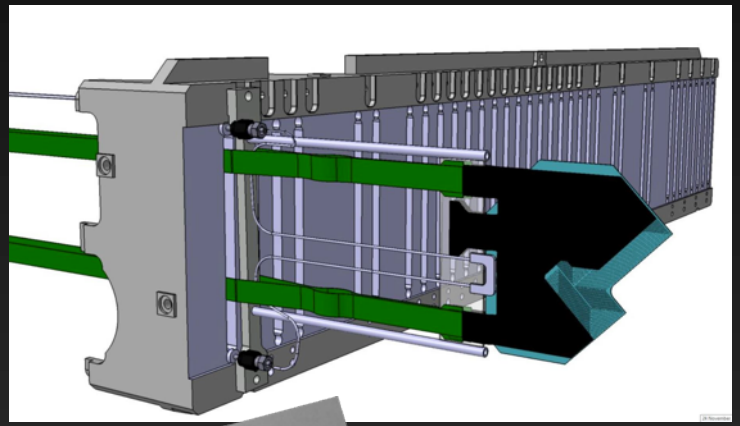
End of 2015

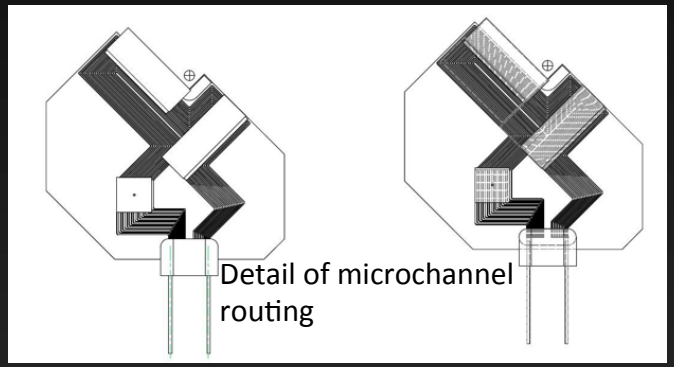
All elements put in place to launch
a summer of verification before first submission



Progress report: Microchannel cooling EDR

400 µm thick silicon substrate; 200x120 um^2 channels; CO_2 pressure ~20 bar

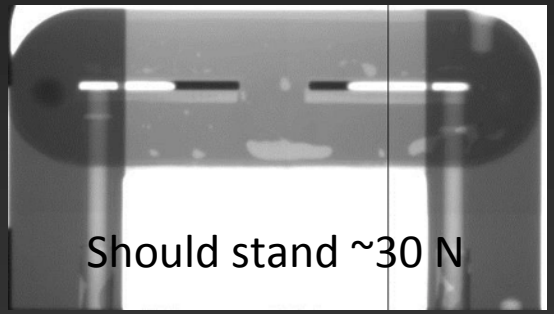


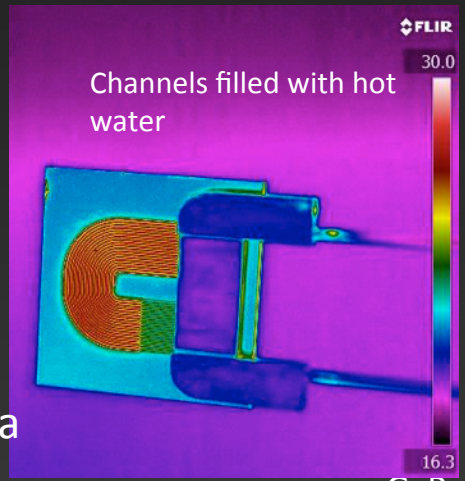


Many challnging issues

Safety is a paramount priority

Some concerns on the connector design and mounting procedure





Tender to be launched in Q1 2016

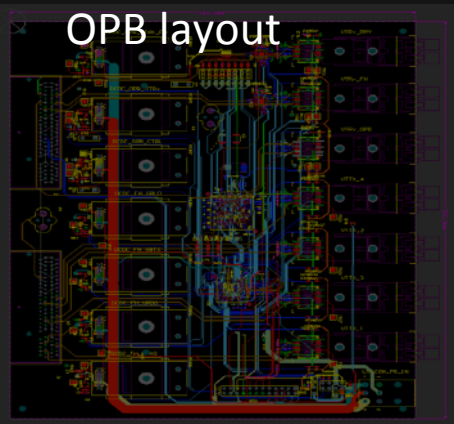
Connector in visible light; X-ray ; IR camera

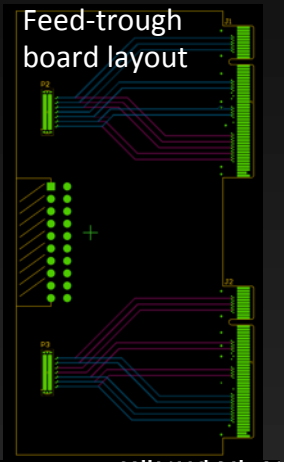
Velo electronics

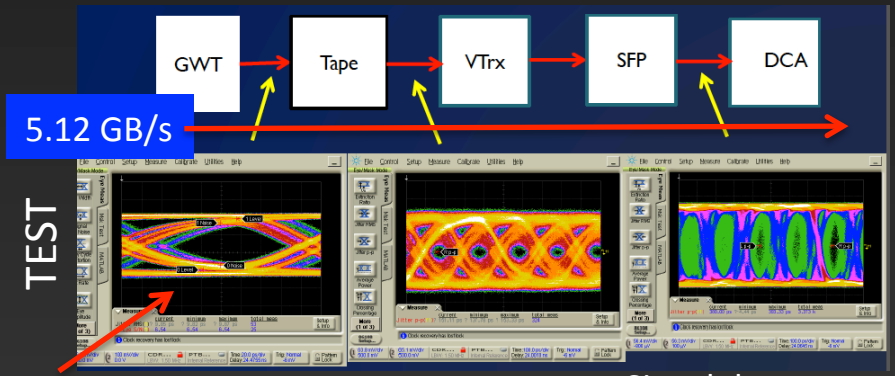
Key blocks of the electroncis chain were reviewed

- Opto-power board (OPB) & Feedthrough boards.
- Velopix hybrid.
- Flex tapes (data & control).

No major problems were spotted by the reviewers but high speed data transmission is challenging !

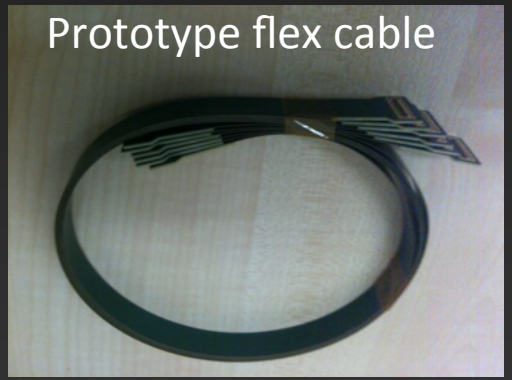


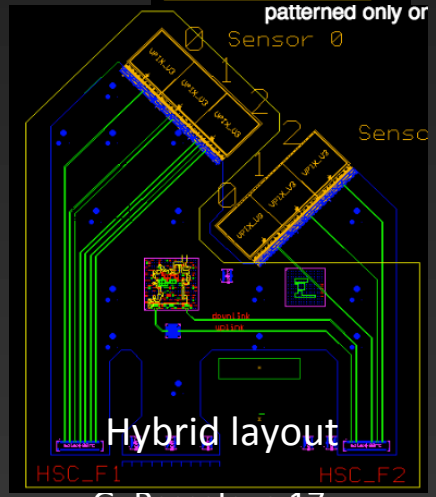




GWT signal (with known jitter problem)

Signal downstream the optical fiber

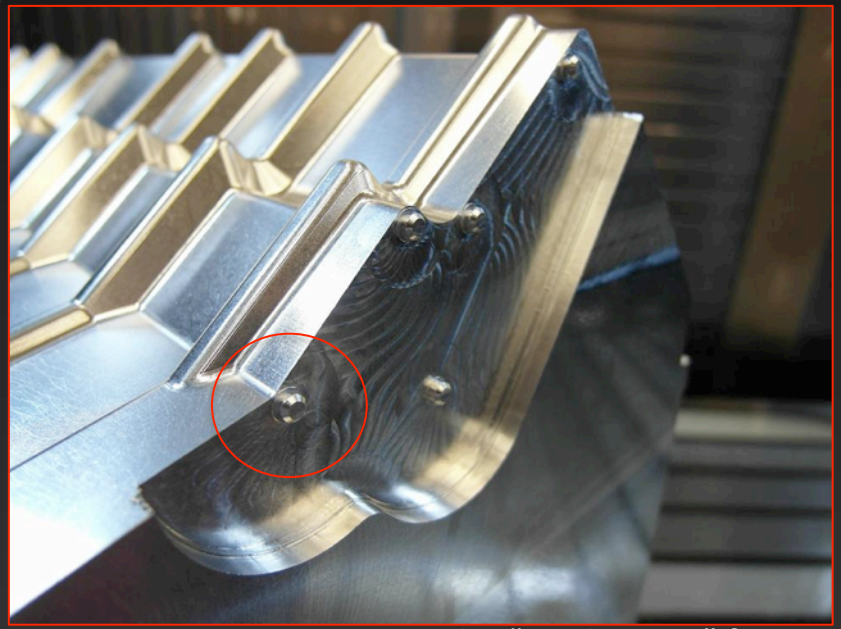




Velo RF foil

- No showstopper seen so far, but several warnings; structure of the box (when closed) gives a Im(Zeff/n) ~4.7 mOhm (while full LHC is 90 mOhm). This can contribute to longitudinal instabilities. However, the small beta* at the VELO mitigates the effect. New measurements indicate that instabilities are well understood under control. No major problems even at HL-LHC intensities

- First half-sized prototype at Nikhef finished
- Machined from a full Al block ~500x300x300 mm^3
  - nominal thickness: 500 micron
  - deviations from nominal geometry <100 um
- Leak tight
- half-size box 0.25 mm (ongoing)
- full-size box 0.5 mm (expected Q2 2016)
- full-size box 0.25 mm (expected Q3 2016)



1/2 size 0.5 mm prototype. Notice the “mushrooms” for WF suppressors connection

Progress report: RICH

First EDRs (CLARO ASIC + elementary cell) one year ago

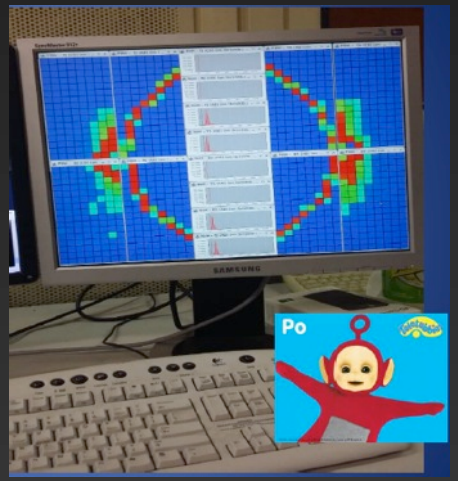
- ☞ A complete set of tests of the integrated photon detector module structure was felt mandatory before going to the PRRs
- ☞ a second version of the CLARO ASIC (CLARO8 v2) was designed incorporating the remarks made at the EDR

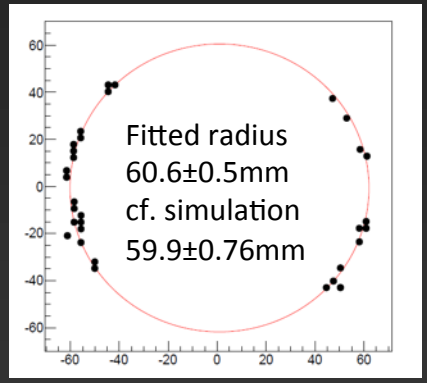
- Crucial test beams this summer before the PRRs. Tested 2 prototype photon detection modules each with 2 ECs mounted on the cooling bar; CLARO8 v2; digital board prototype

- Design of photon detector assembly for RICH2 almost finalised
- RICH1 mechanics progressing and converging towards final design. Will inherit as much as possible from RICH2

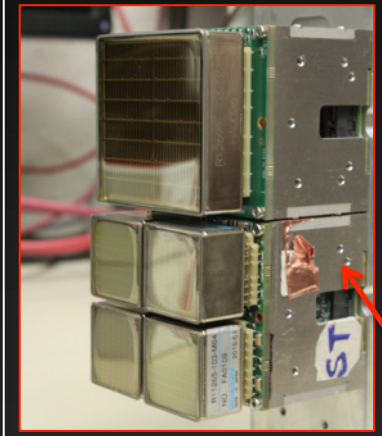
- MaPMT tender finalised. Order placed Nov 2015

Test beam setup





Progress report: RICH elementary cell, mechanics

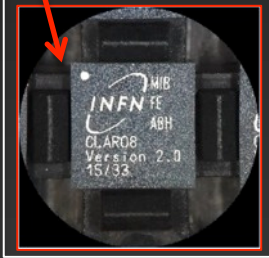


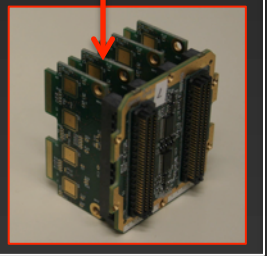
PRRs: Q1 2016

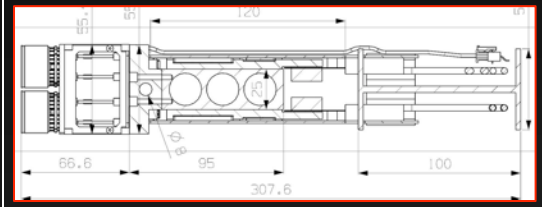
Elementary cells at the boundary between small and large PMTs

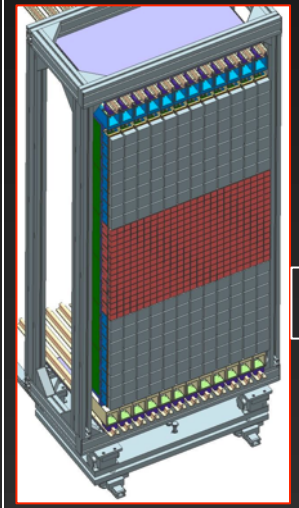
Packaged CLARO8 v2

FE boards+back-board









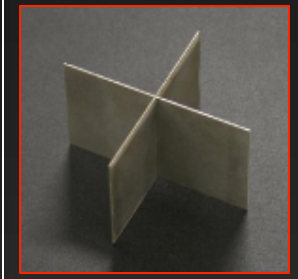
Photon detector module

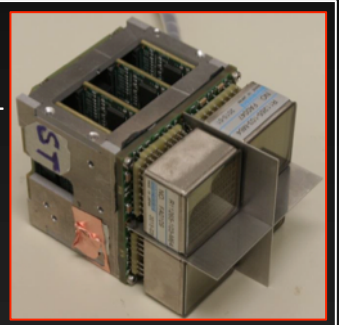
Photon detector assembly (RICH2)

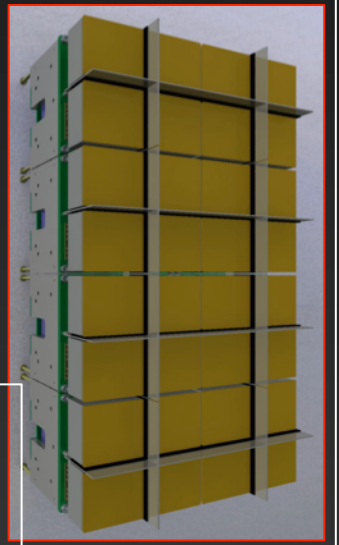
EDR: Q2 2016

Carbon fiber flat mirror prototype for RICH1

Magnetic shielding concept with cross-shaped mu-metal screens







RICH1-2 mechanics EDRs: Q1 2016

Progress report: Calorimeter

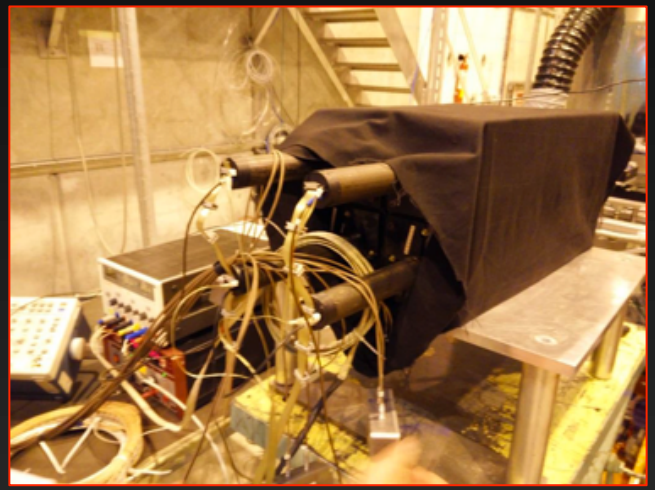
EDR of ICECAL in April 2015

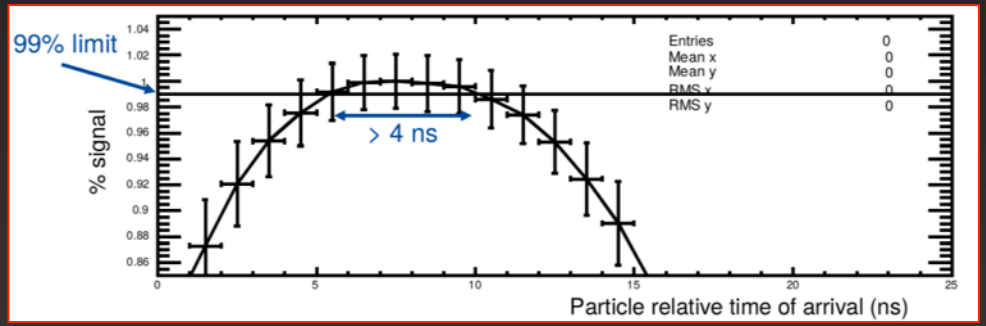
Suggestions and remarks from the reviewers implemented in ICECAL v3

ICECAL v3 and prototype Front-End Board tested on beam in September with a fully equipped Calorimeter module.
Results positive

Signal integration plateau of +-4 ns as desired

Readout electronics EDRs: Q3 2016

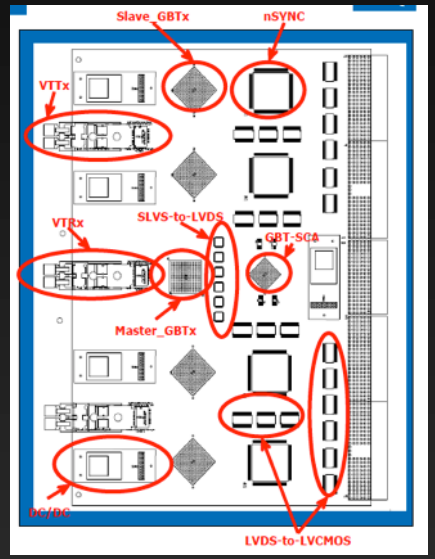




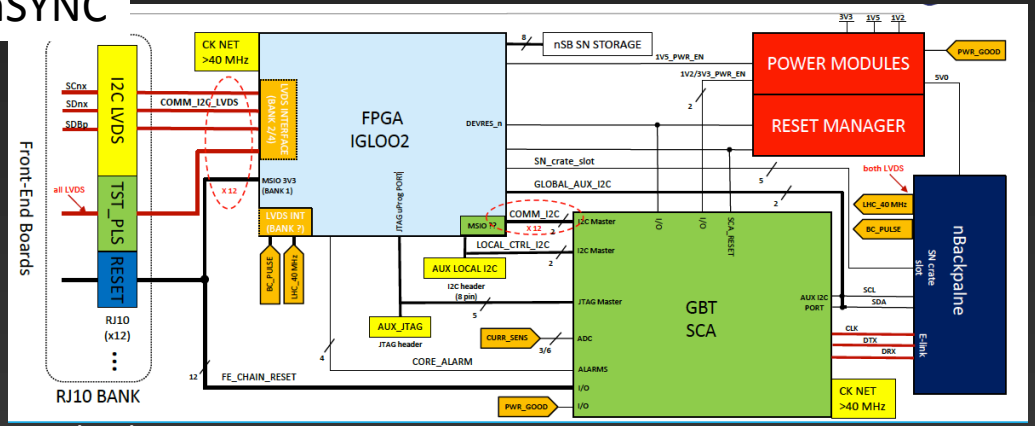
Progress report: Muon electronics EDR

- Full review of the new electronics
- Key elements:
  - ★ New TDC chip (nSYNC)
  - ★ New data transmission board (nODE board)
  - ★ New control/configuration boards (nPDM, nSB)
- *" The design of all four items of hardware is well advanced and there are no apparent technical 'show-stoppers' "*

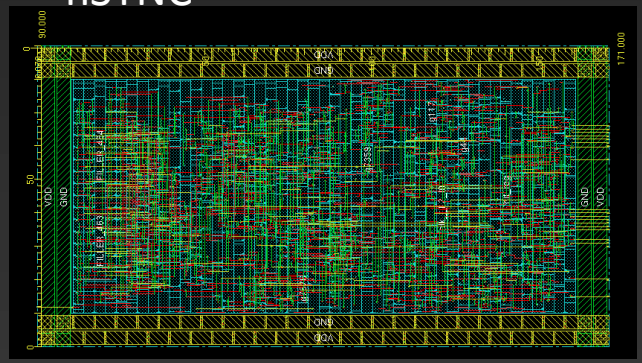
nODE



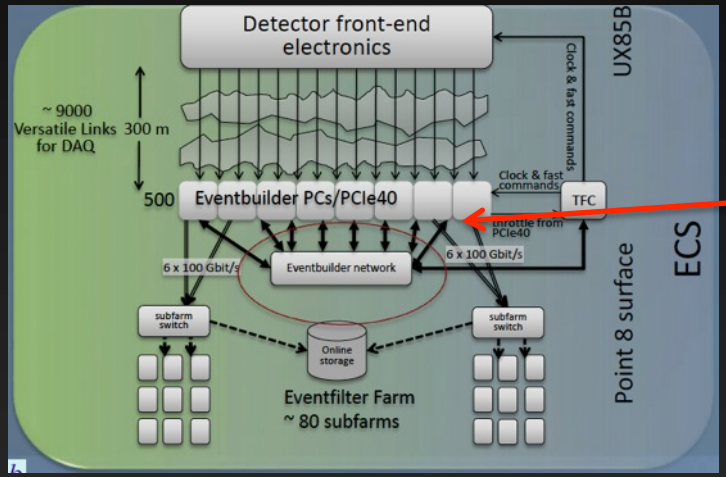
nSYNC

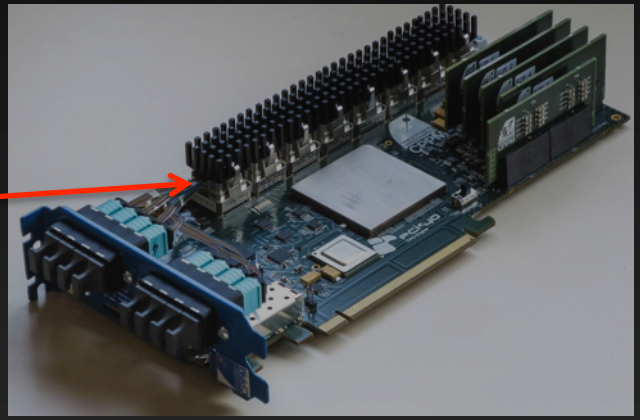


nSYNC



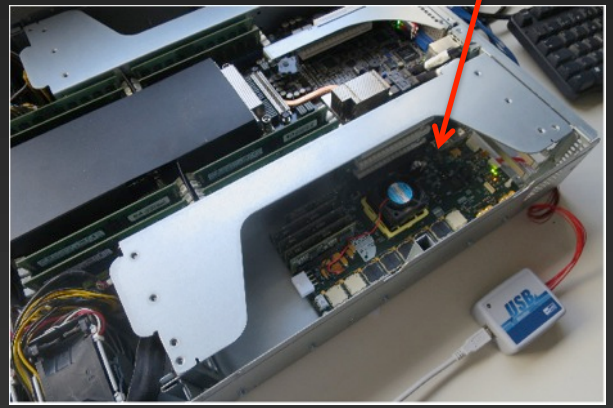
Progress report: ONLINE



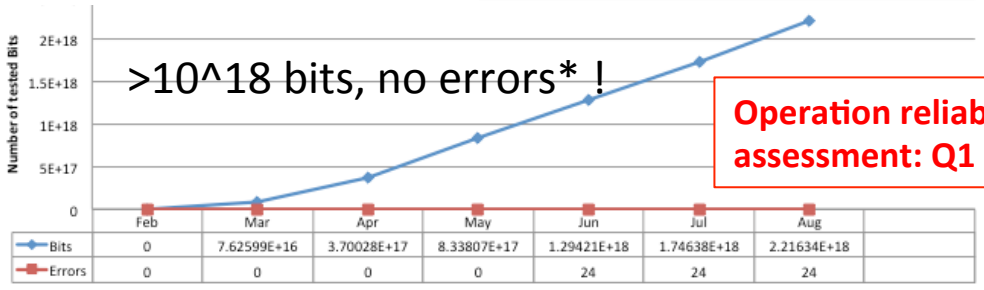


Prototype PCIe40 with ARRIA10 ES2 which implements GEN3 received in June
Will equip the MiniDAQ2
Already integrated in a server

Market survey for tender almost completed



Long distance fibre test



Operation reliability assessment: Q1 2016

* Except for 24 due to an LHC-wide power glitch…

Summary

- The upgrade project is generally progressing well
- Updated milestones have been provided
- New milestones for the production phase also included
- Some area of concern are constantly and strictly monitored