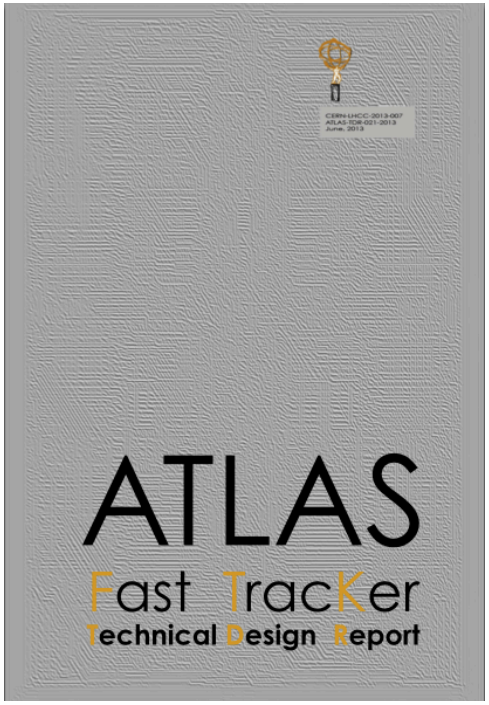

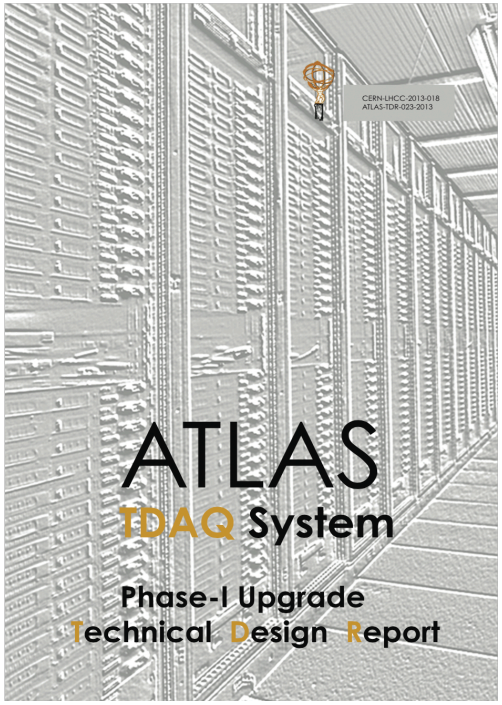

Fast Tracker and TDAQ phase-1 upgrades status

Alberto Annovi

on behalf of the ATLAS collaboration

Outline

- FTK upgrade
  - HW, SW, integration status
- TDAQ Phase-1 upgrade
  - L1Calo
  - L1Muon and MUCTPI
  - Felix

Physics motivations examples 1/2

Efficiently trigger with low thresholds at 3x LHC design instantaneous luminosity

Online $p_T > 20$ GeV 3×10^{34} cm^{-2}s^{-1}	No Change Rate [kHz]	TGC EIL4 + (TGC FI or NSW) + Tile Cal. + low field mask Rate [kHz]
Run 2 (pre NSW) Run 3 (post NSW)	51	28 13

Improved muon trigger and NSW will control muon trigger rates

Physics motivations examples 1/2

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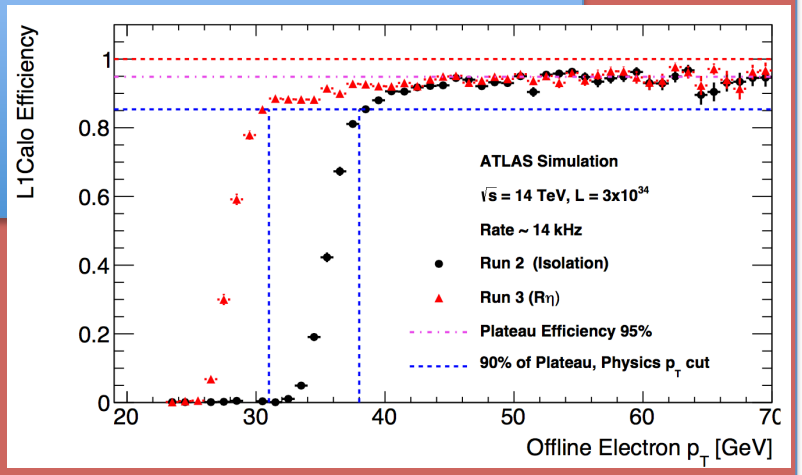
Upgraded L1 Calo will lower electron threshold at fixed rate. Exploit Rη cut.



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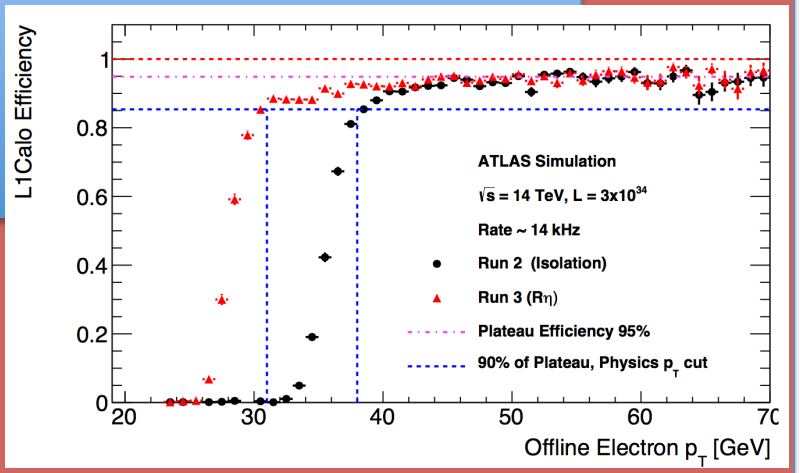

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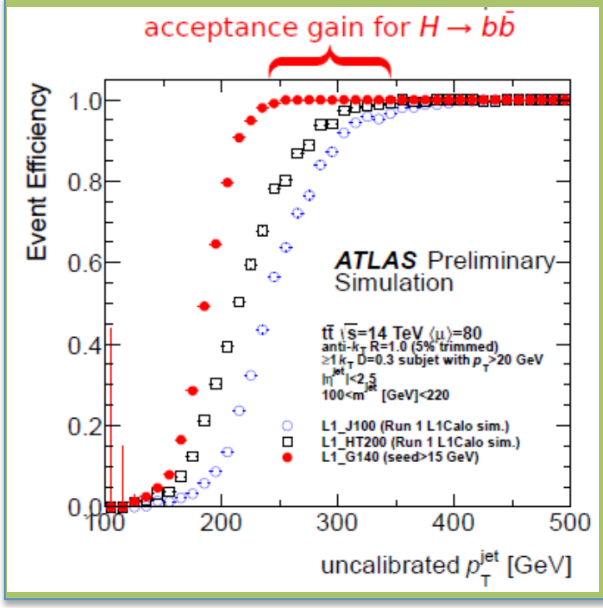

gFEX will reconstruct

- Global event variable
- Large jets reco
- Pileup suppression

Physics motivations examples 1/2

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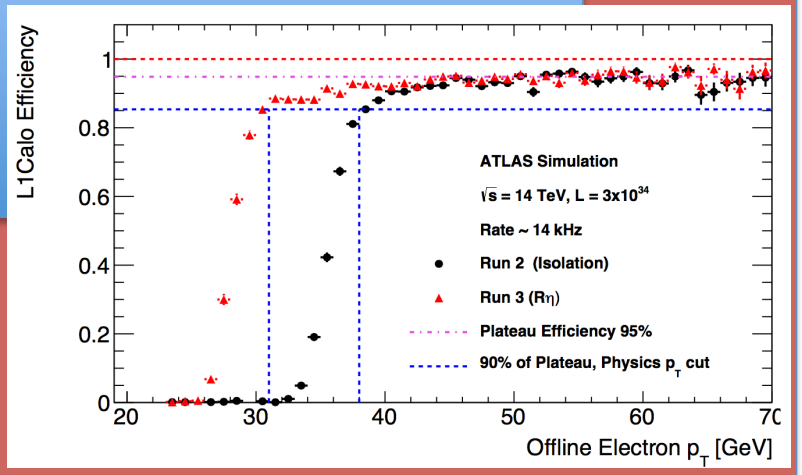

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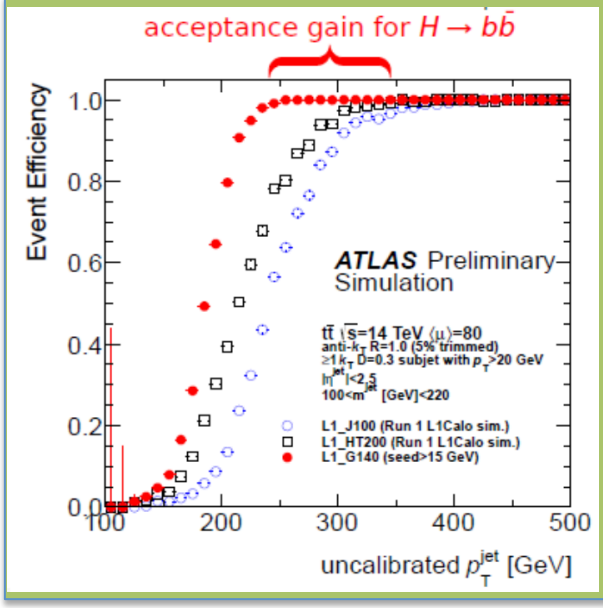


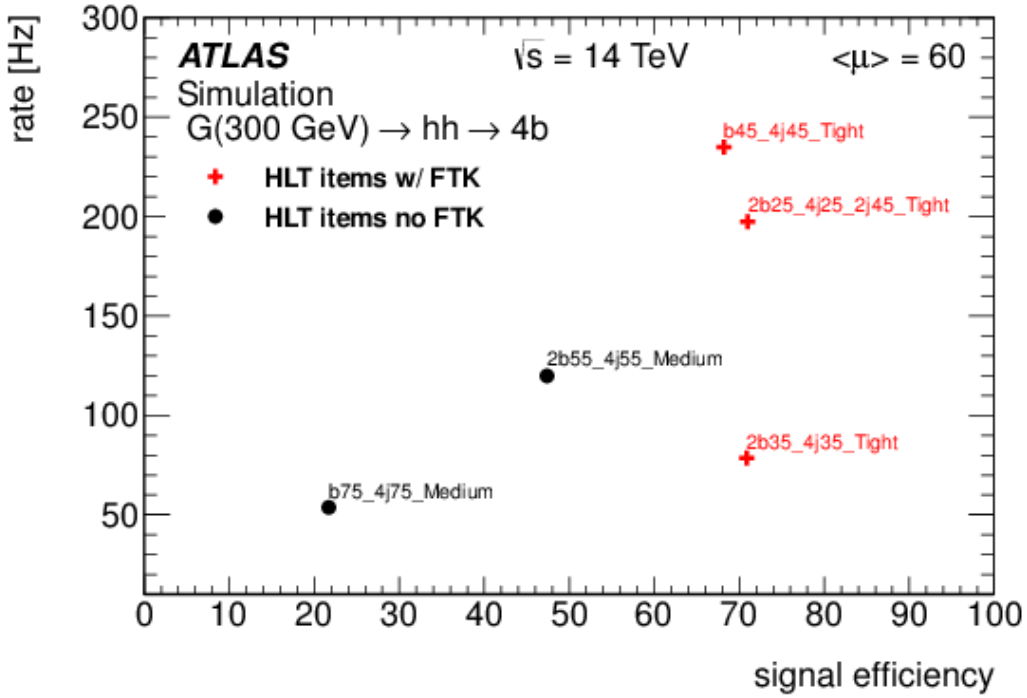
gFEX will reconstruct
- Global event variable
- Large jets reco
- Pileup suppression

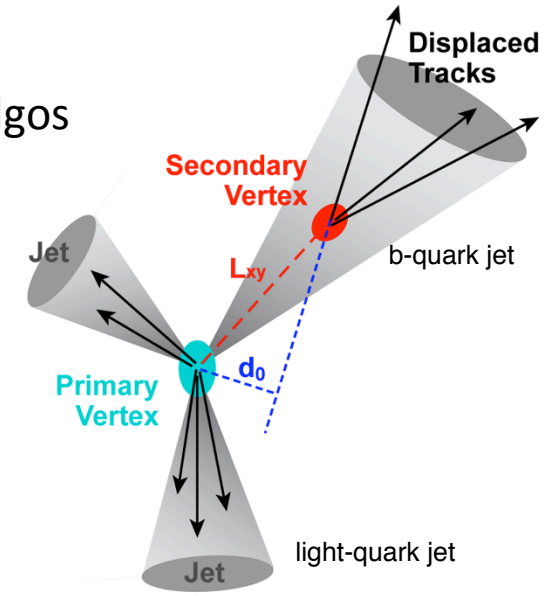
HLT will need algorithms with close to offline reconstruction performance.
Rate of electrons and muons from W and Z decays exceeding 1 kHz output rate.
Need to move analysis selections into HLT.

Physics motivations examples 1/2

FTK performance ATL-COM-DAQ-2014-011

- Exploit extensive FTK tracking for HLT
- Tau identification and Jet/MET pileup correction
- Primary vertex reconstruction for pileup resilient algos
- Can improve efficiency for multi-b jet signals
  - 3x improvements for ~fixed rate





Physics motivations examples 2/2

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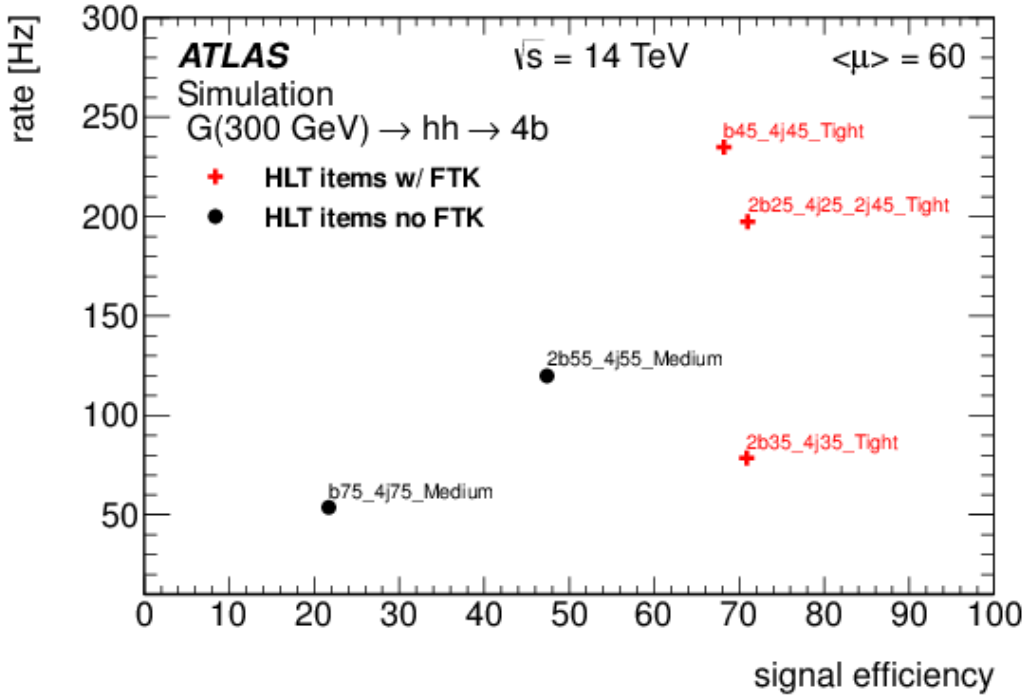
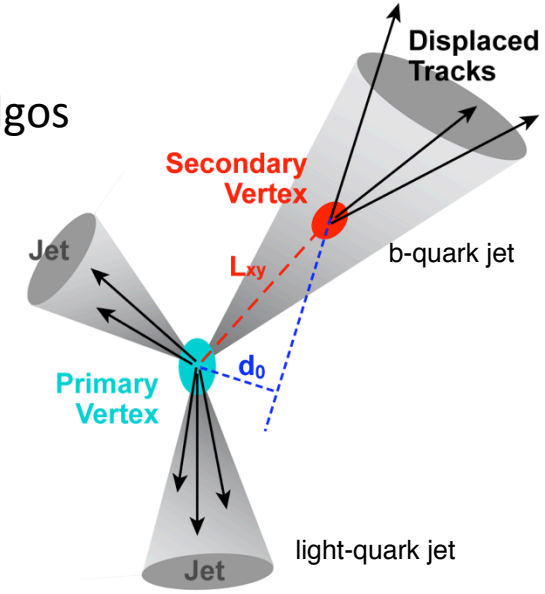
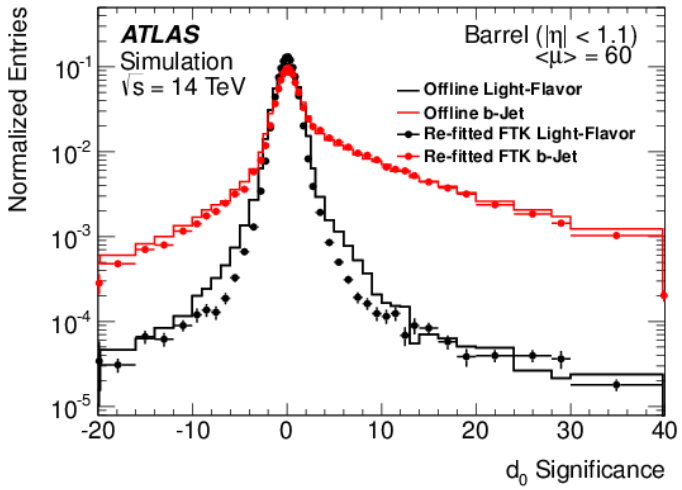
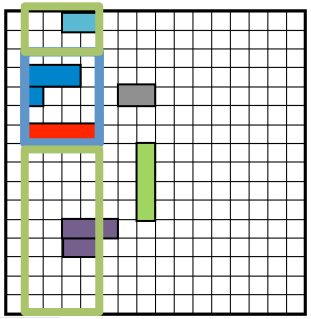




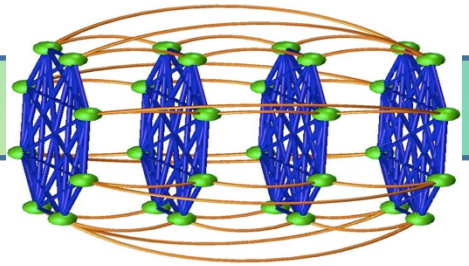


FTK Main Algorithms

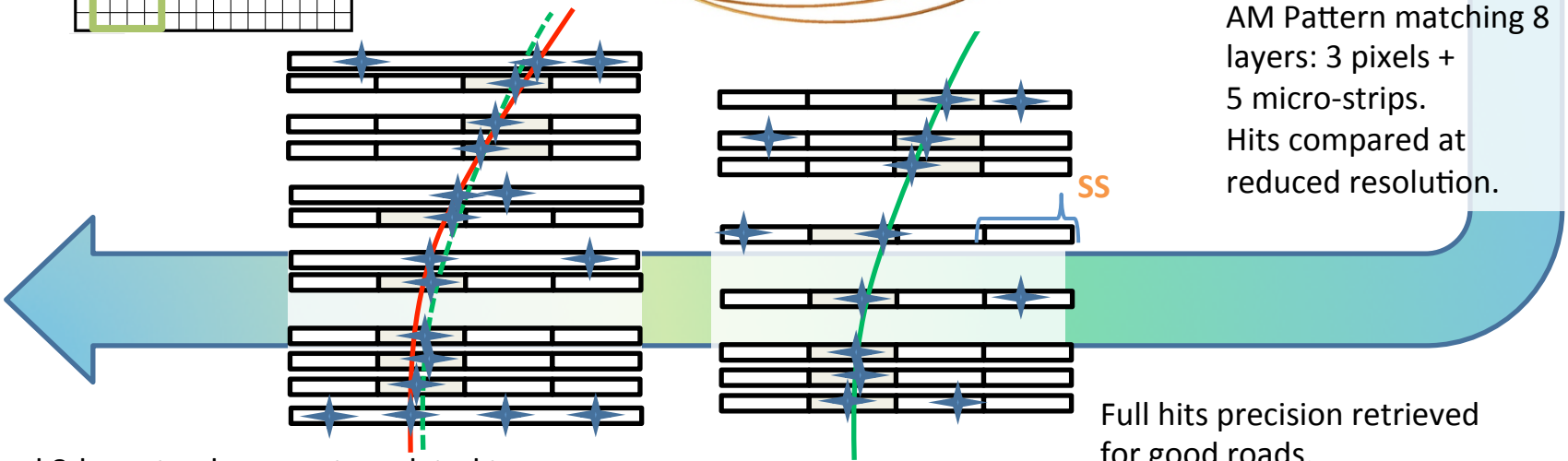
Custom pixel clustering algorithm on FPGAs



The data is geometrically distributed to the processing units and compared to existing track patterns.



AM Pattern matching 8 layers: 3 pixels + 5 micro-strips.
Hits compared at reduced resolution.



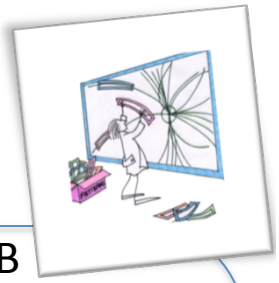
Good 8-layer tracks are extrapolated to additional layers, improving track quality

$$p_i = \sum_j C_{ij} \cdot x_j + q_i$$

Full hits precision retrieved for good roads.
Fits reduced to scalar products.

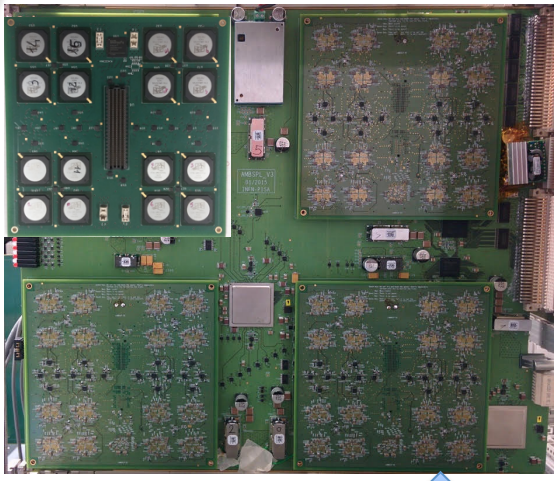
~8000 ASICs (65nm)
~2000 FPGAs
Thousands of I/O links up to 10 Gb/s

System Components



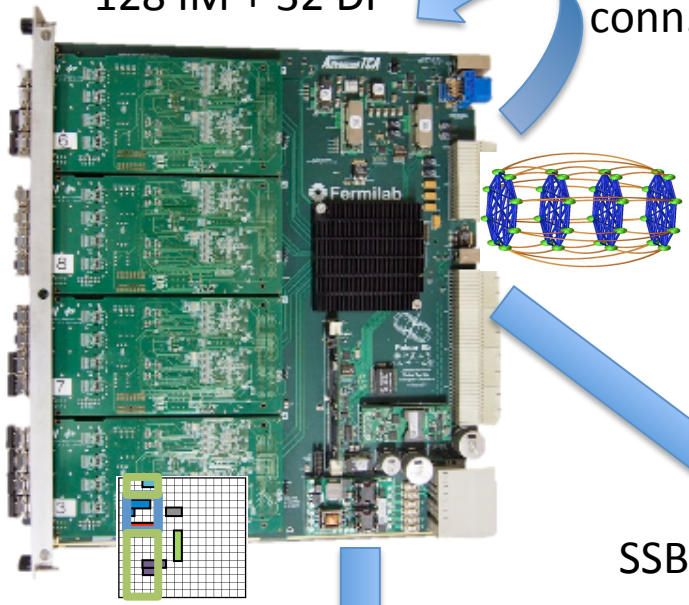
128 PUs

128 AMB



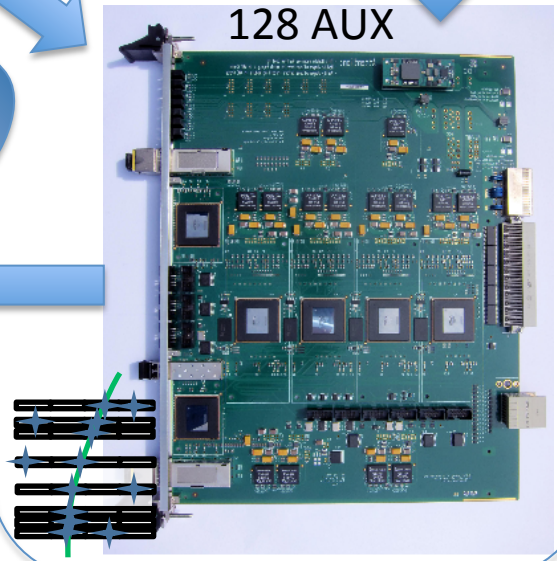
128 IM + 32 DF

DF-DF conn.

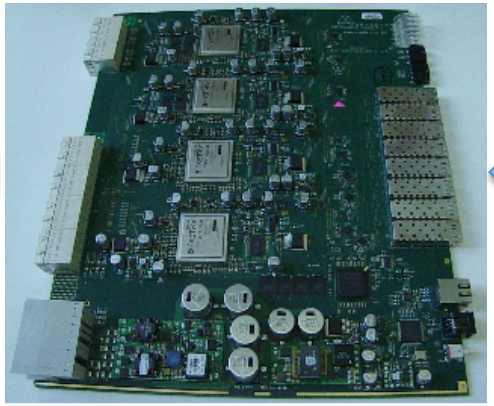


SSB-SSB conn.

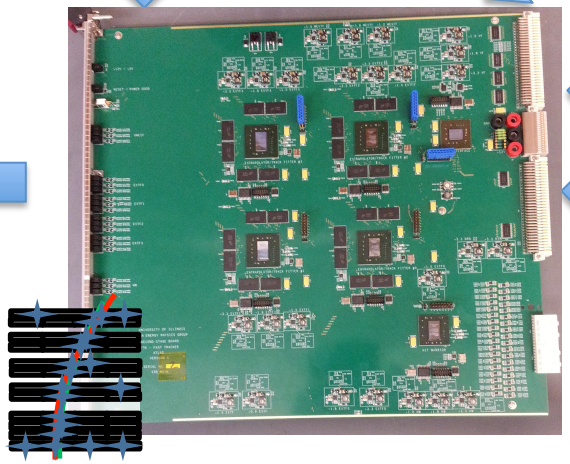
128 AUX



2 FLIC



32 SSB



FTK HW production status for barrel only mu=40

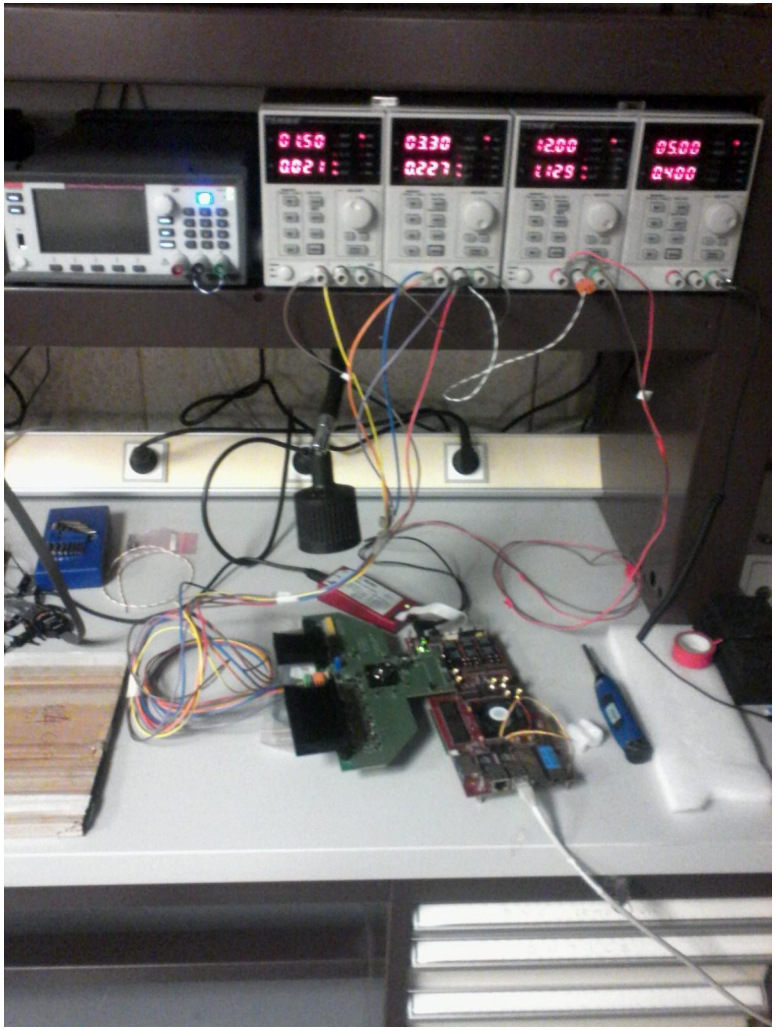
Red: expected dates, blue: actual dates

	PRR	# to be produced*	Prod. Started	1st brd @ CERN	All prd. delivered	Prod. tested	Prod. @ cern	Installed
IM S6	✔ `14	80/80	✔ Jan	Apr 20	Mar 1	100%	Oct 15	Feb `16
IM A7	✔ Apr	80/80	✔ Sep	Nov 19	Nov 26	12%	Dec 15	Feb `16
DF	✔ Jan	36/36	✔ Mar	Jul 9	Aug 31	100%	Oct 8 32/36	Feb `16
AUX	✔ Feb	20/140 *	✔ Mar*	Aug 7	Dec	Dec	Dec	Feb `16
AM06	✔ Aug	1k/8k+sp. *	✔ Jul*	N/A	Jan '16	Mar'16	N/A	N/A
LAMB	Mar`16	80/560 *	Mar `16*	Jun `16	May `16	Jul `16	Jul `16	Jul `16
AMB	Mar`16	20/140 *	Mar `16*	Jun `16	May `16	Jul `16	Jul `16	Jul `16
SSB	✔ Aug	10/37 *	✔ Nov*	Mar `16	May `16	Jul `16	Jul `16	Jul `16
FLIC	N/A	3/3	✔ May	Dec 15	Nov 12	Dec 7	Dec 15	Feb `16

* Production will happen in steps: barrel only μ=40 (indicated by *), full coverage μ=40, more processing power for μ>40

AM06 chip

- AM06 chip is a ~160mm^2 65nm ASIC (400M transistors)
  - Large area version of AMChip05 (3k patterns → 128k patterns)
- Test stand developed, fully-equipped test sites at LPNHE Paris, INFN Milano and INFN Frascati
- Issues appeared with first AM06 packaged devices
  - Discussion on going with IMEC to understand the situation
  - Should have packaged chips in about 3 weeks
- Design was submitted for fabrication in June
  - Accumulated delay is quite disappointing
- Current activity:
  - exercise test system with AM05 on the adapter for AM06 pinout
  - clean-up of firmware and development of more automated scripts for quick tests
- Integration tests use AM05 chip



FTK schedule

- **Steps A-3rd use a combination of production & prototypes boards**
- **Blue=done, * in progress now**

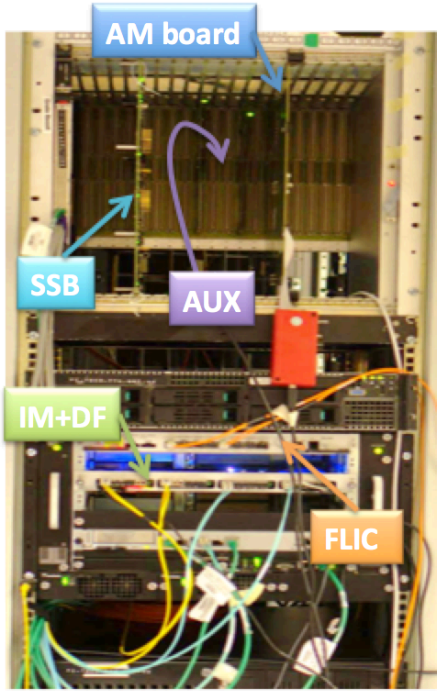
Success oriented

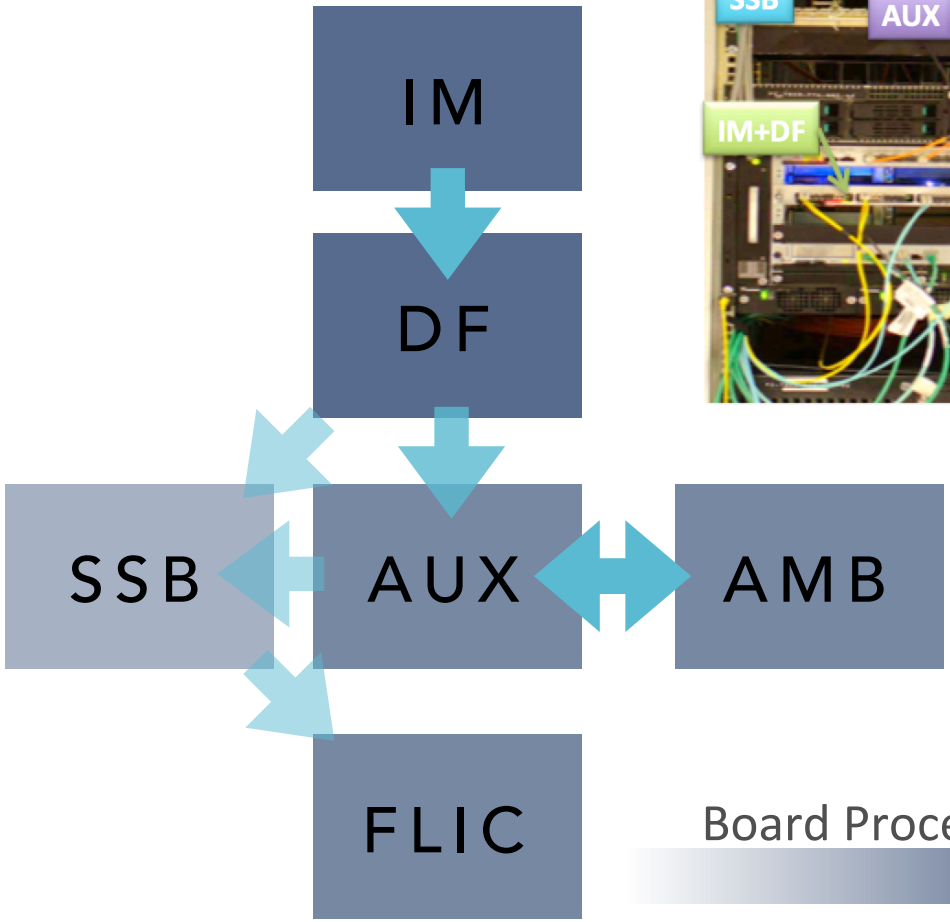
	IM	DF	AUX	AMB	AMchip ver.	SSB	FLIC	Milestones	Expected
A	4	1	1 passthrough					Included in TDAQ	Done
B	32*	8*	1	1	05	1	1*	Included in TDAQ	Next step
3rd	128	32	16	1	05	1	2	Included in TDAQ	3/2016
4th	128	32	16	16	06	8	2	Full barrel (mu=40)	7/2016
5th	128	32	32	32	06	8	2	Full detector (mu=40)	12/2016
Final	128	32	128	128	06	32	2	TDR Specs	2018 / Lumi driven

Goals: integration within ATLAS during winter shutdown
fully commission the system before AM06 are installed

Integration in the lab

- Integration in TDAQ lab in bld4 (lab4)
- At least 1 board of each kind available for chain testing
- Demonstrating:
  - Board-to-board continuous, error free data flow, including proper synchronization, busy, freeze handling
  - Bit-level accuracy of test-vector processing
  - Integration of monitoring information
- Test vectors derived from simulation at PU 40, 60, 80 with nominal system & 2016 configuration
- Activities will continue throughout early 2016



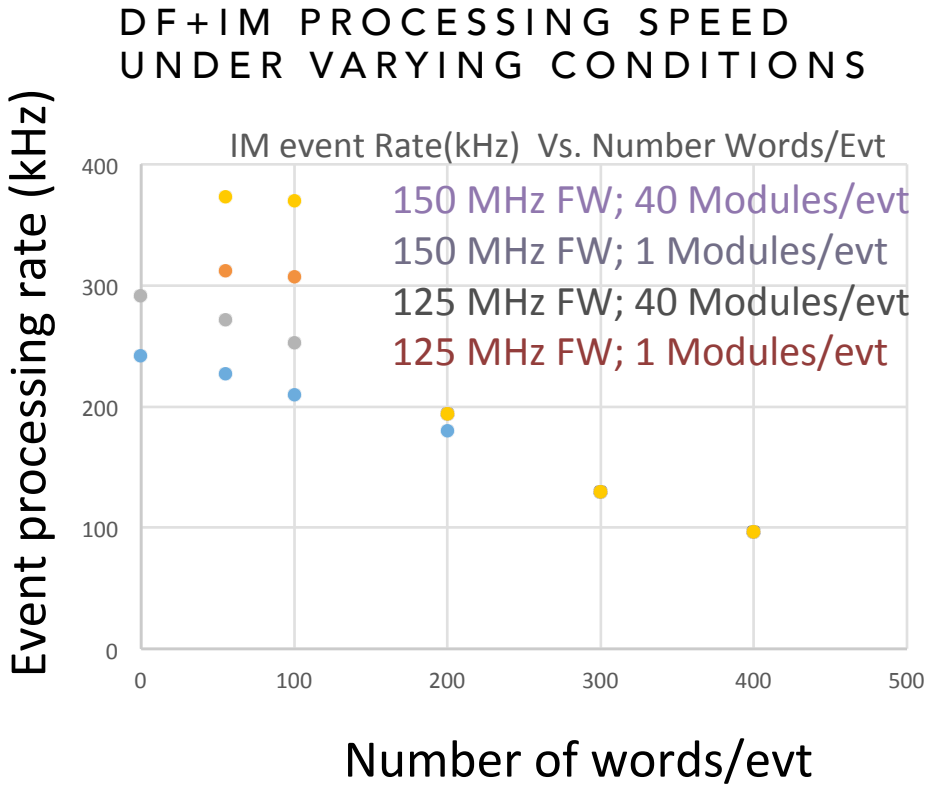


Board Processing

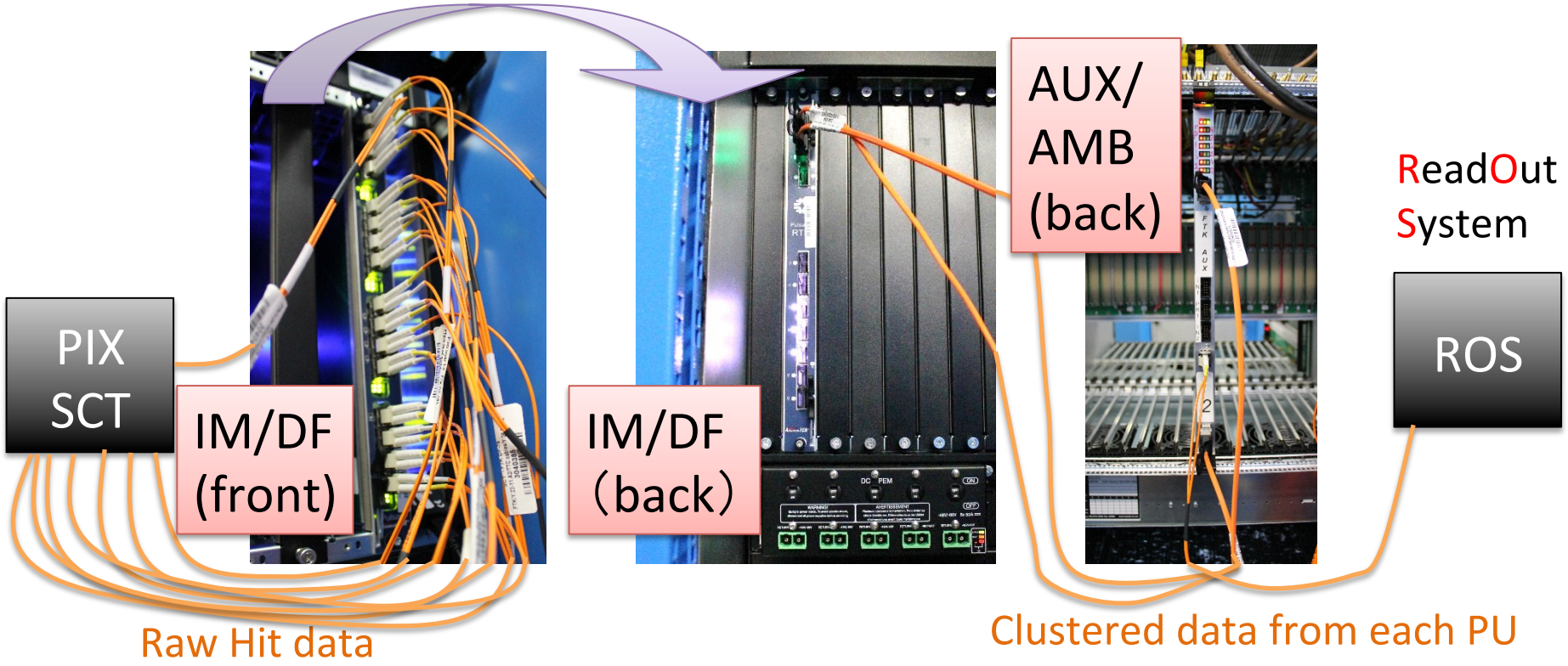
Link Integration

Example usage of Lab 4 test stand

- Controlled environment lets us test FW limits in interaction between two boards



Integration and data flow test at USA15

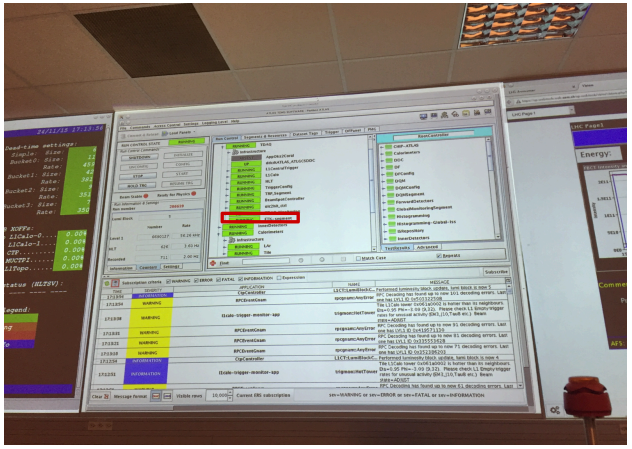


- Pixel/SCT and IBL processing tests (4 IMs + 1 DF)
- SCT → IM → DF → AUX → ROS (achieved last week)
- 32 IMs and 8 DFs (1 ATCA shelf) installation in progress
- Commissioning IM-DF well advanced
  - DF – DF interconnection to follow

Online and offline software

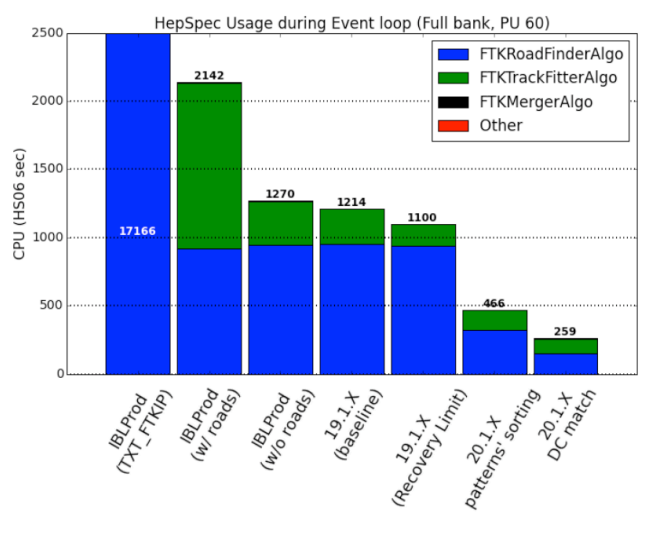
Online SW:

- Control & Configuration implemented in runControl as boards become ready for integration.
- FTK monitoring being developed: status registers are published, SpyBuffer contents analyzed and published. Monitoring system growing as more HW is deployed.

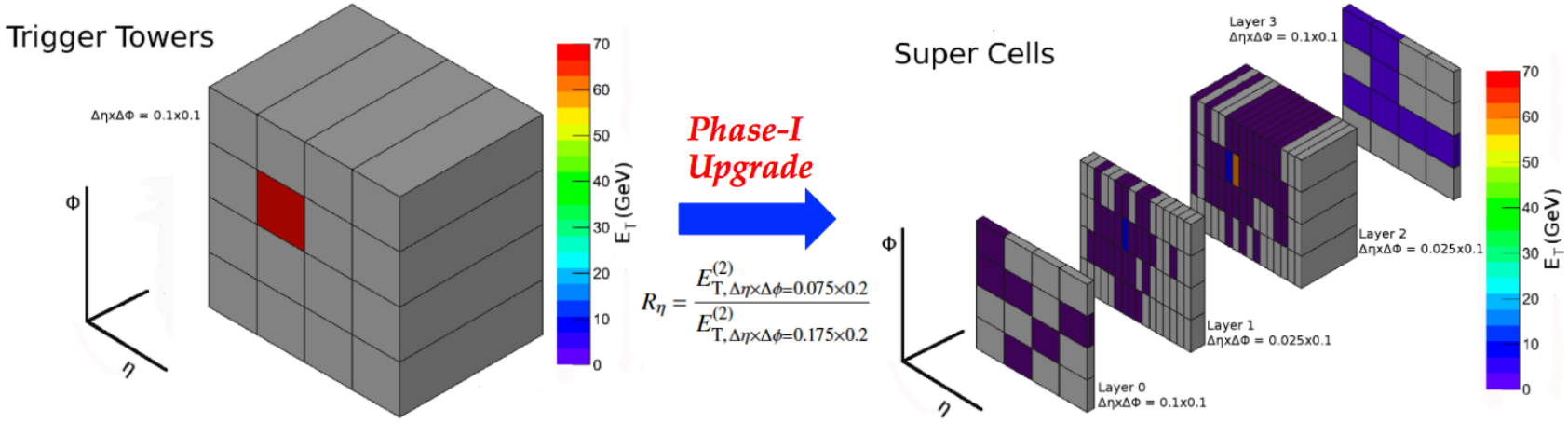


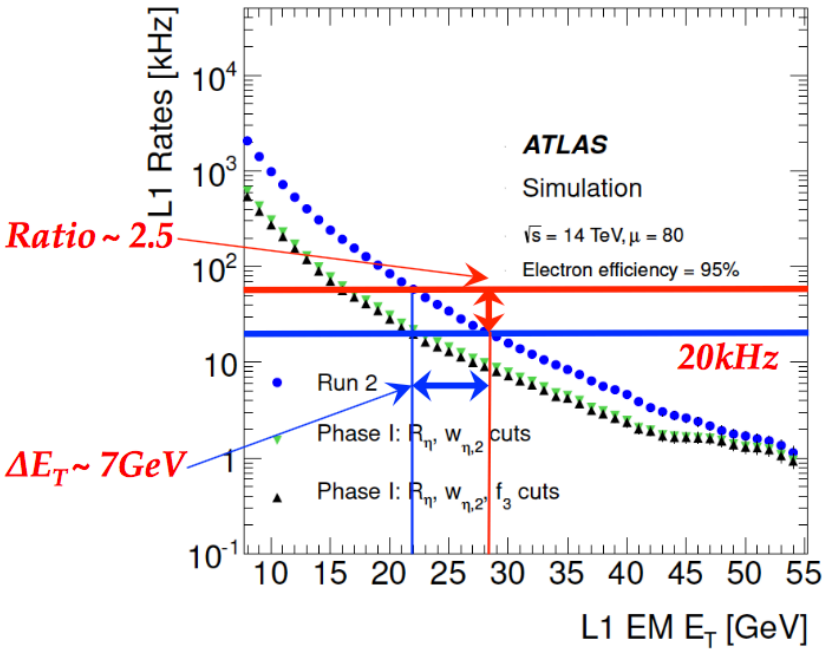
Offline SW:

- Finalizing 2016 FTK configuration and FTK training
- Studying effect of beam movement. FTK to be reconfigured for beam jumps > 400um
- Emulation of billion fold HW parallelism in a single transform fully integrated with prodsys2
- Significant code speed up
- Proof of principle of fast simulation, truth seed tracking with FTK track quality
- HLT interface for FTK tracks available, trigger chains being built
- Simulation strategy: combine full & fast emulation
- Automatic validation in preparation



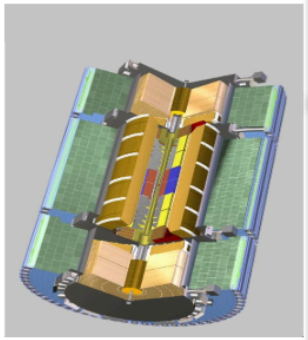
Introduction

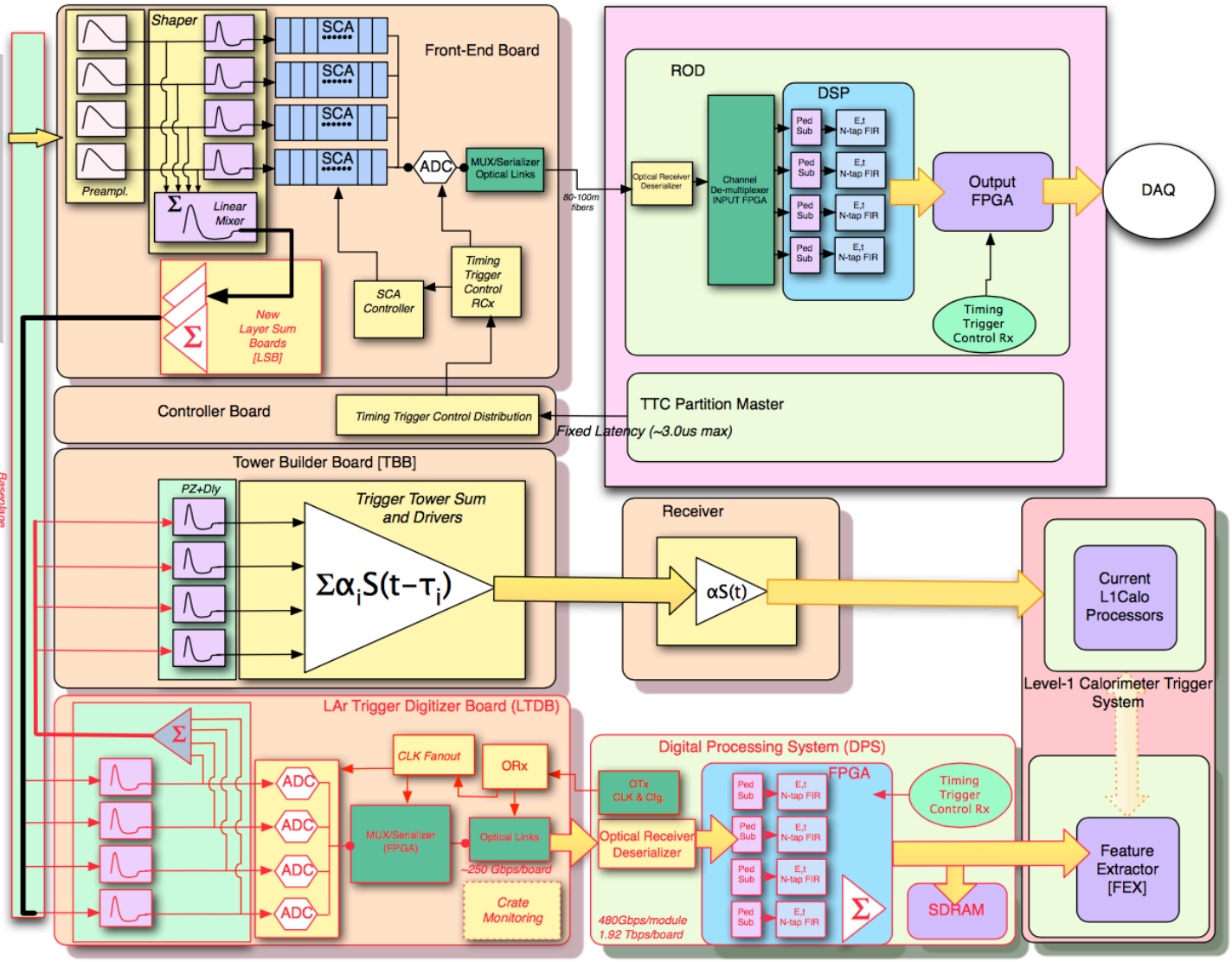




- LAr Phase-I upgrade will have new calorimeter trigger electronics with increased granularity and functionality for LAr calorimeter level 1 trigger
  - Fine lateral and longitudinal LAr Super Cells
  - Increasing granularity 10 times by changing from Trigger Tower to Super Cell readout
  - Calculate shape information for electrons and taus, and improve energy measurement in the trigger readout chain to improve trigger rejection

LAr Phase-I Readout Architecture



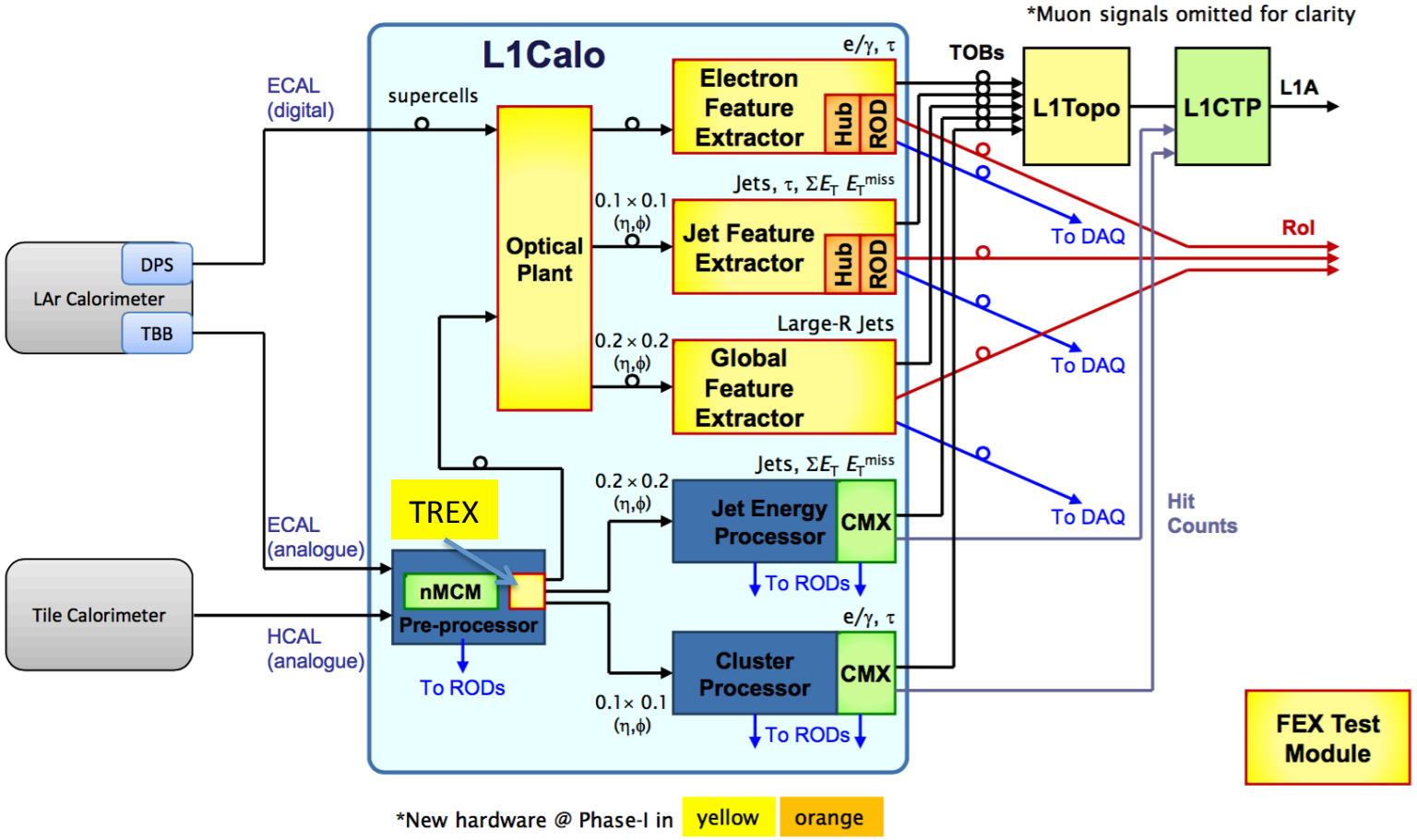


Possible implementation
$\Delta\eta\times\Delta\phi$=0.025x0.1 1st and 2nd layer EM
$\Delta\eta\times\Delta\phi$=0.1x0.1 elsewhere

- ***New elements are highlighted in RED***

New L1Calo trigger

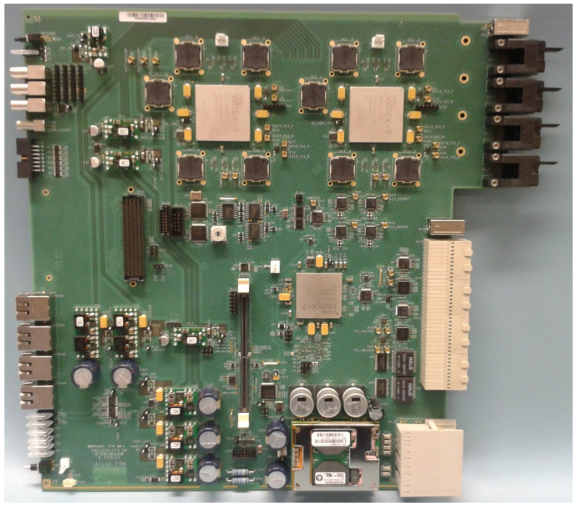
Exploit finer granularity calorimetric information to control rates at run3 pileup



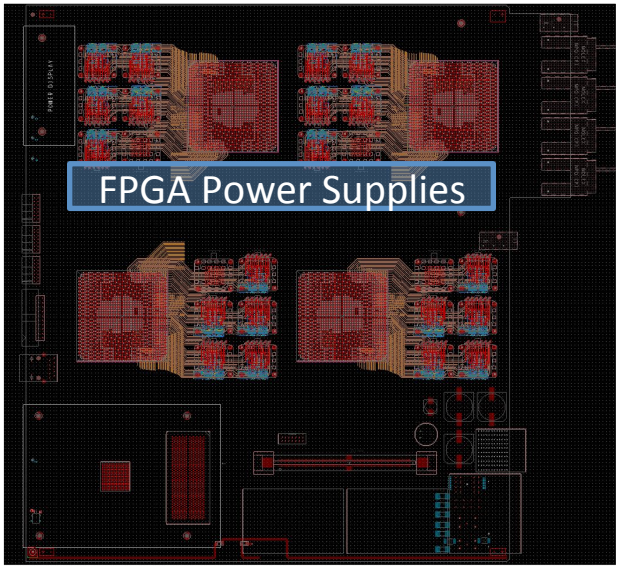
L1Calo: FTM and JFEX

- **provides multi-Gb/s data for Fex testing**
- 2 assembled FTMs delivered
- many components mounted with wrong orientation
  - Corrective actions taken by assembly company
- FTM-0:
  - Some components damaged
  - Partial features successfully tested
- FTM-1 re-worked by assembly company
- Firmware development
  - basic control interface commissioned
  - work on Gigabit links underway

Fex Test Module -> FTM



jet Feature EXtractor -> jFEX

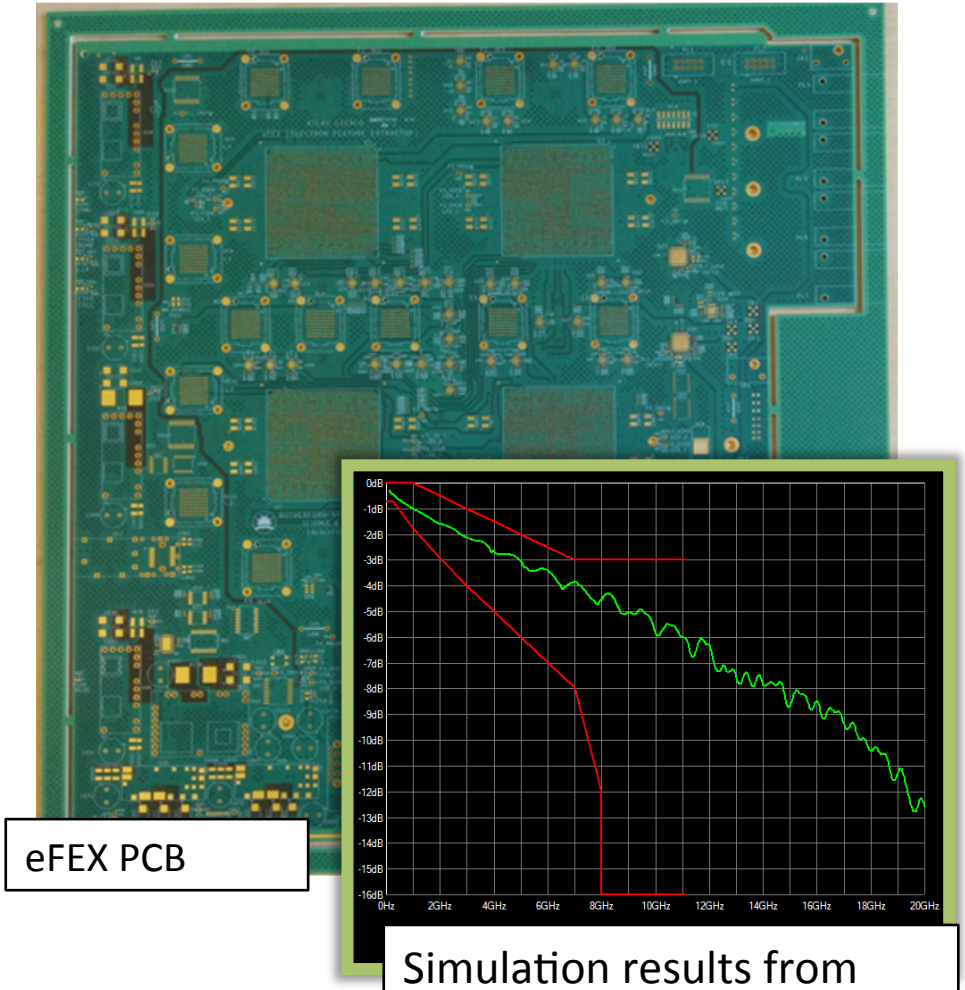


- **7-10 jFEX modules identify jet and τ signatures**
- Profiting from eFEX & L1TOPO experience
- Modular design (FPGA+mPOD) 4-fold symmetry
  - control on the mezzanine
- Layout ongoing
  - manufacture mid-Q1 2016
- Firmware in development
  - I2C, IPBus, monitoring…
  - (a lot common to L1Topo)
- → Integration test at CERN Q2 2016

L1Calo: em Feature EXtractor -> eFEX

(identifies events with e/γ/τ signature; 24 modules covering |η|≤2.5)

- The eFEX in numbers
  - 3189 Components (5x Virtex 7)
  - 4 clock domains
  - 3942 nets (424 multi-Gb/s pairs)
  - 13,142 connections
  - ~350W/module
- Post-layout simulation & optimisation completed
- Sent to manufacture in July 2015
- PCB batch 1 failed
  - plating voids due to oven failure
  - investigating use for power circuit
- PCB batch 2 failed
  - plating voids in micro-vias
  - design OK
    - copper balance, track density & stack-up
  - process to be adjusted: copper-fill vias (as per FTM)
- Batch 3 in manufacture
  - assembled eFEX expected in January
- Firmware
  - basic control firmware complete
  - test engine for link-speed tests in development
    - complete by mid-December



eFEX PCB

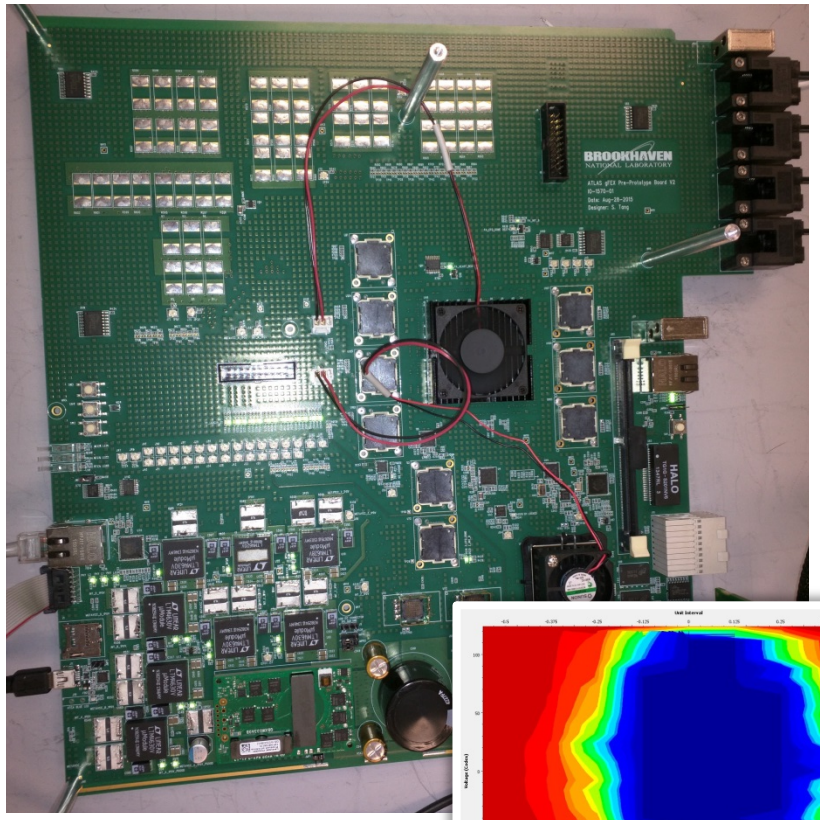
Simulation results from HyperLynx for typical track, attenuation vs. frequency

L1Calo: global Feature EXtractor -> gFEX

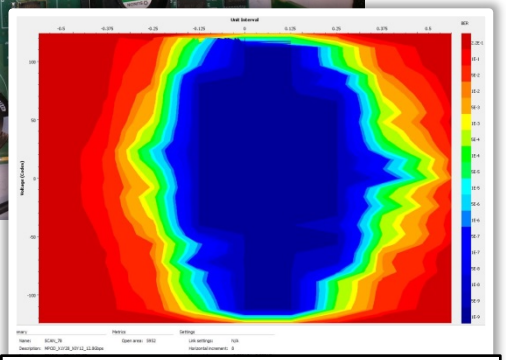
(identify large area jets and global event variables
1 module for the whole calorimeter)

- Prototype 1a tested
  - Power, clock , Zynq
  - MGTs: 80 × 12.8 Gb/s: BER <1.2 × 10^{-15}
- Prototype 1b
  - Re-work (clock, DDR3 & PHY)
    - 4 PCBS received , 1 assembled
    - Testing underway
- Prototype 2: Full prototype
  - Design changes
    - 4×V7 → 3×Ultrascale (XCVU160)
    - FELIX readout
  - 50% Routing completed
    - manufacture end of 2015
- Firmware
  - control
  - test engines
  - algorithmic

  } ~Done
  - GBT & TTC interfaces



gFEX Prototype 1b

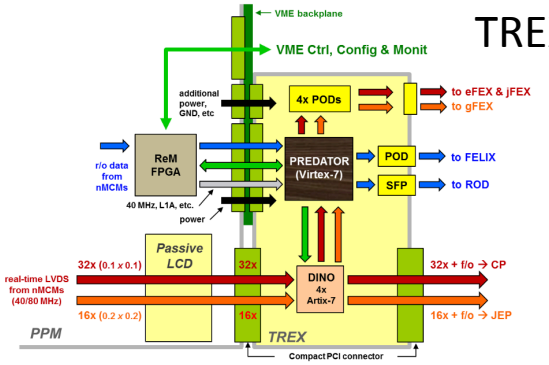


IBERT eye for pFPGA→Fibre→pFPGA @ 12.8 Gb/s

L1Calo input/output

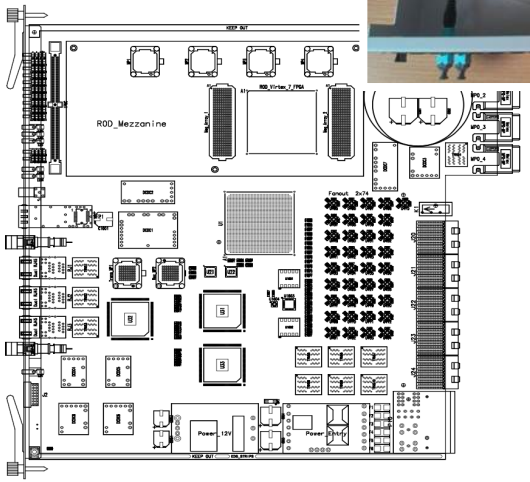
- ***TREX: pre-processor to FEXes***
  - PDR held on 31st July
  - first draft of schematics complete
  - schedule: manufacture Q1 2016
- ***FOX: fiber optic plants***
  - demonstrator manufactured
  - LAr/TileFOX Demonstrator
  - e/j/gFOX Demonstrator
    - Includes splitting and fanout
- ***Hub: ATCA***
  - layout and routing advanced
  - assembled modules expected early January.
  - control firmware in development
- ***ROD (hub mezzanine)***
  - 6 PCBs manufactured
  - 1st module partially assembled under test
  - Fully assembled module expected mid-December
  - Firmware to test major interfaces in development
    - Link-speed firmware to be done

TREX

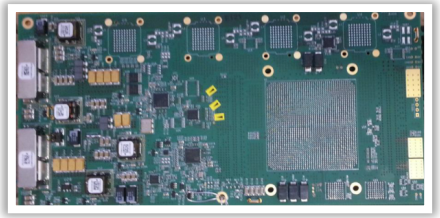


FOX demonstrator

HUB



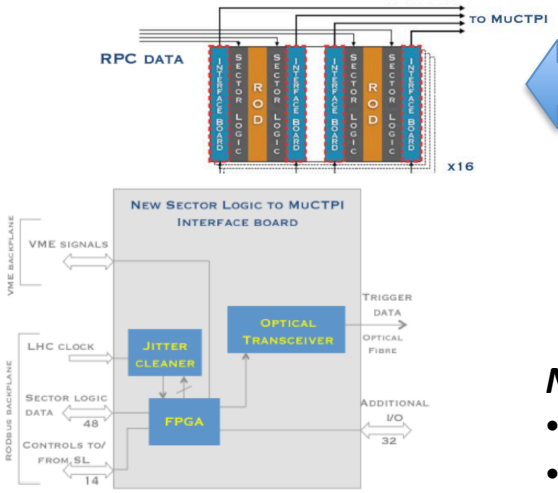
ROD



LAr–L1Calo Link-Speed Tests

- LAr–L1Calo Link-speed is not yet defined: options: 6.4 Gb/s, 9.6 Gb/s, 11.2 Gb/s
  - impact on signal bandwidth, mapping & quality of information
- Limited experience of multi-Gb/s PCBs of complexity of eFEX & jFEX
  - test prototypes before making final commitment
- LAr–L1Calo Link-speed tests scheduled for January– March 2016
  - A first step in on going LAr – L1Calo test plan
  - LAr – gFEX
  - LAr – eFEX (eFEX proxy for jFEX)
    - jFEX will be tested later in 2016

L1Muon upgrades

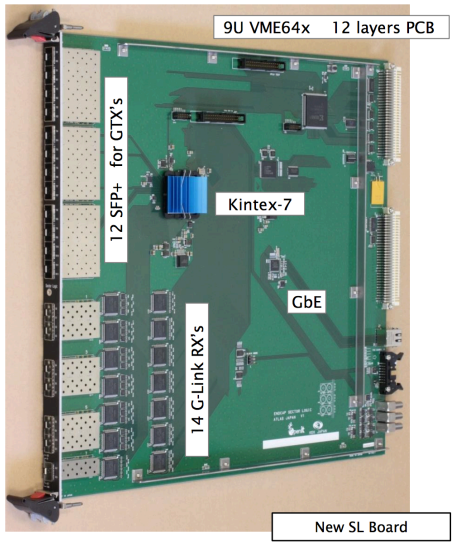


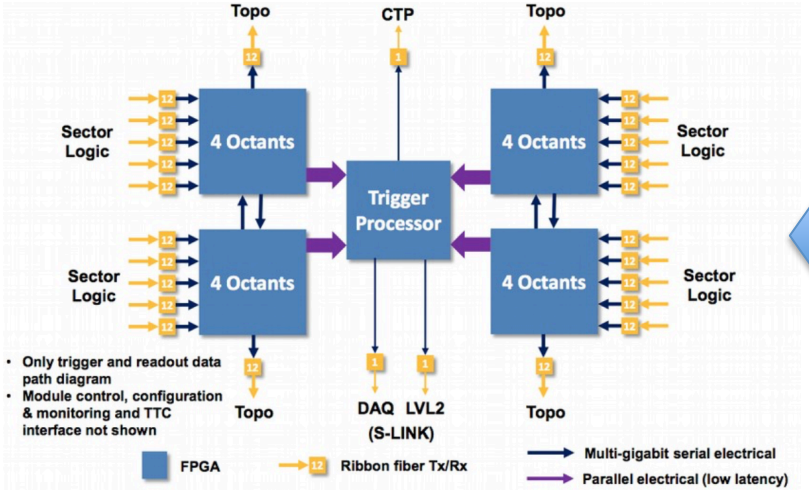
Barrel trigger SL–MUCTPI Interface Board

- Data rate ≤ 6.4 Gb/s.
- ≤ 4 muon trigger candidates per trigger sector per BC
- Design of 1st prototype underway
  - Complete ~Q1 2016

New Endcap Sector Logic (process NSW data)

- 12 optical I/O SFP+↔FPGA GTX
- Optical G-link inputs from TGCs
- Prototype manufactured
- All IO tested & working well: GTX up to 10 Gb/s



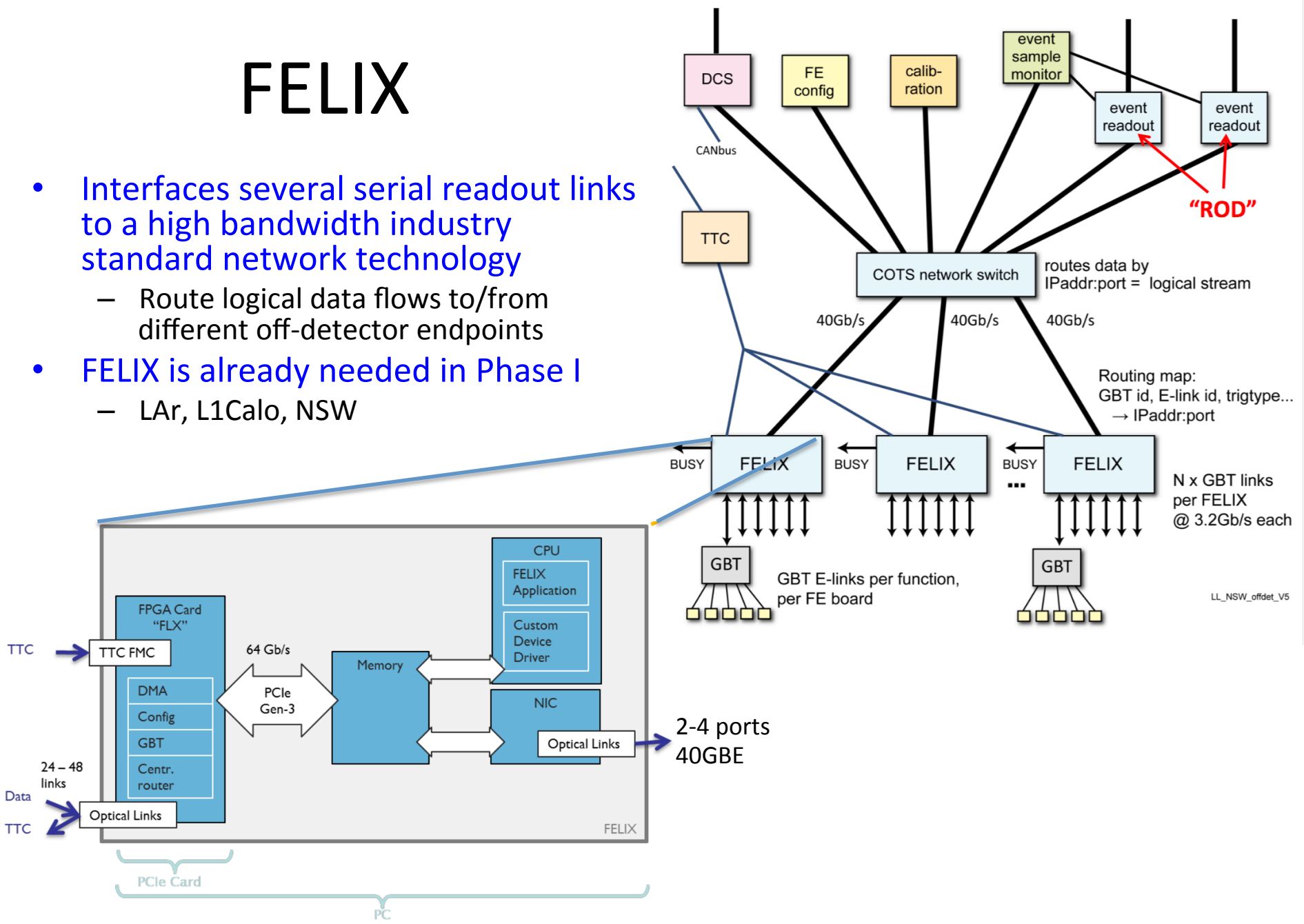


MUCTPI

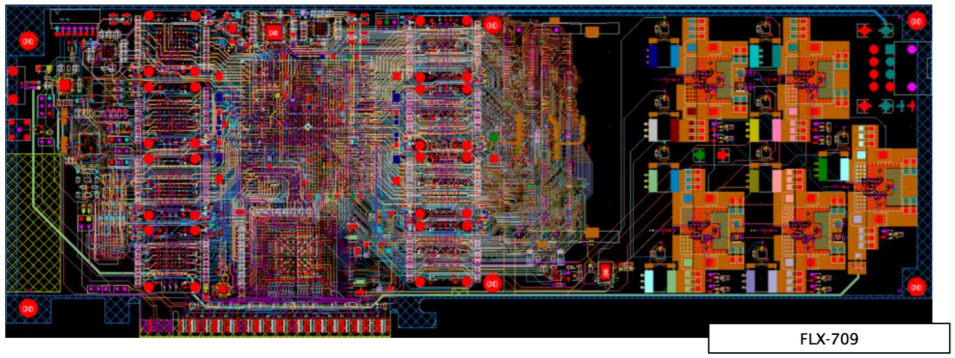
- interface with new Endcap sector logic, NSW
- full-granularity muon trigger RoI information to topo
- PDR 9th December, 2015
- 1st prototype anticipated Q3'16

FELIX

- Interfaces several serial readout links to a high bandwidth industry standard network technology
  - Route logical data flows to/from different off-detector endpoints
- FELIX is already needed in Phase I
  - LAr, L1Calo, NSW



FELIX

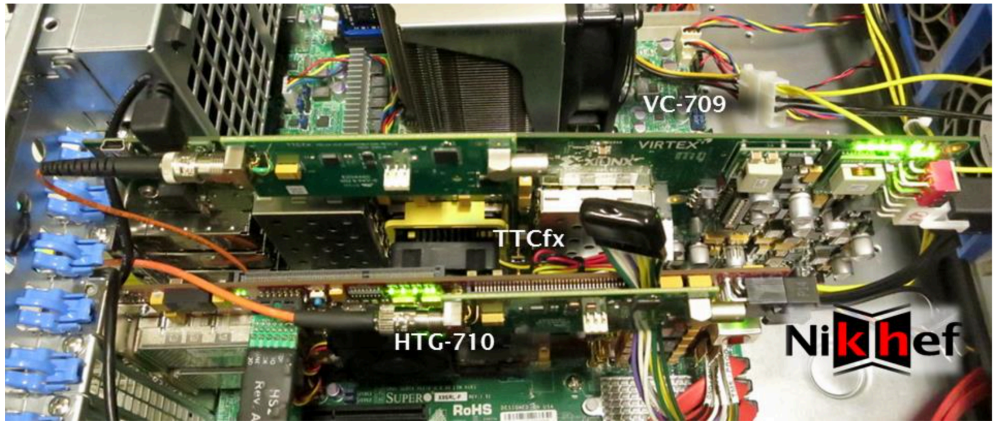

FLX-709

- FLX-709 candidate FELIX card
- PCIe board, ≤48 channels
- Original use in LTDB (LAr Trigger Digitizer Board)
- Xilinx Kintex Ultrascale FPGA
- TTC decoder onboard
- Under development, available beginning 2016

- Mini-FELIX COTS demonstrator using:
  - Xilinx VC-709 eval card (Virtex-7)
  - TTC over FMC card
- Q1/2016 integrate mini-FELIX within detectors test beds
  - FDR Spring 2016


TTCfx

Mini-FELIX



Summary

- FTK upgrade
  - Some delay accumulated w. r. t. a very aggressive schedule
  - Expecting AM06 ready for tests very soon
  - Most HW is in production or will be soon
  - Now integrating first components in USA15
- TDAQ upgrade
  - L1Calo most modules have reached/reaching hardware prototypes
    - some manufacturing problems, monitoring closely
  - L1Muon and MUCTPI prototyping in progress
  - Mini-FELIX demonstrator being integrated
- Will enable ATLAS to efficiently trigger under run 3 conditions

Thanks for your attention