Review Report

By Piyush Joshi

Committee Members: Piyush Joshi (Chair, BNL), Horst Welker (GSI), Gilles Le Godec (CERN), Tony Fowler (CERN), Andrzej Siemko (CERN).

Observer Members: Marta Bajko (CERN), Davide Tommasini (CERN).

Review date; Time; Place: February 29, 2016; 9AM-5PM; CERN Bldg. 30.

Review process consisted of presentation from design engineers of various component of 7.5KA IGBT switch followed by closed door discussions among committee members.

Topics presented were:

1. Power Electronics Design.
2. Control Electronic Design.
3. Cooling water system.
4. Dump resistor assembly.
5. Monitoring software and data logger.
6. Rack, power bus bars and mechanical integration.
7. Simulation and actual test results.

Committee evaluated production readiness based on charges mentioned in appendix A. One of the committee members (Piyush Joshi, BNL) also observed actual functioning of the switch at 7.5KA and all transient data captured on the oscilloscope. Based on the presentations and observations, committee findings and suggestions are as follows.

Power Electronic Design: All IGBTs are observed to be operating within their "Safe Operating Region" with regards to temperature, current, transient voltage and gate drive parameters. Design of triple sandwich bus bar, equal circuit impedance presented to each IGBTs and overall symmetry assures better current sharing and switching symmetry among IGBTs. Laminated bus bar design, IGBT layout and three stage snubber design has very effectively eliminated all transient voltage spikes associated with high current ultra-fast (10microsecond) turnoff.

Control Electronics and Data logger: Control electronics design is observed to be mature and reliable with two channel of redundancy on all components and functions. Committee suggested that connectors be color coded so that they are always correctly matched during plugin operation. It was pointed out by design engineer that even if connectors are plugged in wrong location functional damage is not possible.
Data logger platform based on National Instrument cRIO chassis with embedded FPGA is known to have good reliability. Compact RIO chassis seems to be crowded with very little space for future additions.

Committee suggests that four slot cRIO chassis be replaced by 8 slot chassis to accommodate few more signals regarding cooling water flow as mentioned below.

Software Design: It needs improvement and addition with regards to user interface, clear display of faults and action taken during the fault. User defined threshold should be available on the interface screen and not embedded in the program. For example, what actions should be taken if external watchdog fails, temperature threshold are exceeded, current sharing threshold is reached etc.

Thermal and cooling water: Thermal design is very sound and assures operation of all components within their thermal limits. One suggestion is to monitor and electronically log water flow values.

Dump Resistor: Temperature rise and hot spot during the test of 6 MJ square wave energy dump were well within the thermal rating of each resistive elements. Mechanical assembly and ease of achieving required dump resistor combination is well planned.

Test Results: Test results presented during the review and observed during real test provided enough proof of the sound and reliable overall design. Oscillographs of Vce and transient spikes at turn off are shown in Appendix B.

Other discussions during the review:

- Can monitoring Vce be used to estimate IGBT degradation ?
- Check if degradation of IGBT is function of junction to case thermal resistance or case to heat sink thermal resistance.
- Explore another vendor and/or all master configurations for IGBT gate drivers.
- Review of Lab View program by third party.
- Ensure that connectors are in right place.
- Generate incoming inspection matrix for IGBT and other components manufactured by outside vendors.
- Perform X-ray or ultrasonic imaging of each heat sink manufactured by outside vendor.
- Future Outlook: Considering that 30KA switch is a pilot project for TE-MPE and that Infineon IGBT is optimized and characterized for switch mode applications, it is recommended to qualify several other IGBT suppliers based on a comprehensive study and measurements and not only on datasheets. The main parameters to be assessed, at the least are:
    - The forward collector emitter voltage drop (Vce)
    - The thermal resistance Rth-jc (Junction to case)

Based on the presentations, observations and discussions among review committee members it is concluded that electrical and mechanical design of 7.5KA IGBT based static switch is matured for production phase.

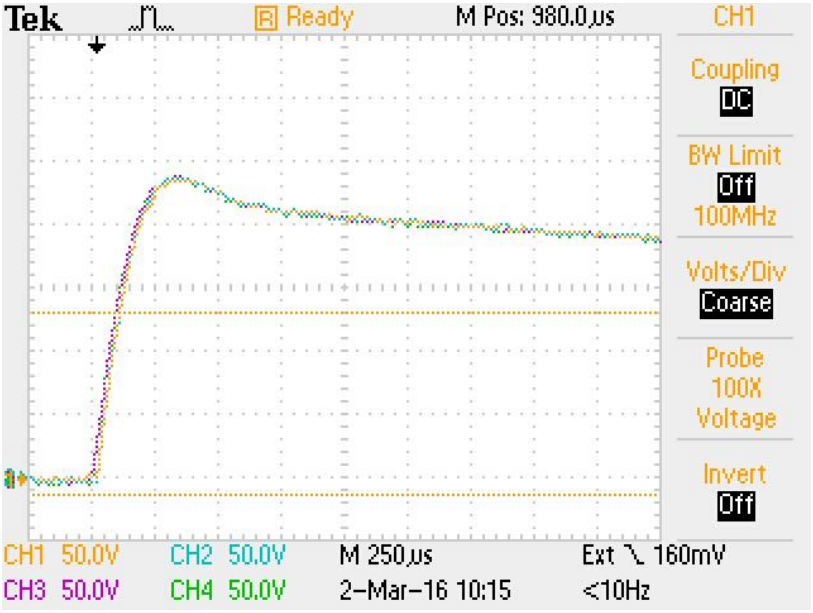
Appendix A

Charge:

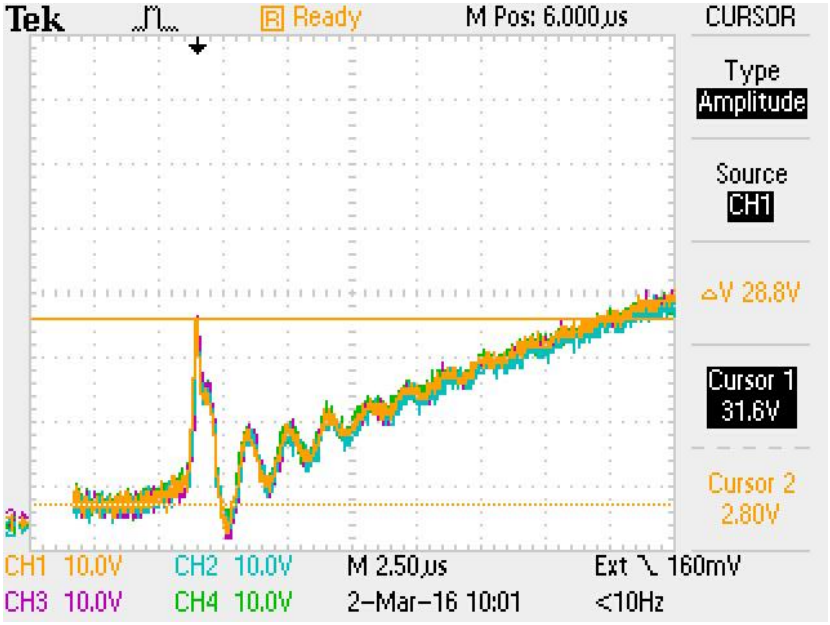
- Is the proposed solution coherent with respect to the functional specification?
- Is the prototype implementation sound regarding:
    - Power electronics and cooling
    - Symmetric design
    - Compensation of e.m. fields
    - Minimization of stray inductance
    - Synchronization of parallel IBGTs
    - Overall integration
- Is the design of the control & protection sub-system adequate?
    - Are the expectations for the controls and protections sub-system clearly defined in the design requirements, risk assessment tables, the critical events & actions and fault matrix documents
    - Are there changes to the control & protection sub-system that are recommended?
- Presentations will also include a preliminary risk assessment for various operating conditions, quality control and test program of the prototype unit. Comments on these would also be appreciated.

Appendix B

Oscilloscope waveforms observed during the 7.5KA switch test



Vce at 250 uS/div time scale. Peak reached is 460V



Vce Switch OFF transient captured at 2.5uS/div