30kA Energy Extraction Semi-Conductor Switch

PRR: 29-01-2016

SM18 - CLUSTER D

30 kA General Layout & Basic Concepts

Gert Jan Coelingh on behalf of all team members
TE-MPE-EE

Outline

- Review objectives
- Project team
- SM18
- Requirements
- Schematics
- Design Criteria

- Starting from zero
- Project Status

Review objectives

- **To present the concept- and prototype design**
- **To present the results of the prototype tests**
- **In the light of those results, to review and discuss together the designs and possible improvements**
- **Come to a common agreement on:**
  - **The designs**
  - **The required validations**
  - **The production schedules**

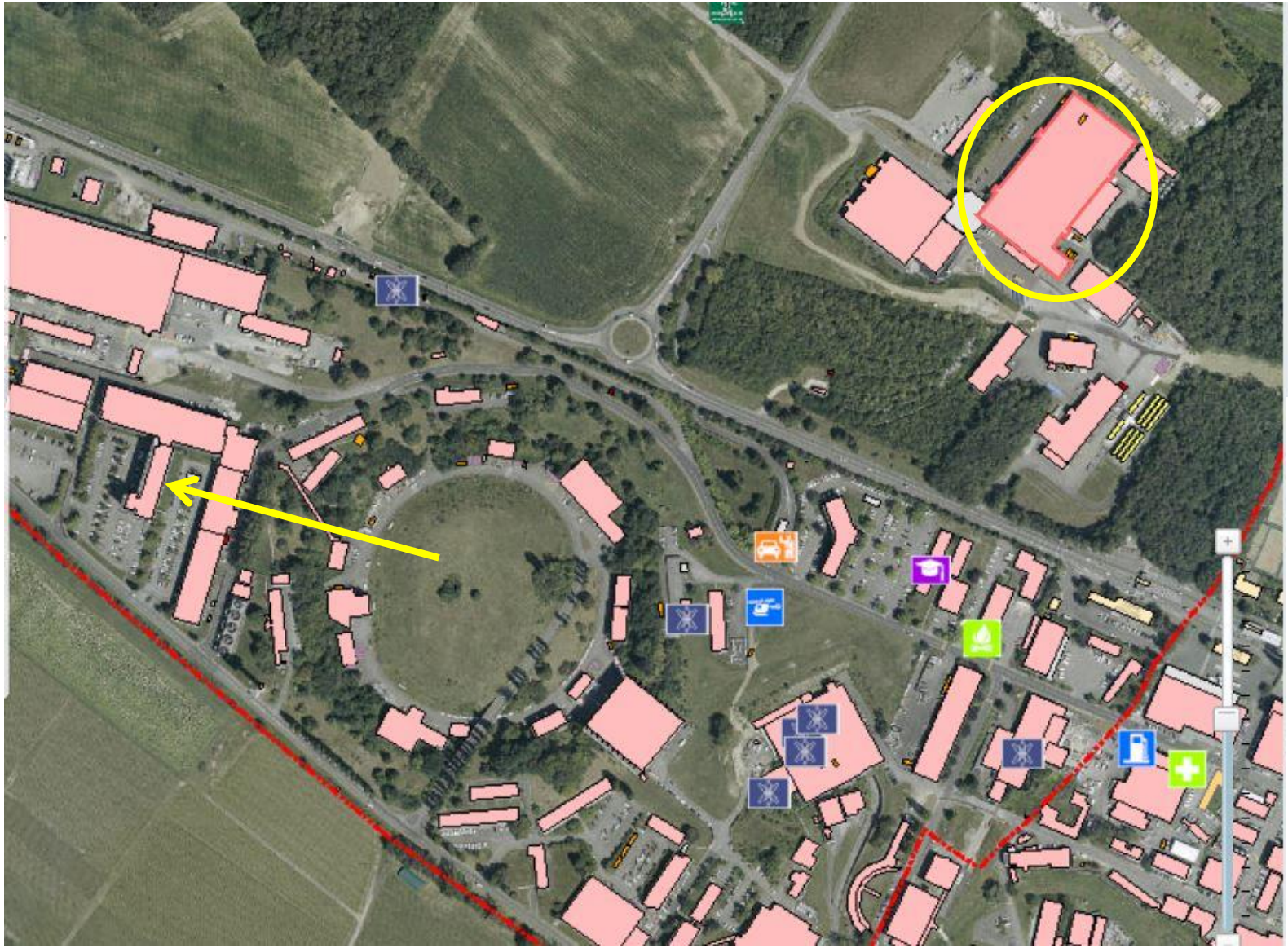
Project team

- Core team members: Alexandr, Arend, Gert Jan, Mateusz

- Supporting teams electronics: Bozhidar, Pål, Szymon, (Ron)
- Supporting team 1 electro-mechanics: Mathieu, Samuel
- Supporting team 2 electro-mechanics: Grzegorz, Stephen, Krzysztof (left)
- Others involved: Knud, Rins (Feb 1),

- Solomon (ext): 2D-, 3D- & production drawings
- Mathieu: production drawings

Building 2173 aka SM18 - Cluster D



Requirements EE Cluster D

- Demand from the TE/MSC group (SM18) for Energy Extraction Systems:
  - Fast opening time (1 ms)
  - High Current 30 kADC
  - Medium Energy (10 MJ)
  - Maximum Extraction Voltage: 1000V

Opening time means; can't be achieved with Electro-Mechanical Breakers

Alternative: Semi-Conductors

Chosen type: Integrated Gate Bipolar Transistor (IGBT)

Requirements F.S.

TE-MSC-TF & TE-MPE-EE

EDMS Document No.

1584106

Date: 2014-03-14

Functional Specification

HL-LHC MAGNET TEST FACILITY IN SM18: POWERING AND ENERGY EXTRACTION PART OF THE CLUSTER

Abstract

For the test of the HL-LHC magnets a new vertical test facility is needed. This document describes the main characteristics of the magnets and the facility functions from the powering and energy extraction point of view.

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Distribution List:

Documents Status: Engineering Check

TYPICAL MAGNET PARAMETERS

- Maximum stored energy : 10 MJ
- Short Sample current : 21.5 kA
- Magnet inductance (ex. Of HL LHC QXF type) : 8. 27 mH/m
- Magnet length : 1 – 4.2 m max.
- Nominal Ramp Rate: 11 – 20 A/s
- Maximum Ramp Rate: 200 A/s

Requirements Functional Specification

3.1.4 ENERGY EXTRACTION OF CLUSTER D

The energy extraction will be made with and external dump resistor. The dump resistor value will be adjusted case by case and in function of the necessity but always set such that with the maximum expected quench current the voltage stays below the last successfully qualified test value, typically obtained during a test performed while the whole magnet is in LHe and ready for the test. The max. value is 1000 V. To extract the maximum energy and stay within a given voltage , lower than the designed value, there is a strong interest to place the ground of the converter in the middle of the dump resistor.

The extraction will be triggered by the quench detectors with or without delays and trough a dedicated switch the power converter will be switched off and the current will go trough a free wheel. The reaction time of the switch was set up in function of the maximum allowed temperature in the most critical magnets after a quench and is set in the range below 1 ms leading to the choice of IGBT based technology.

4.1.2 EXTRACTION SWITCH OF CLUSTER D

The switch will be composed by a transistor based semi-conductors of type IGBT. Two identical switches of 15 kA will each consist of 8 elements in parallel and both racks will be located in the Cluster D area under the platform. Each rack is again split up in two modules, rated for 7.5 kA. One IGBT will carry a maximum of 1.875 A depending on number of elements in parallel. The current sharing is expected to be better than 5% difference between the individual IGBTs, leading to temporary maximum currents of 1970 A for short durations (minutes). The maximum forward voltage of each switch will be 3 V. Therefore no redundancy in the system will be possible so this switch will be directly acting on the circuit. The command chain will be doubled as far as possible to guaranty the opening of the switch. It will be mono polar and the reaction time (time from FPA to 0 current in the switch) will be less than 1 ms. To be remarked that the max. of 1000 V will be also seen by the switch in blocking mode. The maximum forward losses, roughly 30 kA x 3 V will be 90 kW and water-cooling is needed. At the time of writing this document a flow rate is estimated at 200 l/min. This may decrease since the forward losses are linear with the circuit current and a higher delta T of the water in vs out may be accepted at occasions where 30 kA is needed.

The estimated floor space needed for each of the two switches will be maximum 2 x 1 meters with a maximum height of 2.20 meters. There will be free space of 1 m around each of the switches allowing access to it.

Each 15 kA switch will be connected, by means of a 2x2x200mm2 ultra-low-inductance cable to a separate dump resistor capable of absorbing 5 MJ each grounded via their midpoint.

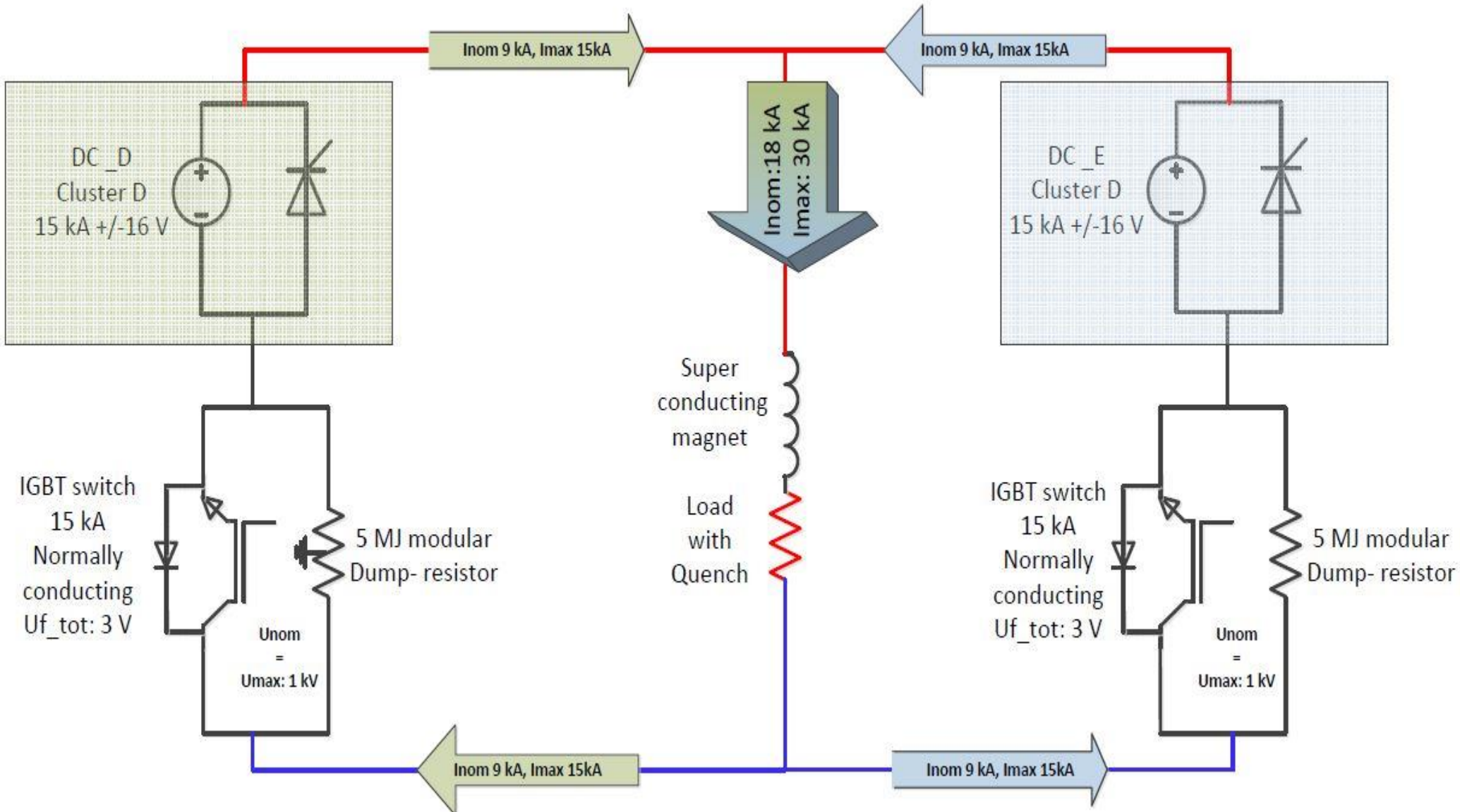
4.1.3 THE DUMP RESISTOR OF THE CLUSTER D

The resistor racks will be located at the first floor as close as possible above the switches. The total modular resistor can be changed roughly between 3.6 and 120 mΩ.

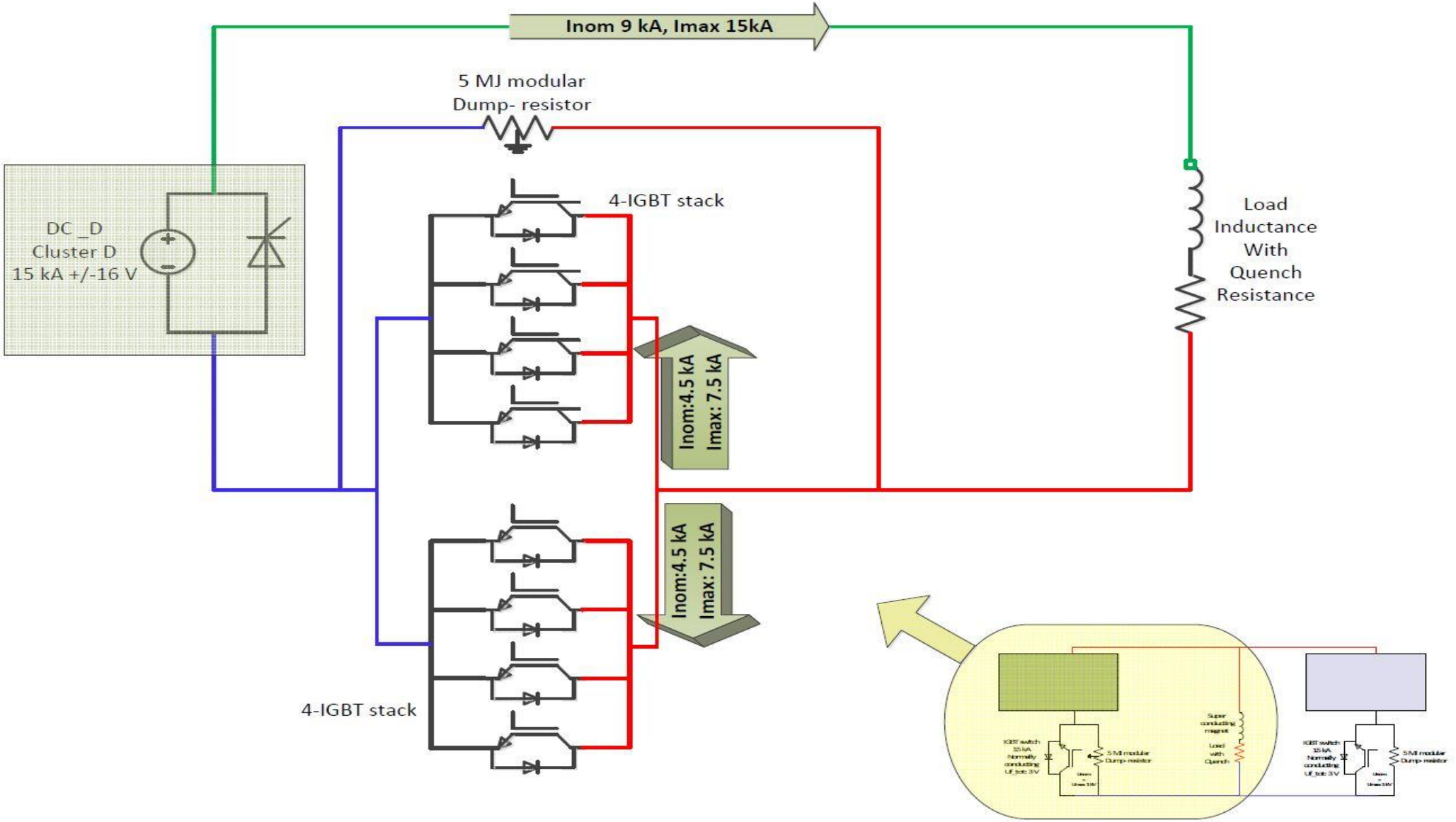
The number of steps in between these values is still to be decided as well as absorbed energy for each resistor value. For each 15 kA switch, a proposal of

6 elements of 40 mΩ and 1 MJ each seems to be a realistic option. Each element will have a mid-point grounding tab. This allows 4 configurations with full energy dump.

Simplified 30 kA schematic



Simplified 15 kA schematic



Design criteria 1

Reliability of the Semi Conductor

- Major failure causes due to
  - **Weak Thermal design (DC application)**
  - **Over-voltages due to stray / parasitical inductances**
  - **Over-current due to unsymmetrical design**

Forward losses reduced because of over-rating

Commercial Availability

Design criteria 2

Lifetime Reliability

- Due to thermal cycling the lifetime decreases drastically

  - Keep Delta T of junction < 80 °

    $Tj_{max} < 110°C$

  - See Alexandr's presentation

Design criteria resumed 3

- **Transient processes lead to high voltage spikes and potential over-currents through single IGBT**
  - Fully symmetrical design
  - Stray inductance to be kept as low as possible
    - non compensated stray inductance will lead to high voltage spikes
  - Fully compensated design
  - Need for multi-level snubber implementation
  - Simultaneous switching of all 16 IGBTs (sub µs range)
  - Trade-off: efficient cooling, current distribution & stray inductance

Project started from 0 in June 2013

- Started with Alexandr and Gert
  - low availability due to LS1
- Conceptual ideas generated during summer/autumn 2013
- Strategic decision to develop in-house
- Detailed study on type of semi-conductors
- Detailed study on low-inductance dump-resistors
- Alignment of controls electronics to SM18 applications
- DAQ systems and instrumentation
- Software controlled actions and PM files
- Thermal management
- Etc…

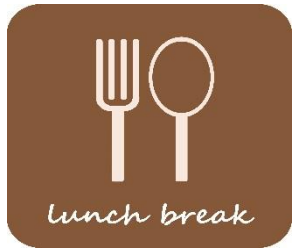
Project status

- Prototype tested! But “only” up to qualification of items regarded as “on the critical path” in the planning
  - Delivery delays expected of 8 – 12 weeks
- Remaining tests to be completed over the next months
  - “in the shadow”
    - EMC tests
    - Reliability tests – endurance tests
    - Reduced water flow
    - Ultimate current
- Ordering of all remaining items after this review
  - For orders over 50 kCHF support is needed at departmental level for single-source procurement

Next presentations:

- 7.5 kA and 30 kA; Topology - Critical Design Issues
- Electronics for Control & Interlocks

- Software and Signals Conditioning
- Mechanics, Rack and Integration within SM18 Facility



- General water system and calculations
- Dump Resistor: Requirements and Design
- Quality Control, Test Program and Results

Thank you for your attention

Additional slides

FIT rate IGBT vs IGCT

The Failures In Time (FIT) rate of a semi-conductor is the number of failures that can be expected in 10^9 hours of operation

- or for 500 devices during 2 million hours (228 years)
  - strongly dependent on the applied voltage
  - small dependence on temperature

Typical FIT numbers for (only to compare IGCT and IGBT)

- IGCT: 100 & Gate driver: 200 => 300
- IGBT: 250 & Gate driver: 150 => 400

- SM18 application FIT numbers should be devided by 100