Contribution ID: **12** Type: **not specified**

Development of redundant and reliable Fast Interlock Controllers using COTS based on IEC 61508 (Luis Fernandes)

Tuesday, 2 February 2016 16:00 (20 minutes)

For interlock functions at ITER requiring a response time faster than the capabilities of the S7-400F PLC an interlock controller using COTS FPGA has been developed. A system based in NI cRIO was designed following the same IEC standard applied to the PLC based interlocks which could reach SIL-3 like integrity.